All Ink-Jet Printed Low-Voltage Organic Field-Effect Transistors on Flexible Substrate

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Abstract

In this work, all ink-jet printed (IJP) low-voltage organic field-effect transistors (OFETs) on flexible substrate are reported. The OFETs use IJP silver (Ag) for source/drain/gate electrodes, poly(4-vinylphenol) (PVP) for gate dielectric, 6,13-bis(triisopropylsilylethynyl)-pentacene (TIPS-pentacene) blended with polystyrene (PS) as the semiconducting layer and CYTOP for encapsulation layer. All the printing processes were carried out in ambient air environment using a single laboratory ink-jet printer Dimatix DMP-2831. The all IJP device presents state-of-the-art performance with low operation voltage down to 3 V, small subthreshold swing (*SS*) of 0.155 V/decade, mobility of 0.26 $cm^2V^{-1}s^{-1}$, threshold voltage (V_{th}) of -0.17 V and on/off ratio of 3.1×10^5, along with a yield of 62.5%. Through interface engineering and proper process optimization, this work demonstrates a promising low-voltage all IJP device platform for low-cost flexible printed electronics.

Keywords

Organic field effect transistors (OFETs); all ink-jet printed TFTs; low-voltage operation

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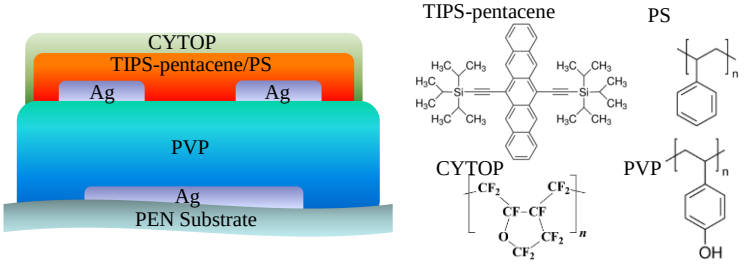
1. Introduction

Solution processed organic field-effect transistors (OFETs) have received considerable attention, owing to their attractive features of low-cost printable processes [1]-[2], superior intrinsic mechanical flexibility [3], and sustainable performance improvement [4]. These fascinating features of OFETs make them perfect candidates for applications as sensors [5], radio frequency identification (RFID) tags [6], smart memories [7], point-of-care diagnostic systems [8], flexible display backplanes [9] and wearable systems [10]. In the past few decades, apart from developing high mobility organic semiconductors [11], significant efforts focused on developing low-cost solution-based processes for OFETs [12]-[14], with ink-jet printing as one of the most promising candidates. Its merits include drop-on-demand direct patterning, non-contact mode, material saving and good compatibility with large area flexible substrates [15], all of which are highly desirable for low-cost and high-throughput electronics [16]-[19]. To further reduce the cost and improve the efficiency for OFETs' manufacturing, an all ink-jet printed (IJP) OFET device platform is highly very much in demand. Up to now, there have been very few publications on all IJP-OFETs [20]-[23]. Most demonstrate high operating voltage of typically a few tens of volts, which would be a bottleneck for most mobile or wearable applications where the electronics have to be powered with battery or AC field. Therefore, reducing the operating voltage of all IJP-OFETs has become a key challenge.

To reduce the operating voltage, we can increase the gate dielectric capacitance per unit area (C_i) [24] and/or reduce the semiconductor/dielectric interface trap density (N_{SS}) [25]. The larger C_i can be achieved by ultrathin or high-*k* gate dielectric. However, a thin gate dielectric can result in large gate leakage and a high-*k* gate dielectric would suffer from the interface dipole disorder [26], neither of which are compatible in all IJP-OFETs. For an all IJP-OFET, a bottom-gate bottom-contact (BGBC) device architecture is preferred [20]-[23], which prints source/drain electrodes on the dielectric layer rather than the process-sensitive semiconductor layer. In previous work, it has been shown that a reduced N_{SS} can be achieved with BGBC device architecture by using a blend of small molecule organic semiconductor and polymer binder [25][27]-[30]. Such an approach would be more compatible with ink-jet printing processes, which provides more flexibility on the dielectric thickness and dielectric constant (*k*) of the gate insulator. In addition, a higher mobility of IJP TIPS-pentacene OFET can be also achieved by blending with insulating polymer [31].

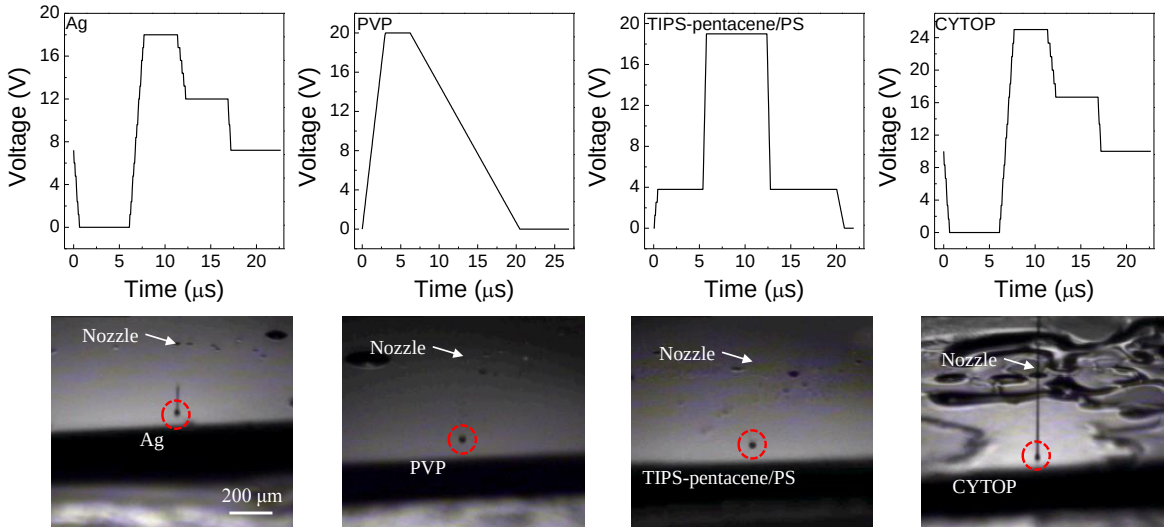
In this work, we adopt the approach of reducing N_{SS} and show that it is effective. Based on a small molecule organic semiconductor blended with polymer dielectric material system, combining with careful process optimization, a low-voltage (< 3 V) all IJP-OFETs on flexible polyethylene naphthalate (PEN) substrate is reported. This work shows the first time through interface engineering and proper process optimization, all IJP low-voltage OFETs on flexible substrate can be achieved in ambient air lab environment.

2. Experimental



(a) (b)

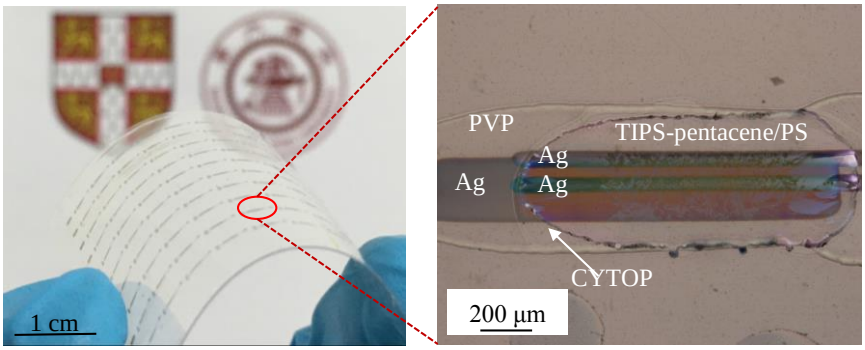
Fig. 1 (a) Schematic diagram of the all IJP-OFETs. (b) Chemical structure of the used materials.



(a) (b) (c) (d)

Fig. 2 Controlling voltage waveform for the ink-jet printing process and photograph of the ink-jetted drops from nozzle for (a) Ag, (b) PVP, (c) TIPS-pentacene/PS and (d) CYTOP.

The device structure of the all IJP-OFETs and the chemical structure of the used materials are shown in Fig. 1 (a) and (b), respectively. The BGBC devices were fabricated on a 125-μm-thick PEN substrate from DuPont. The size of the PEN was 4 cm × 4 cm. The Ag ink (jet-600C) was supplied by Hisense Electronics, Kunshan, China, and the CYTOP (CTL-809M) and its solvent (CT-Solv. 180) were provided by Asahi Glass. All other chemicals were purchased from Sigma-Aldrich. The poly(4-vinylphenol) (PVP) was dissolved in propylene glycol monomethyl ether acetate (PGMEA) at a concentration of 80 mg/mL. Subsequently, the cross-linking reagent poly(melamine-co-formaldehyde) (PMF) was mixed into the solution at a mass ratio of 1:2 to PVP. The mixed solution was then used as ink for the dielectric layer. We used a cross-linkable PVP dielectric as it has been proven to be a suitable gate dielectric for ink-jet printing process, and frequently used in the all IJP-OFETs [20]-[23]. The ink of semiconductor layer was prepared by mixing 6,13-bis(triisopropylsilylethynyl)-pentacene (TIPS-pentacene) and polystyrene (PS) at 10 mg/mL concentration of solids in toluene (3:1 ratio by volume). The blended material system (TIPS-pentacene/PS) appears to reduce N_{SS} [25]. The CYTOP was diluted with a mass ratio of 1:3 to the CYTOP solvent (CT-Solv. 180), and then used as the ink for the encapsulation layer. By careful optimization of the controlling voltage waveform, nice ink-jetted drops out of the nozzle were achieved, as shown in Fig. 2. During the printing, the temperature of the cartridge for Ag, PVP, TIPS-pentacene/PS and CYTOP were 45°C, 35°C, 40°C and 50°C, respectively. The ink-jetted drops shown in Fig. 2 were the prerequisite for device fabrication. All the ink-jet printing processes were conducted with Dimatix DMP-2831 with 10 pL cartridges. The DMP-11610 cartridge was used for Ag ink, and DMPLCP-11610 cartridges were used for the other inks.



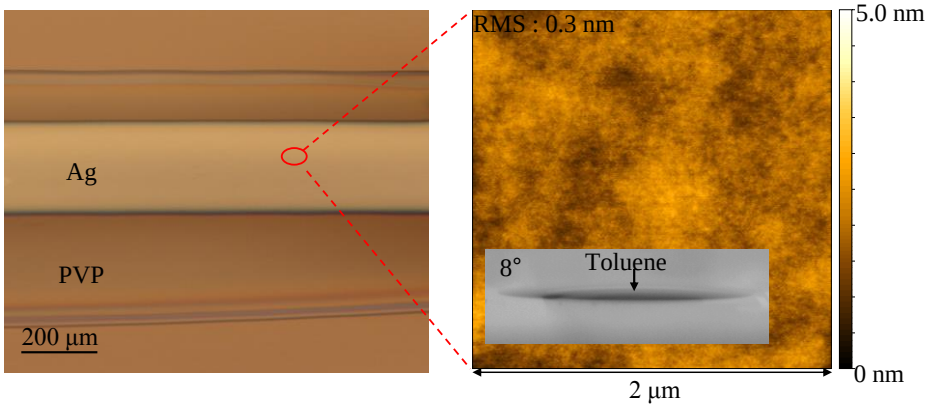
(a) (b)

Fig. 3 (a) Photograph of fabricated flexible sample. (b) Polarized optical micrograph of the fabricated device.

The Ag gate electrode was printed onto the PEN substrate at a drop space (D_S) of 50 μm. The drop frequency (D_F) and the drop height (D_H) from the cartridge nozzle to the top surface of the substrate were 5 kHz and 1 mm, respectively. In all the ink-jet printing processes, the temperature of the printer plate was kept at 30°C. The IJP-Ag was annealed at 150°C for 15 min to form conductive electrodes. Then the sample was treated by ultraviolet/ozone (UV/O_3) for 6 min before printing the PVP dielectric. To avoid the interaction between neighboring PVP lines, a single PVP line was used to cover the whole Ag gate electrode by reducing the D_S. The D_S, D_F and D_H for all-printed PVP were 5 μm, 5 kHz and 1 mm, respectively. The PVP dielectric layer was cross-linked at 150°C for 120 min. For the subsequent the source/drain electrode formation, the Ag ink was printed on PVP surface with the same jetting and annealing parameters as the gate electrode. The channel width (W) and length (L) were 1200 μm and 40 μm, respectively. The surfaces of the source/drain electrodes were then treated by immersing the samples into a 7.5×10^{-3} mol/L solution of perfluorobenzenethiol (PFBT) in ethanol for 3 min and then rinsed with ethanol. The PFBT surface treated Ag electrodes were shown to be able to form good contacts with p-type organic semiconductors [32]. The semiconductor layer was then printed with a D_S of 5 μm, a D_F of 2 kHz and a D_H of 1 mm, followed by an annealing process at 100°C for 30 min. Finally, the CYTOP ink was printed as the encapsulation layer. The D_S, D_F and D_H for CYTOP were 5 μm, 2 kHz and 1 mm, respectively. After the process of printing the encapsulation layer, the sample was heated at 100°C for 30 min before measurements. The photograph of the sample and the polarized optical micrograph of the device are shown in Fig. 3 (a) and (b), respectively.

In this work, all the printing processes and measurement were carried out in a non-cleanroom, ambient-air environment. The electrical properties of the devices were characterized with a Keithley 4200 Semiconductor Characterization System. The surface roughness of the PVP film was recorded with a Veeco EnviroScope atomic force microscope. The thickness was measured with a Dektak surface profilometer. The wetting property of PVP surface was characterized by a video contact-angle analyzer SL200B. The polarized optical micrographs were taken with a Nikon Eclipse ME600. The UV/O_3 treatment was carried out with a Bioforce Nanosciences Procleaner 220.

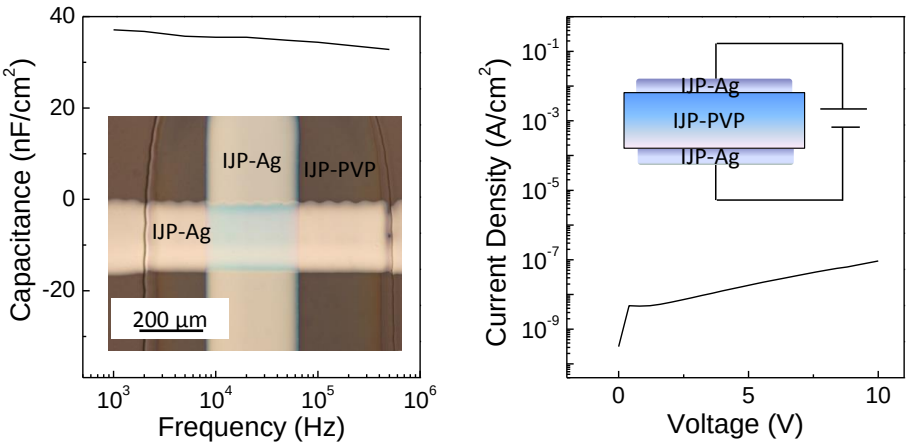
3. Results and discussions



(a) (b)

Fig. 4 (a) Optical micrograph of the device with IJP-PVP dielectric on Ag gate electrode. (b) Measured atomic force micrograph (AFM) image of the PVP film. Measured toluene contact angle of the film is shown in inset.

As shown in Fig. 4 (a), the single IJP-PVP line covers the whole Ag gate electrode, which is thought to be beneficial for a smooth surface of dielectric to avoid possible interaction between neighboring PVP lines. The measured atomic force micrograph (AFM) image of the PVP film is shown in Fig. 4 (b). It shows a very smooth surface with a root mean square (RMS) roughness of about 0.3 nm. The smooth surface is very important for forming a high quality semiconductor/dielectric interface. Meanwhile, the strong wetting property of the semiconductor solvent (toluene in this work) on the PVP surface is also essential in bottom-gate OFETs [33], as shown in the inset of Fig. 4 (b). Through careful interface engineering, a high-quality semiconductor/dielectric interface is obtained, which is prerequisite to reduce N_{SS}.

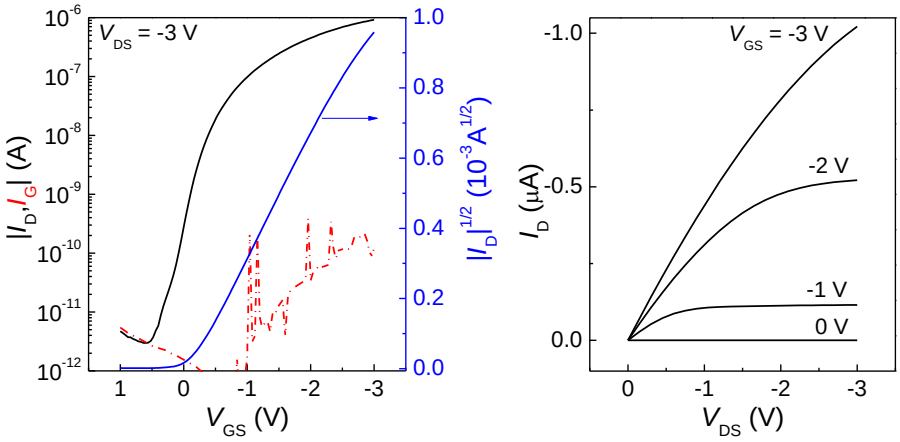


(a) (b)

Fig. 5 (a) Measured capacitance as a function of frequency and (b) leakage current density as a function of voltage for the IJP-PVP dielectric. Optical micrograph and schematic diagram of the test structure Ag/PVP/Ag are shown in the insets of (a) and (b), respectively.

The capacitance as a function of frequency for IJP-PVP dielectric is presented in Fig. 5 (a). The C_i is measured to be 37.0 nF/cm^2 at a frequency of 1 kHz. The measured thickness is 103 nm yielding a dielectric constant k of 4.3 at 1 kHz. The leakage current density is shown in Fig. 5 (b), with a value of

2.3 × 10^{-7} A/cm^2 at a bias voltage of 10 V. The optical micrograph and schematic diagram of the test structure are shown as insets in Fig. 5 (a) and (b), respectively.



(a) (b)

Fig. 6 Measured electrical characteristics of the fabricated OFETs: (a) transfer characteristics (I_D-V_{GS}) and (b) output characteristics (I_D-V_{DS}).

Figure 6 shows the measured transfer (I_D-V_{GS}) and output (I_D-V_{DS}) electrical characteristics of the fabricated OFETs. The device presents a threshold voltage (V_{th}) of -0.17 V, mobility of 0.26 cm^{2}V^{-1}s^{-1}, an on/off ratio of 10^5-10^6 with a small subthreshold swing (*SS*) of 0.155 V/decade. The V_{th} value was estimated through a linear fit of the square root of I_D versus V_{GS} plot with its intercept on the *x-axis* as illustrated in Fig. 6 (a). The mobility was calculated by fitting the plot of the square root of I_D versus V_{GS} using the following equation:

$$I_D = \frac{\mu C_i W}{2L}(V_{GS} - V_{th})^2 \quad (1)$$

where μ is the mobility, L the channel length, W the channel width and C_i the gate dielectric capacitance per unit area. To the best of our knowledge, this is the first report of low operating voltage for an all IJP-OFET is achieved.

The required voltage swing to switch OFETs is highly dependent on the subthreshold swing (*SS*), which can be described as [34]:

$$SS = \ln 10 \cdot \frac{k_B T}{q} \cdot \left(1 + \frac{q^2 N_{SS}}{C_i}\right) \quad (2)$$

where k_B is Boltzman's constant, T the absolute temperature, N_{SS} the semiconductor/dielectric interface trap density, q the elementary charge, and C_i the gate dielectric capacitance per unit area. According to equation (2), since $k_B T/q$ is a constant, the required operating voltage for the OFET depends on both the C_i and N_{SS}. A larger C_i and a lower N_{SS} are preferred for low-voltage operation.

Table 1 Comparison of substrate, C_i, mobility, V_{th}, highest on/off ratio, operation voltage, *SS* and N_{SS} for this work and other reported all IJP-OFETs.

Work	Substrate	C_i (nF/cm^2)	Mobility ($cm^2V^{-1}s^{-1}$)	V_{th}	Highest On/off Ratio	Operation Voltage (V)	*SS* (V/decade)	N_{SS} ($eV^{-1}cm^{-2}$)
[20]	Polyarylate	3.8	0.02	-1.2	10^4	60	2.52	9.80×10^{11}
[21]	PEN	2.4	0.02	-14.0	1.2×10^2	30	N/A	N/A
[22]	Wafer	33.8	0.01	-1.5	1.4×10^3	40	4.28	1.50×10^{13}
[23]	PEN	5.3	0.00025	-3.5	2.0×10^2	30	N/A	N/A
Our work	**PEN**	**37.0**	**0.26**	**-0.17**	**3.1×10^5**	**3**	**0.155**	**3.70×10^{11}**

N/A: Not available.

A systematic comparison of extracted device parameters for devices in this work and all IJP-OFETs reported in the literature is shown in Tab. 1. It can be seen that that the overall performance of the devices reported here is very promising. The value of N_{SS} is calculated to be 3.70×10^{11} $eV^{-1}cm^{-2}$, which is also the lowest value reported for all IJP-OFETs. We believe that the reduced N_{SS} and larger C_i as listed in Tab. 1 are the main reasons for the reduced operating voltage of our OFETs.

In earlier reports on all IJP-OFETs [20]-[23], thick dielectrics were usually used to avoid dielectric breakdown, which yield a small C_i. Meanwhile, the small-molecule-only semiconductor system used in these papers [20]-[23] suffers from a relatively high N_{SS} due to the poor crystallization control during the ink-jet printing process. As a result, the operating voltages tend to be very high (>30V). Meanwhile reports have demonstrated that a blend of small molecule organic semiconductor and polymer binder is useful to reduce the N_{SS} [25][27]-[30], due to the better semiconductor crystallization induced by vertical phase separation [35]. The different solubility parameters between small molecule organic semiconductor and polymer binder is responsible for the vertical phase separation [35]-[36]. This approach for low-voltage operation is more compatible with low-cost printing processes, since there is less strict requirement on the value of C_i. Moreover, the low-voltage operating property also decreases the likelihood of dielectric breakdown by virtue of lower gate electric field, thus providing a much wider process window of IJP dielectrics. These attributes open up the possibility of realizing low-voltage all IJP-OFETs by reducing the interface state density. To make this approach effective, a smooth surface and proper wetting property of the dielectric are very important. In this work, the strong wetting property of the PVP dielectric shown in the inset of Fig. 4 (b), is consistent with earlier reports [20]-[23]. Moreover, the smooth surface of the PVP dielectric is achieved through the method of single-line printing with a small D_S, as shown in Fig. 4 (b). A smooth surface is important for low voltage operation since surface/interface roughness hinder charge transport through additional scattering and by increasing defect states at the interface.

Finally, the transfer characteristics of 50 OFETs are shown in Fig. 7 (a). The devices are classified as failures when the on/off ratio is lower than 500. The yield is 62.5% (i.e. 50 out of 80 functional) for the all IJP-OFETs over 4 cm $\times$ 4 cm size flexible substrate. The histograms of the extracted mobility, on/off ratio, V_{th} and *SS* for the 50 OFETs are also shown in Fig. 7. The low on/off ratio of the failed devices is attributed to the printing misalignment, and also the gate leakage. The yield can be improved by using an industry-standard ink-jet printer and a thicker gate dielectric in the future work. Considering that all processes were carried out in a non-cleanroom ambient-air environment using a single Dimatix DMP-2831, the results shown are very encouraging.

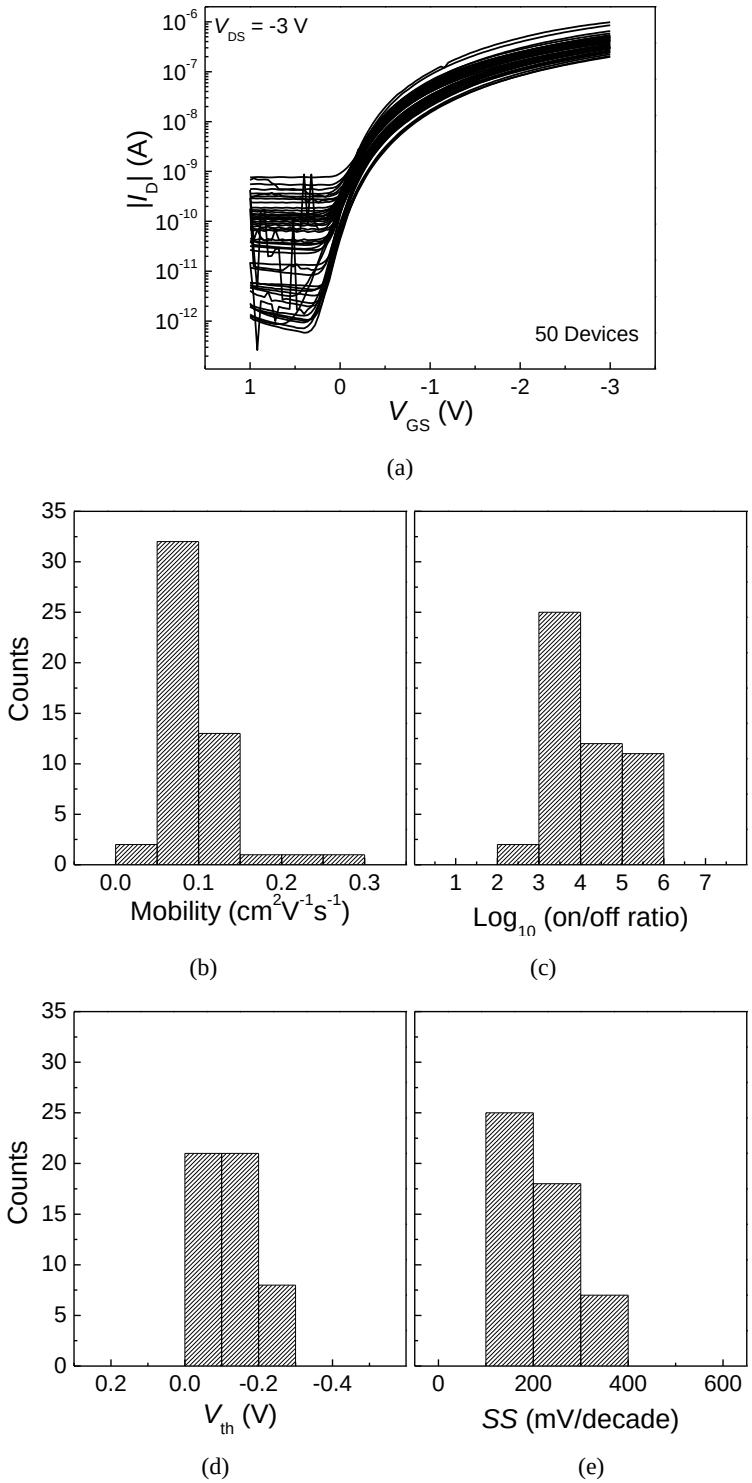


Fig. 7 (a) Measured transfer characteristics of 50 all IJP-OFETs over the 4 cm × 4 cm size flexible substrate. Histograms of 50 all IJP-OFETs over the 4 cm × 4 cm size flexible substrate: (b) mobility, (c) on/off ratio, (d) threshold voltage and (e) subthreshold swing.

4. Conclusion

With proper device architecture, material selection and process optimization, this work demonstrates that low-voltage OFETs can be achieved using low-cost printing processes. The approach of reducing the interface state density at the semiconductor/gate dielectric interface proved to be effective in reducing the OTFTs operating voltage. Since all the processes were carried out in non-cleanroom ambient-air environment using a single laboratory printer (Dimatix DMP-2831), and not exceeding a process temperature of 150°C, this work would open a new route for development of commercially viable printed OFET technology platform for low-cost, low-power, flexible electronics.

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