Defect State Passivation at III-V – oxide Interfaces for CMOS devices

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Abstract
The paper describes the reasons for the greater difficulty in the passivation of interface defects of III-V semiconductors like GaAs. These include the more complex reconstructions of the starting surface which already possess defect configurations, the possibility of injecting As antisites into the substrate which give rise to gap states, and the need to avoid As-As bonds and As dangling bonds which give rise to gap states. The nature of likely defect configurations in terms of their electronic structure is described. The benefits of diffusion barriers and surface nitridation are discussed.

Introduction

The dominance of silicon in semiconductor technology is not based on its superior transport properties, but on the high quality (smoothness, abruptness and lack of electronically active defects) of the Si-SiO_2 interface [1]. However, the continued scaling of metal oxide field effect transistors (MOSFETs) will now need the use of higher mobility semiconductors such as the III-V semiconductors GaAs and InGaAs [2-5]. The use of III-Vs in MOSFETs has been delayed for many years by the poor quality of their oxide interfaces.

Historically, the surfaces of III-V semiconductors have been very difficult to passivate. This first arose in the 1980's surface science experiments when it was found that the introduction of oxygen or metal atoms on the non-polar GaAs(110) surfaces led to the pinning of the Fermi energy (E_F), even at very low surface coverage (Fig. 1)[6]. The pure GaAs(110) surface has no surface states in the gap, so that the ideal surface would not pin E_F. Spicer et al [6,7] proposed a 'unified defect model' to account for the observed Fermi level pinning, and attributed the pinning to vacancy defects. A second version of the model later attributed the pinning to antisite defects instead of vacancies [8]. However, the existence of Fermi level pinning inhibited the development of GaAs-based MOSFETs for some period.

At the same time, the native oxide of GaAs was known to be of low quality and to contain many defects [9-11]. The alternative is to use a non-native dielectric. Generally, there are rather few examples of good non-native dielectrics on semiconductors; silicon nitride on amorphous silicon being one of the few good cases. Hasegawa [9,10] tabulated the measured interface state densities (D_{it}) of various deposited dielectrics on GaAs, which showed that they possessed high D_{it} values, as seen in Fig. 2. Various surface treatments such as the use of ammonium sulphide were also found to improve the situation [12-14].

Remarkably, it was then found that an epitaxial Ga,Gd oxide deposited by electron beam evaporation onto GaAs would give a low enough D_{it} to allow the fabrication of functioning MOSFETs [15,16]. These results resulted in a prolonged effort to develop the GaAs MOSFETs [17]. There were numerous efforts to characterise the interfaces, such as by photo-luminescence (Fig. 3) and scanning tunnelling spectroscopy, compared to those formed by other oxides [10,18-20].

The status of using non-native oxides completely changed with the development of high dielectric constant (high K) oxides such as HfO_2 to replace SiO_2 as the gate dielectric of Si MOSFETs [21,22]. The use of atomic layer deposition (ALD) was particularly important in this, as a practical, commercial technique to controllably deposit very thin films [5]. Thus, ALD was then considered for the deposition of dielectrics such as Al_2O_3 and HfO_2 onto GaAs and other III-V semiconductors [23-25].

A second advance was the use of more advanced surface characterisation techniques, such as in-situ photoemission spectroscopy and synchrotron radiation sources that allowed us to monitor the chemistry of every stage of the ALD growth process [26,27].

These advances have now allowed very good III-V based MOSFETs to be fabricated, in a way suitable for commercial production. A landmark event was Intel's announcement of the first InGaAs quantum well MOSFET which used an InP capping layer and a Ta silicate gate dielectric [28,29], as shown in Fig 4. It showed that a fully engineered III-V FET was possible.

There have been numerous studies of the interface states and their relation to ALD on III-V substrates, and how to improve and understand the ALD process [26,27,30-39]. It is now useful to understand what has made III-V semiconductors more difficult to passivate and how this can be overcome by better understanding of the surface chemistry.

The anomalous situation of III-Vs should also be pointed out. Defect passivation in general occurs because defects are often under-coordinated so that bonding some defect species X to a small univalent atom like hydrogen or bonding it to reactive oxygen atoms will be exothermic, due to the formation of X-H or X-O bonds, which removes states from the band gap, Fig 5. Thus the driving force for passivation is usually energy gain.

What causes interface states

We first consider some general questions. There are two types of gap states at metal – semiconductor interfaces; first the intrinsic states due to the decay of the extended metal states into the semiconductor band gap (also called metal induced gap states or MIGS), Fig 6(a), and second the extrinsic states around the interface due to specific defects [40]. Turning to interfaces between two semiconductors, or between a semiconductor and an oxide, the MIGS type state can only exist where there are extended states on the other side of the interface; that is there will be no MIGS type states within the band gap of the narrower gap material, usually the semiconductor [40], as shown in Fig 6(b). Interface states here can only come from defects.

The MIGS and defect states often change their character across the band gap, from being donor-like in the lower gap to being acceptor-like in the upper gap. There is an energy where this change-over occurs. It is called the charge neutrality level (CNL) for the MIGS, and it is called the trap neutrality level (TNL) for the defect states. Perhaps confusingly, the CNL and TNL often have numerically similar energies [40,41].

Origin of Interface States in III-V oxide interfaces.

There are two main possible causes of the excess defect density at III-V oxide interfaces. The first is lattice mismatching or strain. The oxidation of Si or a III-V to give SiO_2 or other oxide leads to a factor 2.4 increase of volume [42]. Unless the oxide can relax, this leads to strain at the interface which can create dangling bonds, because of a mismatch of the two lattices [43]. On the other hand, there are many cases like deposited oxides which do not create strain, or where lattice-matched oxides are used and there is no large volume expansion. Thus strain is not a universal problem at a III-V interface, but a large D_{it} is.

The remaining source of defects is chemistry, and the difference in bonding of GaAs interfaces to that of elemental semiconductors. Some years ago, Harrison [44] considered the bonding at Ge-GaAs interfaces. Si or Ge atoms have four valence electrons, so that each of their sp^3 hybrids forming bonds is allocated 1 electron. On the other hand, for GaAs, Ga has 3 valence electrons, so that each of its sp^3 hybrids has ¾ of an electron, whereas As has 5 valence electrons so each of its sp^5 hybrids has 5/4 electrons. This is satisfactory in bulk GaAs because 1 Ga hybrid and 1 As hybrid still makes a 2-electron bond.

At the non-polar (110) interface, there will be Ge-Gas bonds and Ge-As bonds. Each bond will be either ¼ electron below or ¼ electron above its requirement, but they can transfer that ¼

between adjacent bonds to maintain neutrality, Fig 7a. On the other hand, at a polar GaAs(100) interface, the GaAs side is either Ga or As terminated. There will be a lack of ½ electron or an excess of ½ electron. This will lead to a divergent potential if extended to infinity (Fig 7b). Harrison [44] showed that this can only be counteracted if the interface becomes non-abrupt and spread over three layers to allow mixtures of Ga-Ge and As-Ge bonds to remove that singularity, fig 7c. In effect, there is an electron counting rule which says that locally the number of electrons over 2 bonds should add up to eight.

It is notable that GaAs surfaces have much more complex reconstructions that those of Si surfaces. The 2x1Si(100) surface consists of a simple pairing of adjacent Si sites in the outer layer only. On the other hand, GaAs(100) has a number of reconstructions. A typical one is the (2x4)GaAs(100) surface which covers three layers (Fig 8) [45-47]. The observed reconstructions of GaAs (and ZnSe) were found by Pashley [48] to be described by an electron counting rule, illustrating its importance. The surface reconstructions of GaAs can generally possess Ga dangling bonds (DBs), As dangling bonds, Ga-Ga dimers and As-As dimers. The energy levels of these configurations can be calculated (Fig 9); dimers give rise to bonding and anti-bonding states, Ga DBs give states near the conduction band edge and As DBs give state near the valence band edge. If the Fermi energy is to lie near midgap, this requires all bonding states to be filled, all As DB states to be filled and Ga DB states to be empty. We can compare this requirement to the ¾ or 5/4 electrons in each neutral sp^3 hybrid. This gives an electron-counting rule and this leads to a sum rule for the number of Ga or As DBs, and the number of Ga-Ga or As-As dimers. It turns out that the 2x4 reconstruction of GaAs(100), which contains 3 As-As dimers, 6 As DBs and 2 Ga DBs, is one of the simplest reconstructions to satisfy this electron counting rule. Thus the (2x4) GaAs(100) reconstruction is not a consequence of an excess of As at the surface, but a consequence of the electron counting rule [48]. The same rule applies to the interface bonding and is an origin of its higher than usual defect density.

We can see three roles that the dielectric must perform to give rise to a low D_{it}.

(1) The first is that complex surface reconstructions of GaAs should be broken up and returned to simpler, flatter 1x1 configurations [49,50]. Growing oxide films should not bury defect complexes such as the As-As dimer bonds that give rise to gap states. The Al_2O_3 precursor trimethyl aluminium (TMA) is useful because it is a small molecule that will insert into As-As bonds, breaking them [27], Fig 10. Clemens [51] has observed that TMA will cause a rearrangement of the (4x2)InGaAs reconstruction, removing some dimer bonds. Pi et al [36,39] have studied the evolution of the (2x4) GaAs(100) under ALD cycles of TMA and water, and found that the upper layer As-As dimers are disrupted, but the third layer dimers are not so easily disrupted. On the other hand, it is notable that Si starts with a flat hydrogen-terminated unreconstructed (100)Si surface [52] (Fig 11), on which ALD can occur. No defect species get buried. The Hf precursors tend to be larger molecules than TMA [27]. They do appear to insert into As-As dimers according to Pi et al [36], but generally they could be less effective than a smaller molecule.

(2) The dielectric should act as a diffusion barrier to prevent the accidental oxidation of the III-V substrate. Al_2O_3 is generally a good diffusion barrier, Fig 12. The reason is that the Ga of GaAs is preferentially oxidised, as Ga_2O_3 as a higher heat of formation. This leads to an excess of As, and some As interstitials will be injected into the substrate. The same injection process will occur at Si/SiO_2 interfaces during oxidation. The difference is that Si is a single element. On the other hand, As interstitials will react with the interior of GaAs and form As_{Ga} antisites, and these defects give rise to gap states which have been observed by electron spin resonance (ESR) by Stesmans [53]. Thus, a diffusion barrier of Al2O3 will prevent this, Fig 12b.

(3) The interface should also follow the electron-counting rule. This favours trivalent oxides [49,50]. The ideal polar GaAs(100) surface can have two terminations, Ga-terminated or As-terminated. If say a Ga-terminated face is connected to an O-terminated HfO_2(100) layer, then the interface will be lacking ½ electron, and E_F will lie in the valence band. This contrasts to the case

of O-terminated HfO_2 on Si(100), which obeys the electron counting rule, and for which E_F lies in midgap, giving an insulating interface [54]. On the other hand, an As-terminated GaAs(100) face bonding to O-terminated HfO_2 will have ½ too much, and E_F will then lie in the conduction band.

Interestingly, if As-terminated GaAs(100) is bonded to Al-terminated Al_2O_3 then there are just the right number of electrons to satisfy the rule. The ionic charges of the layers can be seen in fig 6. If As is taken as –3, and Ga is taken as +3, then the As layer of 2 As is –6, the 2 Ga's are +6. In the Al_2O_3, there are 2 Al's counting as +6 and three oxygens, counting as –6. So the +6 / -6 alternation continues on both sides of the interface [49,50].

Thus an abrupt insulating interface between a trivalent oxide and GaAs(100) is possible. Ga termination on the GaAs side should be matched by O termination on the other, and As termination on GaAs by Al termination of Al_2O_3.

The same electron counting rules apply to trivalent transition metal oxides such as Gd_2O_3 [49]. These are the oxides used in epitaxial interfaces, which were first discovered to be effective passivants. On the other hand, Al_2O_3 tends to be amorphous, but the interface bonding only depends on the Al valence. If a trivalent oxide is not used, Robertson [50] showed how defects could be generated to compensate and drive E_F into the midgap.

It is also important to realise that Si process technology can produce simple passivated surfaces in a low vacuum system, we do not use ultra-high vacuum systems as used in physics experiments. The Si(100) surface has a simple 2x1 reconstruction. Treatment with hydrofluoric acid coverts it to the 1x1 hydrogen terminated surface, which is passivated and also simple. On the other hand, it can be treated with an acid, and converted into an ultra-thin chemical oxide surface from which would be the best nucleation point for oxide ALD. This route is not so far possible for III-V substrates.

Another advantageous factor of ALD is the self-cleaning effect [33,35]. Whereas ALD of oxides on Si starts with the oxidation half-cycle, ALD on a III-V start with the metal precursor such as TMA first. TMA reacts strongly with any sub-oxides which might be present accidentally on the surface, and returns the surface to a more pristine condition, as seen by in-situ XPS [32,33,26,35]. This allows a finite pressure process to give high quality interfaces, as if it were a UHV process.

Defect Gap States

We now describe the states created by interfacial defects [49,50,55-65]. It should be noted that the most important defects are those on the semiconductor side due to dimers or dangling bonds. These defects are strongly localised and their energy levels are to first order independent on the type of oxide that is bonded on the other side. Again defects in the oxide side are also quite localised, and these depend mainly on the nature of the oxide itself, not the substrate.

We can use an interface between Al_2O_3 and the III-V as the ideal model interface with no defects, as in Fig 13d [55,58]. It has no gap states. The ideal non-polar HfO_2/GaAs(110) interface is another suitable model into which we can introduce defects. Both interfaces have no gap states (Fig 14). A polar (100)HfO_2:GaAs interface model can be used, provided that substitute atoms are introduced to satisfy the electron counting rule [55,58].

Fig 15a shows the Ga dangling bond created at the (110) model interface [59]. Fig 15b shows its electronic structure and the resulting partial density of states (PDOS). It is seen that the Ga DB gives rise to an empty state just into the conduction band. As it is empty, the Ga site is positively charged and this causes this site to relax towards more planar geometry (Fig 15a).

Fig 15c shows the As dangling bond. It can be modelled at the (100) or (110) interface [59]. This gives rise to a state around the valence band edge. This state is easily filled, and then the state lies just above the valence band top (Fig 15d). It is a likely source of gap states seen in D_{it}. Because the As DB state is filled, it causes the As site to become negatively charged, and so the As site relaxes into a more pyramidal geometry.

Fig 16a shows an interface with a Ga-Ga dimer bond, and Fig 16b shows the resulting PDOS [57]. We see that this defect introduces an empty Ga-Ga anti-bonding state well into conduction band, and a filled bonding state in the upper valence band at –2 eV. Thus, it gives no gap states.

Fig 16c shows the As-As dimer configuration created at a (100) interface. This gives rise to an empty gap state lying below the GaAs conduction band (Fig 16d). The wavefunction of this antibonding state is shown in Fig 16c. This is a candidate for the defect state seen at midgap and in the upper gap range [57-60].

The defect states were also calculated in the other III-V oxide interfaces [57,60]. The resulting chemical trends are shown in Fig 17. First, the bulk band edges have been aligned using their bulk CNL energies. The valence band edges of GaAs and InAs lie at similar energies, the conduction band edge of GaAs is higher. InP has a wider gap than GaAs both because of its higher CB and a lower VB.

We see that the As dangling bond forms a gap state above the VB in both GaAs and InAs. This is the likely cause of defects in this range. We see that the As-As dimer forms a gap state in GaAs, but that this gap state lies above the CB in InGaAs and InAs [60]. The P-P antibonding state lies above the gap in InP, due to the stronger P-P bond, Fig 18.

There are four reasons to attribute the As-As dimer as the main cause of state in mid and upper gap, rather than say the Ga dangling bond [57]. First, the chemical trend is better. InGaAs has a lower D_{it} than GaAs, and thus their FETs have much *higher* conductances. This was first noted by the model of Ye [41,66]. If the defect was the metal site DB, then this state would follow the conduction band edge down, and the D_{it} would not change, but it does. It is notable that the chemical trends of the interface defect energy levels follow those of defect levels in the amorphous semiconductors [65].

The second reason is that the resonant state of the As-As bond has been observed experimentally in the CB of InGaAs. MOSFETs of InGaAs show a lower field effect conductance compared to their Hall effect conductance, and this can be attributed to induced charge lying in the resonant bound states, rather than in the conducting states [67]. These states lie experimentally where they are predicted (Fig 19). (Their energy can be varied slightly by varying the interface passivation (with or without S) and the nature of the oxide [67]).

The third reason is the better performance of GaAs FETs on the (111)A face than on (100) [68]. We have noted the problems caused by the presence of As-As dimers on the GaAs(100) face. The GaAs(111) face is polar with two terminations, A and B. The A face is Ga-terminated, and to ensure that it is stable, it adopts a defective 2x2 reconstruction with ¼ of Ga atoms as surface vacancies [69,70], Fig 20. This reconstruction has no As-As bonds. Thus the presence of As-As bonds on (100) and absence of As-As bonds on (111)A surface is strongly correlated with the better performance of FETs made with the (111)A face [54].

We also note that the P-P bond's anti-bonding state lies above the CB in InP. This allows InP to form good MOSFETs, which indeed occurs. It also explains why InP can be used as a capping layer in the first InGaAs QW FETs [28]. The InP removed any possible As-As dimers, while any P-P dimers would lie safely in the InP conduction band.

The early CV data for GaAs interfaces showed a peak in D_{it} near midgap [71]. This has gradually been removed as deposition techniques have been removed [32,35,27]. It is possible that this state corresponds to the -/2- transition of the As-As antibonding state. This transition corresponds to the breaking of the As-As bond as the antibonding state becomes occupied [72].

The usefulness of having an Al2O3 based diffusion barrier in the high K stack on GaAs was emphasised by the results of Suzuki [73]. They found that even a few ALD cycles of Al2O3 under a HfO2 stack was sufficient to reduce the overall D_{it}, Fig 21. This allows a very low effective oxide thickness (EOT) to be achieved [73]. The use of combined Al2O3/HfO2 gate stacks has been found to be useful by a number of groups [73-75].

They also found that a plasma nitridation was useful to reduce D_{it} [76,77]. This has the effect of converting some of the Al2O3 into AlN. AlN is useful as it is also a diffusion barrier. It is

calculated that N dangling bond states lie much deeper below the valence band edge well below the gap [60]. On the other hand, possible N-N dimer bonds do not occur, they are unstable and split into N dangling bonds. Thus, the troubling anion antibonding state does not occur for nitrided interfaces [60].

Hasegawa [9,10,78] noted the different shape of the CV plot for III-V oxide interfaces to those of Si-oxide interfaces. There have been a number of models for the cause of this difference, in terms of the defect density of states. The extraction of density of states from the CV plots requires use of a range of measurement temperatures [71]. The lower effective mass of III-V semiconductors affects the time response and impact of defect states on the CV plot. Yuan et al [79] have proposed that the major component of the defects are border traps, located in the oxide close to the interface. Galatage et al [80] have proposed that the defects are disorder related and at the interface, based on their dependence on the nature of the III-V. There are similarities between the models, in that they give similar response time constants. The interfaces of Yuan et al [79] initially were more abrupt with better deposition conditions.

Finally, the implementation of III_V MOSFETS requires great efforts to integrate the III-V semiconductors channels into an overall Si platform, and to work out the preferred fabrication procedure. This has been reviewed in various articles [2-4,81].

Summary

III-V semiconductor MOSFETs are being introduced based on great improvements in the quality of the semiconductor-oxide interface and the measurement techniques now available. We have reviewed the understanding of interface defect states in these systems, and how to gain the lowest defect densities. Our emphasis on need for diffusion barriers, breaking surface reconstructions and valence satisfaction have developed from those in previous reviews [49].

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Figure captions (please keep figures to single column)

1. Fermi level pinning revealed on GaAs(110) as a function of (a) oxygen coverage, (b) absorption element. From [6].
2. The high interface defect density across the band gap for various interfaces of GaAs, compared to those on InP and for GaAs/InGaAs heterostructures.
3. Photoluminescence efficiency for various passivation schemes on GaAs, from [19]. PL efficiency varies inversely with defect density.
4. InGaAs quantum well MOSFET device, from Radosavljevic [28].
5. Driving force for defect passivation as bonding energy gain, which removes states from the gap.
6. States at (a) metal – semiconductor and (b) semiconductor – oxide interface showing allowed energy ranges of metal induced gap states.
7. (a) Abrupt interface for non-polar Ge/GaAs(110) interface, (b) divergence for polar Ge/GaAs(100) interface, and non-divergence for polar non-abrupt (100) interface.
8. The (2x4) reconstruction of GaAs(100) surface.
9. Generalised energy levels for dangling bonds and like-atom bonds for GaAs.
10. Insertion of TMA into As-As dimers on the 2x4GaAs(100) surface.
11. Hydrogen terminated (2x1)Si(100) surface, showing flatness.
12. (a) oxidation leading to injection of As interstitials into GaAs substrate, giving As_{Ga} antisites. (b) oxygen diffusion barrier inhibiting this process.
13. (100) interfaces for Si/HfO_2, GaAs/HfO_2, GaAs/Gd_2O_3 and GaAs/Al_2O_3.
14. Abrupt (100)GaAs/ Al_2O interface and its partial density of states.
15. Structure, defect orbital, and calculated partial density of states (PDOS) for (a,b) Ga dangling bond, and (c,d) As dangling bond.
16. Structure, defect orbital, and calculated partial density of states (PDOS) for (a,b) Ga-As dimer bond, (c,d) As-As dimer bond.
17. Chemical trends of defect energy levels for dangling bonds and dimer bonds.
18. Calculated PDOS of P-P bond art InP/ Al_2O_3 interface.
19. Comparison of resonant state energies in InGaAs/ Al_2O_3 interfaces, compared to calculated energies.
20. The (2x2)GaAs(111)A surface reconstruction, with Ga surface vacancy and no As-As bonds.
21. Showing InGaAs/Al_2O_3/HfO_2 gate stack, and its associated measured D_{it}, from [73].
22. Showing D_{it} of nitrided InGaAs/ Al_2O_3 gate stack, from [76].
23. Structure, and calculated partial density of states for N dangling bond at GaAs/Al2O3 interface.

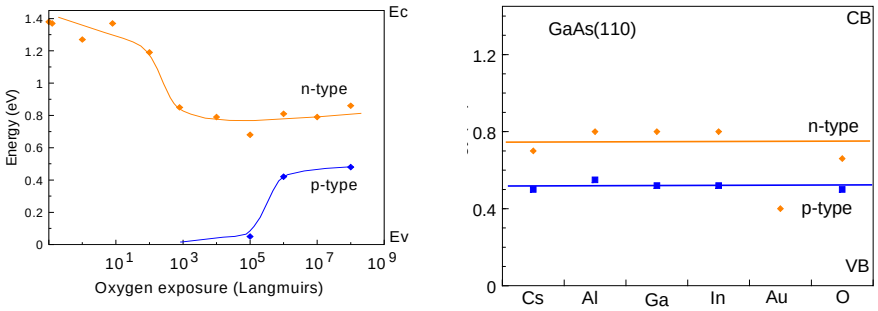
Ec
Ev
n-type
p-type
Energy (eV)
Oxygen exposure (Langmuirs)
GaAs(110)
CB
VB
n-type
p-type
Cs
Al
Ga
In
Au
O

Fig. 1.

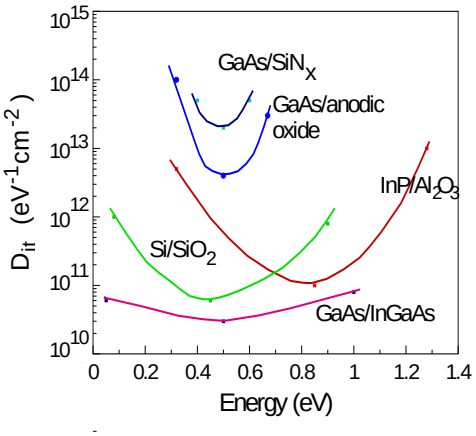
10^{15}
10^{14}
10^{13}
10^{12}
10^{11}
10^{10}
D_{it} ($eV^{-1}cm^{-2}$)
GaAs/SiN_X
GaAs/anodic oxide
InP/Al_2O_3
Si/SiO_2
GaAs/InGaAs
0
0.2
0.4
0.6
0.8
1
1.2
1.4
Energy (eV)

Fig. 2.

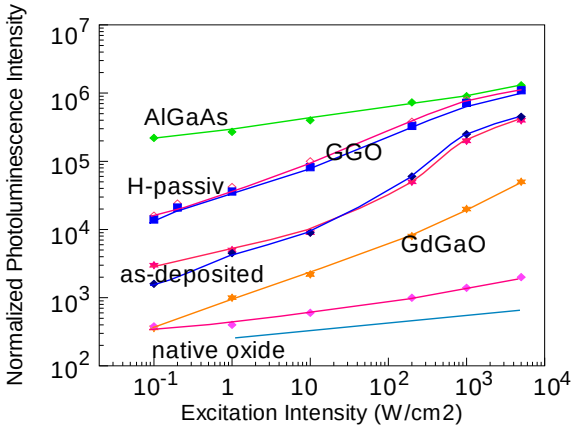
Normalized Photoluminescence Intensity
10^7
10^6
10^5
10^4
10^3
10^2
AlGaAs
GGO
H-passiv
GdGaO
as-deposited
native oxide
10^{-1}
1
10
10^2
10^3
10^4
Excitation Intensity (W/cm2)

Fig. 3.

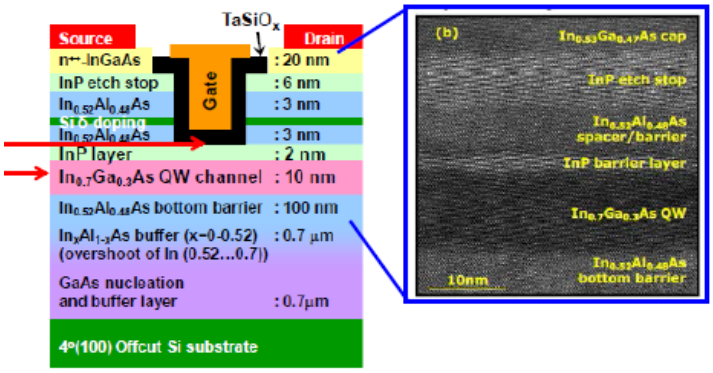
TaSiOx
Source
Drain
Gate
n+-InGaAs : 20 nm
InP etch stop : 6 nm
In0.52Al0.48As : 3 nm
Si δ doping
In0.52Al0.48As : 3 nm
InP layer : 2 nm
In0.7Ga0.3As QW channel : 10 nm
In0.52Al0.48As bottom barrier : 100 nm
InxAl1-xAs buffer (x=0-0.52) : 0.7 μm
(overshoot of In (0.52...0.7))
GaAs nucleation
and buffer layer : 0.7μm
4º(100) Offcut Si substrate
(b)
In0.53Ga0.47As cap
InP etch stop
In0.53Al0.48As
spacer/barrier
InP barrier layer
In0.7Ga0.3As QW
In0.53Al0.48As
bottom barrier
10nm

Fig. 4.

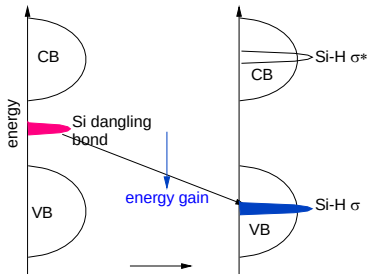

Fig. 5.

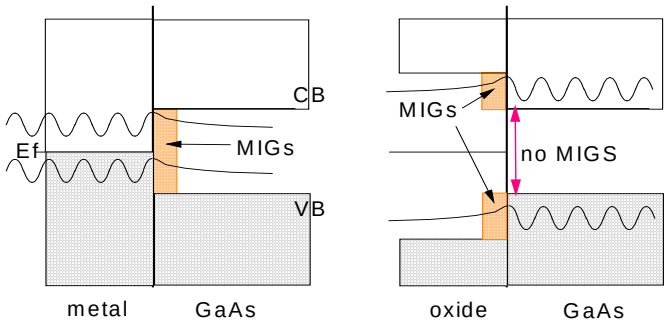

fig. 6

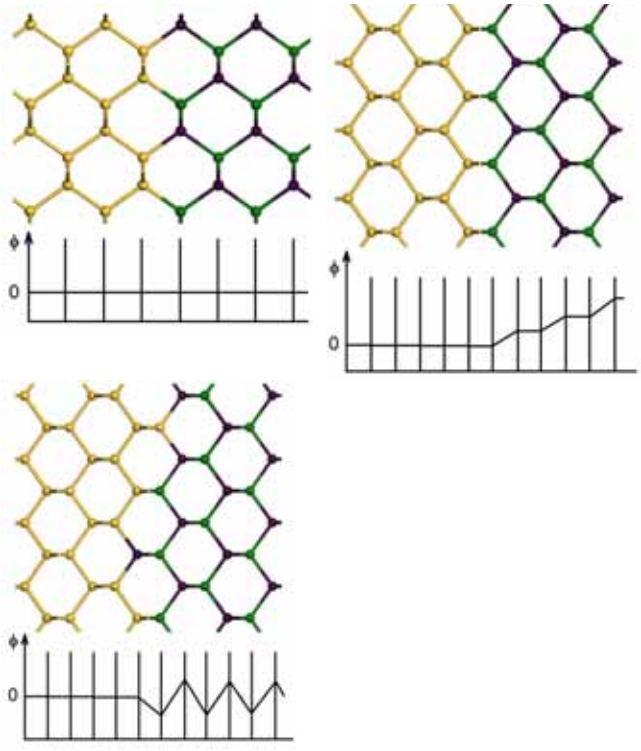

Fig. 7

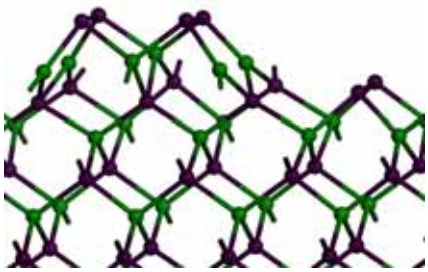

Fig. 8.

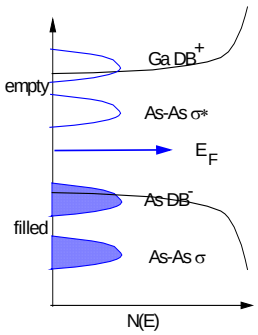

Fig. 9.

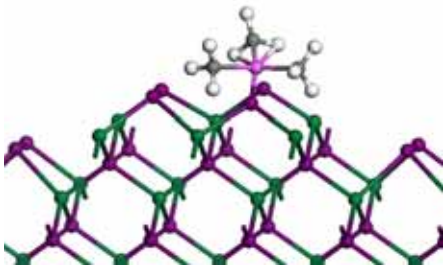

Fig. 10.

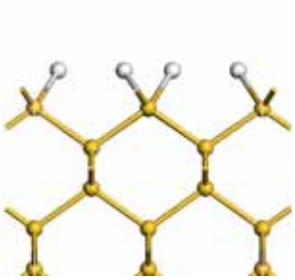

Fig. 11.

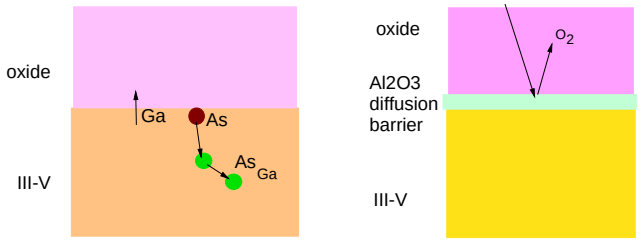

Fig. 12.

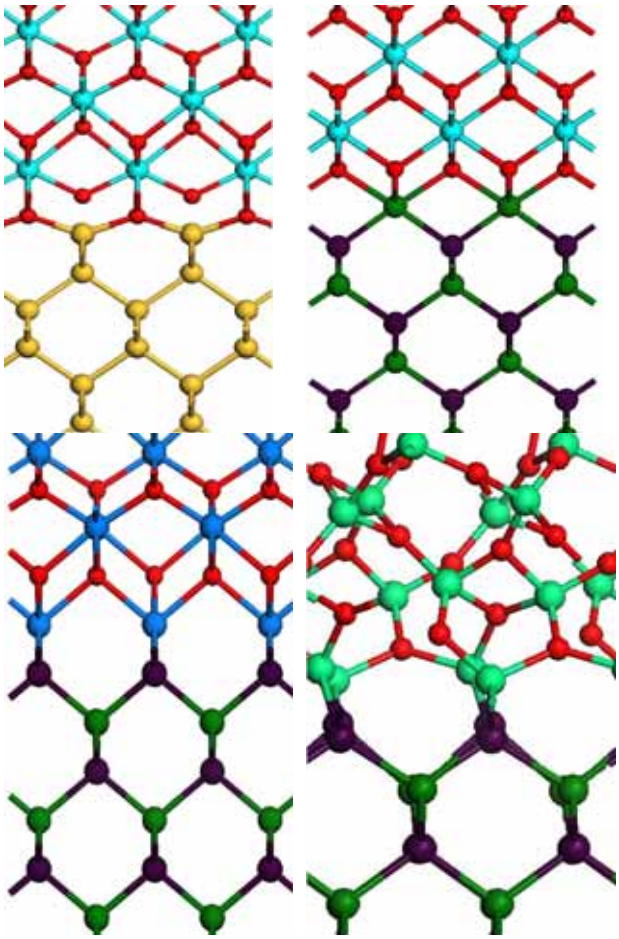

Fig. 13.

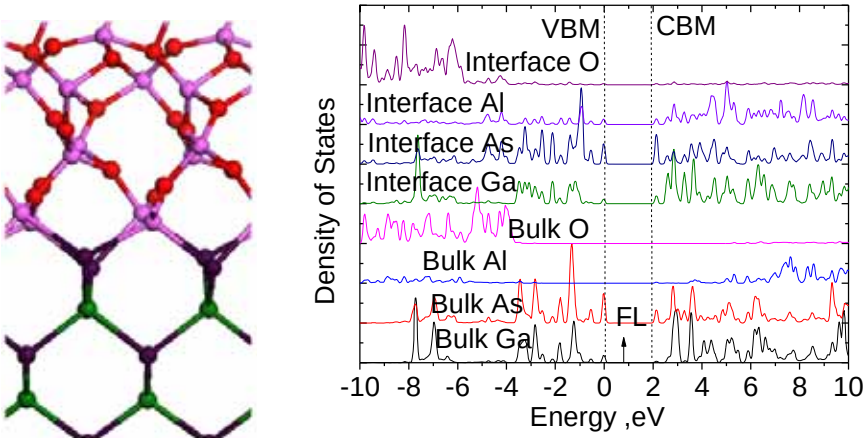
VBM
CBM
Interface O
Interface Al
Interface As
Interface Ga
Bulk O
Bulk Al
Bulk As
Bulk Ga
FL
Density of States
-10 -8 -6 -4 -2 0 2 4 6 8 10
Energy ,eV

Fig. 14.

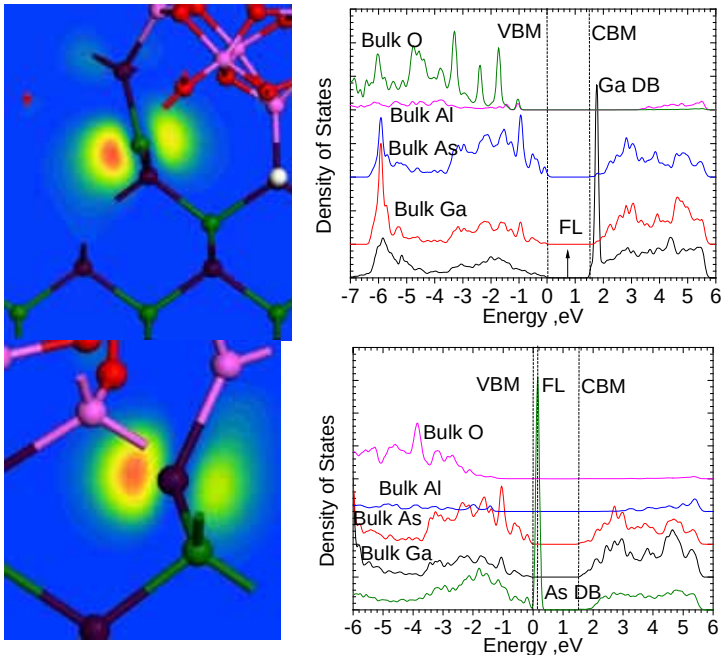
Bulk O
VBM
CBM
Ga DB
Bulk Al
Bulk As
Bulk Ga
FL
Density of States
-7 -6 -5 -4 -3 -2 -1 0 1 2 3 4 5 6
Energy ,eV
VBM
FL
CBM
Bulk O
Bulk Al
Bulk As
Bulk Ga
As DB
Density of States
-6 -5 -4 -3 -2 -1 0 1 2 3 4 5 6
Energy ,eV

Fig. 15.

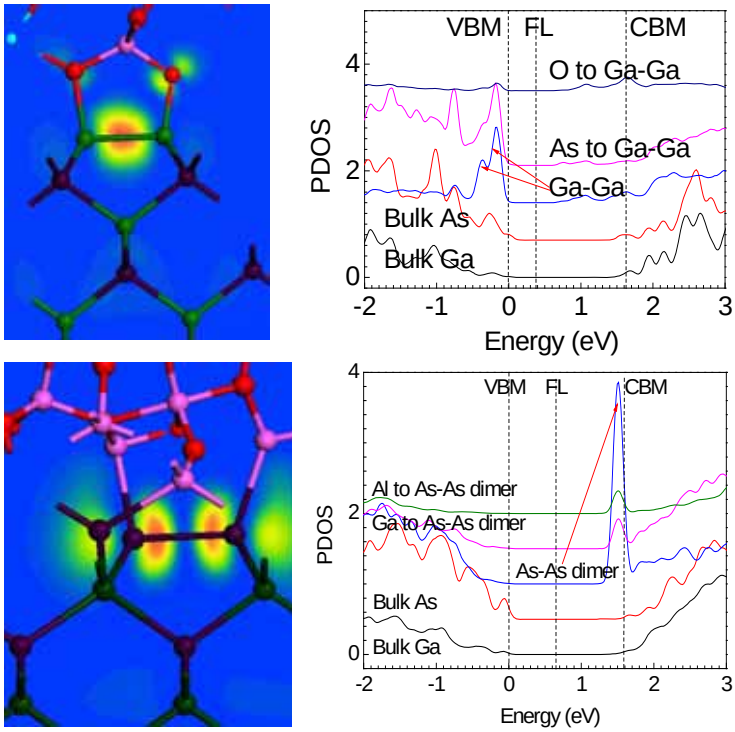
VBM
FL
CBM
O to Ga-Ga
As to Ga-Ga
Ga-Ga
Bulk As
Bulk Ga
PDOS
Energy (eV)
Al to As-As dimer
Ga to As-As dimer
As-As dimer
Bulk As
Bulk Ga

Fig 16.

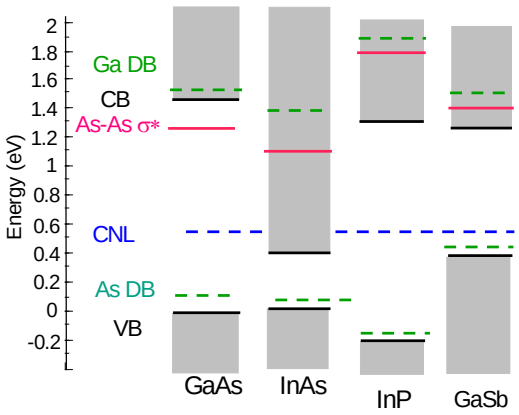
Energy (eV)
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
Ga DB
CB
As-As σ*
CNL
As DB
VB
GaAs
InAs
InP
GaSb

Fig. 17

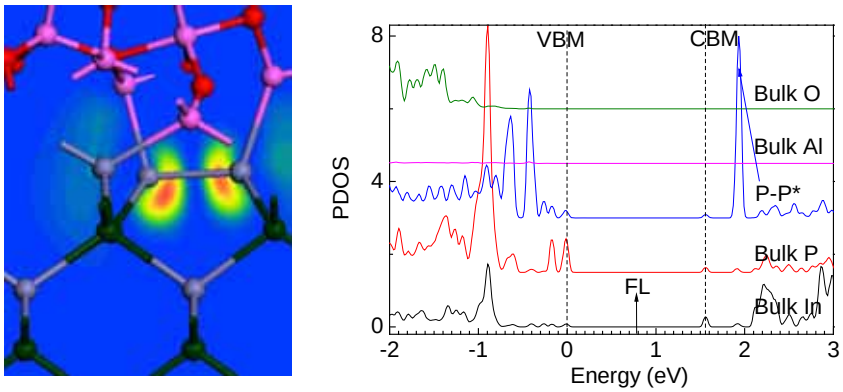
8
4
0
PDOS
VBM
CBM
Bulk O
Bulk Al
P-P*
Bulk P
FL
Bulk In
-2
-1
0
1
2
3
Energy (eV)

Fig. 18.

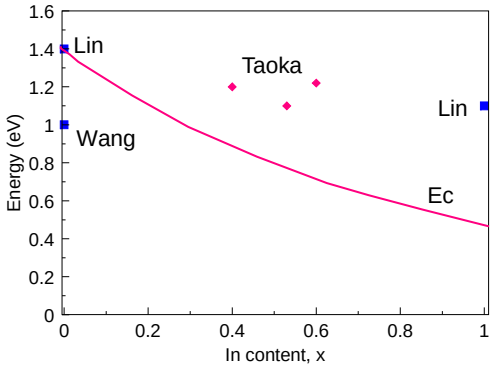
Lin
Taoka
Lin
Wang
Ec
Energy (eV)
In content, x
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
0.2
0.4
0.6
0.8
1

Fig. 19

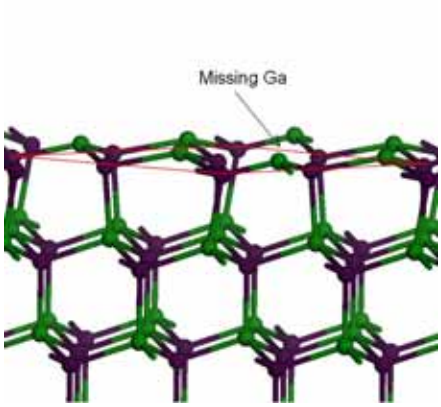

Fig. 20

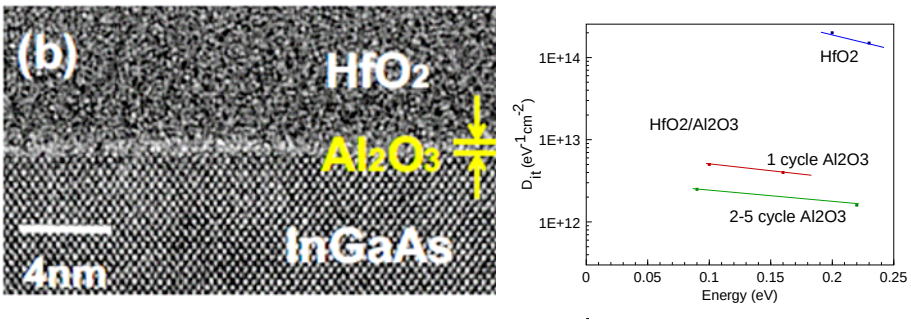
(b)
HfO2
Al2O3
InGaAs
4nm
HfO2
HfO2/Al2O3
1 cycle Al2O3
2-5 cycle Al2O3
1E+14
1E+13
1E+12
0
0.05
0.1
0.15
0.2
0.25
Energy (eV)

Fig. 21

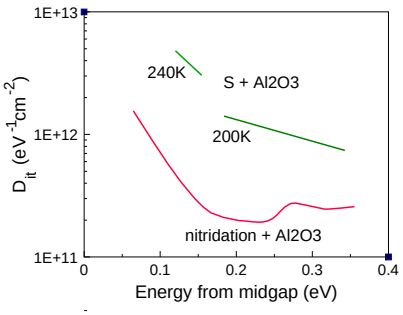
1E+13
1E+12
1E+11
D_{it} ($eV^{-1}cm^{-2}$)
240K
S + Al2O3
200K
nitridation + Al2O3
0
0.1
0.2
0.3
0.4
Energy from midgap (eV)

Fig. 22.

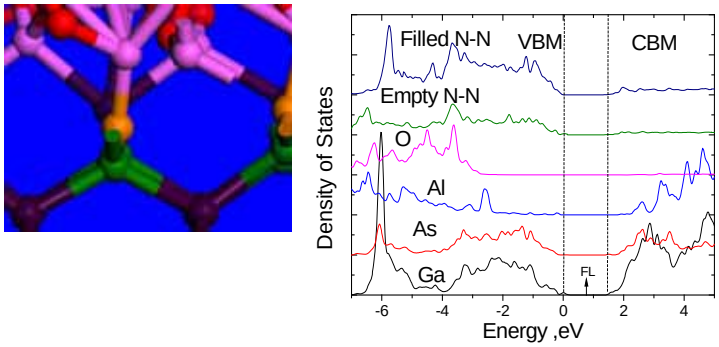
Filled N-N
VBM
CBM
Empty N-N
O
Al
As
Ga
FL
Density of States
-6
-4
-2
0
2
4
Energy ,eV

Fig. 23.