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Elucidating contact-limited temperature dependence of charge transport in 2D tin halide perovskite field-effect transistors

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Abstract

Two-dimensional (2D) tin halide perovskites are gaining attention for their potential in high-performance field-effect transistors (FETs) due to their ease of processibility and high mobility. However, their complex charge transport mechanism remains poorly understood with no definitive transport models established. While temperature-dependent mobility analysis is a proven method for constructing accurate charge transport models in a given material system, systematic temperature dependence studies in prototypical 2D tin perovskites, PEA_2SnI_4, have been rarely reported. Here, we investigate the temperature-dependent transport properties of PEA_2SnI_4 in FETs, employing contact resistance analyses to decouple intrinsic channel mobility from contact resistance contributions. Our results reveal that the extracted mobility values are significantly contact-limited, particularly at lower temperatures, leading to substantial deviations in apparent mobility trends. By correcting for contact resistance, we establish that the intrinsic mobility of PEA_2SnI_4 remains nearly temperature-independent from 100 K to 300 K. Our results clearly address the critical need to account for contact effects in determining carrier mobility of perovskite materials within the community, offering a refined framework for accurately evaluating and enhancing the performance of perovskite-based electronic devices.

1. Introduction

Metal halide perovskites (MHPs) have emerged as a pivotal class of materials in optoelectronic research due to their exceptional properties, including high charge carrier mobility [1], tunable bandgaps [2], and long carrier diffusion lengths [3]. These characteristics position MHPs as strong candidates for applications such as light-emitting diodes, photovoltaic cells. Benefiting from their low effective mass [4] and defect tolerance property [5], perovskites are attracting significant interest for thermoelectric [6] and field-effect transistor (FET) applications [7–10]. Amid this growing attention, Ruddlesden–Popper (RP) perovskites, with their layered two-dimensional (2D) structures, exhibit unique electrical and physical properties [11–15], offering distinct advantages for advanced electronic devices. These advantages have spurred interest in exploring specific 2D RP perovskites for high-performance applications [16, 17].

Among these, tin-based 2D RP perovskites, particularly PEA_2SnI_4, have attracted significant attention for their superior charge transport properties and enhanced stability under operational conditions. For instance, Matsushima *et al* reported a high carrier mobility of up to 12 $cm^2\ V^{-1}{\cdot}s^{-1}$ in PEA_2SnI_4 thin-film transistors (TFTs) fabricated on NH_3I self-assembled monolayer-treated substrates [18]. More recently, Zhu *et al* introduced an optimised fabrication approach by adjusting the molar ratios of PEAI, SnI_2, and the solvent

mixture (DMF:DMSO). This method resulted in grain boundary passivation via excess PEAI, as confirmed using conductive atomic force microscopy (AFM), leading to an improvement in transistor mobility from 0.7 to 3.5 $cm^2\ V^{-1}{\cdot}s^{-1}$ While these advancements underscore the potential of PEA_2SnI_4 for high-performance applications, they also highlight the need to better understand the underlying complex mechanisms governing the charge transport involving elusive roles of dynamic and energetic disorder in the system that have not been resolved for metal-halide perovskites [19].

A critical challenge lies in unravelling these charge transport mechanisms in 2D RP perovskites. Charge carrier mobility, a key parameter for FET performance, is influenced by various intrinsic processes in the channel such as ion migration [20, 21] and self-doping [22, 23], as well as extrinsic factors arising from the device such as contact effect [24]. While significant progress has been made in characterising optical and structural properties, the interplay between these factors in charge transport is poorly understood. Notably, contact resistance, often underestimated in perovskite FET studies, can distort mobility measurements, either underestimating or overestimating intrinsic material performance.

To address these challenges, this study investigates the interplay between the intrinsic charge transport properties and extrinsic contact resistance effects in PEA_2SnI_4 FET device observed in the temperature-dependent FET characteristics. By employing temperature-dependent transport analysis, the contact resistance analysis via transmission line method (TLM) and Gated-TLM analysis, we decouple the contact resistance effects from the intrinsic transport characteristics. This approach not only clarifies the impact of contact resistance on the mobility extraction in perovskite FETs, in general, but also provides a protocol for quantitatively characterising accurate carrier mobility values in metal-halide perovskite materials, critical for assessing and advancing perovskite-based electronic devices.

2. Method

2.1. FET substrate fabrication

300 nm thick SiO_2/Si p++ substrates were cleaned using an ultrasonic bath with acetone and isopropanol for 10 min each. After drying with a nitrogen (N_2) flow, the substrates were treated with oxygen (O_2) plasma for 10 min. The cleaned substrate were pre-patterned with FET channel patterns (Width: 1000 μm, Length: 200 μm) using a shadow metal mask. Metal electrodes were deposited by thermal evaporation. A 3 nm layer of chromium (Cr) was deposited at a rate of 0.1 Å s^{-1} as an adhesion layer between the SiO_2 substrate and the gold (Au) electrode. Subsequently, a 20 nm Au layer was deposited at a rate of 0.3 Å s^{-1}.

2.2. Preparation of perovskite solution and device fabrication

The perovskite solution was prepared by dissolving phenethylammonium iodide (PEAI, purchased from Greatcell Solar Materials) and tin(II) iodide (SnI_2, 99.99% trace metals basis, Merck) in a 4:1 mixed solvent of dimethylformamide (DMF, anhydrous, 99.8%, Sigma-Aldrich) and dimethyl sulfoxide (DMSO, anhydrous, $\geqslant$99.9%, Sigma-Aldrich) at a molar ratio of 2.3:1. The solution was stirred for 4 h at 60 °C. FET substrates were cleaned using an ultrasonic bath with acetone and isopropanol for 10 min each. After drying with a nitrogen (N_2) flow, the substrates were treated with oxygen (O_2) plasma for 10 min. The prepared perovskite precursor was deposited on the FET substrate by spin coating at 4000 rpm for 30 s and annealed at 100 °C for 10 min in a glovebox.

2.3. Material characterizations

For device characterization, all FET measurements were conducted using a Keithley 4155C semiconductor parameter analyser under dark conditions at room temperature. The measurements were performed in a vacuum probe station, where the pressure was maintained using a turbo pump at approximately 10^{-6} Torr to ensure accurate device performance assessment. The sample temperature was controlled and measured by Lake Shore Cryotronics 331.

The x-ray diffraction spectra was obtained with D8 Advance, 2020 (multi-purpose XRD). The photoluminescence (PL) spectra of the PEA_2SnI_4 thin films were characterised using a spectrofluorometer (FP-8550ST, JASCO) with a 300 W Xenon arc lamp (excitation wavelength = 430 nm) and the absorption spectrum was obtained with a UV–Vis spectroscopy (V-770, JASCO). The AFM image and line profile was obtained by Park Systems (NX-10)

3. Results & discussion

In this study, we characterised the electrical properties of RP perovskite FETs fabricated in a bottom-contact (BC), bottom-gate geometry (figure 1(a)). BC devices simplify the electric field distribution, effectively eliminating charge transport in the out-of-plane direction. To further minimise device complications, we

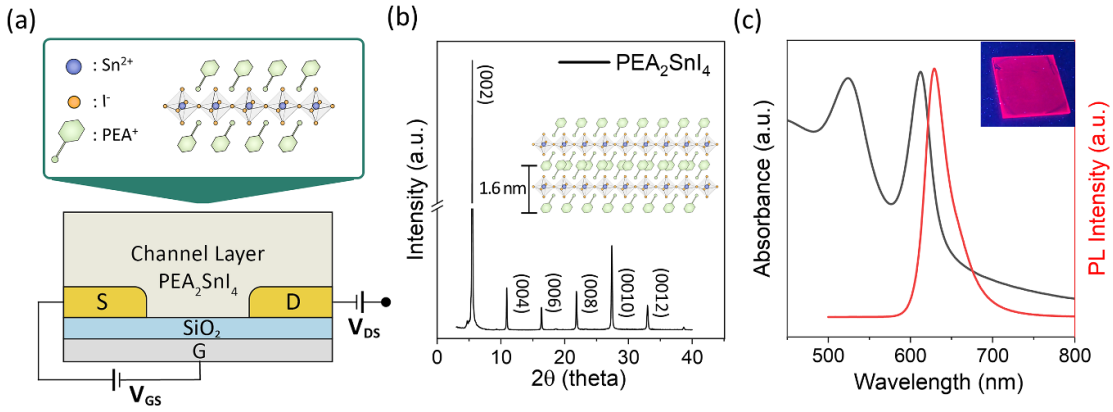

Figure 1. (a) Schematic of PEA_2SnI_4 perovskite transistor. (b) X-ray diffraction (XRD) data (c) UV–vis and photoluminescence data of PEA_2SnI_4 perovskite.

selected 2D PEA_2SnI_4 RP-type Sn based perovskite due to its low ion migration properties and high mobility [18, 19], which are known to adversely affect device stability and performance.

The structural properties of the PEA_2SnI_4 thin film were analysed to confirm the quality of the synthesis and the proper formation of the film. As shown in figure 1(b), the XRD patterns reveal a highly ordered organic—inorganic layered structure, characterised by a well-connected network of SnI_6 octahedra. The PEA_2SnI_4 film showed strong diffraction patterns at (0 0 L) ($L = 2, 4, 6, 8, 10$) indicating parallel aligned layer-by-layer structure. The interlayer spacing of the perovskite was measured to be approximately 1.6 nm according to Bragg's law.

Additionally, the signal of PEAI appears at a peak of 4.7° for the film, which is attributed to the presence of excess PEAI. This observation is consistent with findings reported in previous studies [19]. Furthermore, as shown in figure S1, the film thickness was analysed using AFM, which revealed a uniform thickness of approximately 62 nm.

Figure 1(c) presents the UV–vis absorption and PL spectra of the PEA_2SnI_4 thin film. The PL spectrum exhibited a pronounced peak at 620 nm, confirming strong excitonic emission in the visible range. When exposed to UV light, the films emitted a bright red luminescence, as shown in the inset image. Furthermore, the absorption edge in the UV–vis spectra suggested a bandgap of approximately 1.9 eV.

To explore the temperature-dependent charge transport mechanism, we measured FET device characteristics at various temperatures (from 290 K to 130 K) in a high-vacuum environment (10^{-6} Torr) to suppress external influences such as oxygen-induced p-type doping [25]. After a 2 h stabilization time, we observed a consistent device performance, ensuring reliability in our measurements (figure S2).

We first measured the I–V characteristics using a 2-terminal measurement (i.e. with gate electrode floating) (figure 2(a)) which showed a noticeable decrease in the conductivity from 0.039 S cm^{-1} at 290 K to 0.0076 S cm^{-1} at 130 K as the temperature decreased. As the temperature dropped below 190 K, the conductivity converged to a near-constant value, while a slight increase in the current was observed at higher voltages ($V_{DS} = 5$ V) between 130 K and 190 K.

The lower conductivity at lower temperatures can be attributed to a combination of transport parameters. Intrinsically, the conductivity, $\sigma = ne\mu$, where n is the carrier concentration, μ is the carrier mobility and e the electric charge, the reduction of n due to thermally activated free carrier generation in the channel may limit σ. Furthermore, reduced μ due to trap states [26] or inter-grain hopping transport [27, 28] at lower temperatures could also contribute to the overall decline in the conductivity.

Moreover, the non-linear behaviour in the I–V curves may arise due to the contact resistance, likely arising from a Schottky barrier at the metal/semiconductor interface, which becomes increasingly significant at lower temperatures as the available thermal energy decreases [29]. Together, these effects appear to drive the observed changes in conductivity. In addition to the previously noted trends, the I–V curves reveal non-linear behaviour as the temperature drops further below 190 K. This additional observation signals a transition from Ohmic conduction, where transport is dominated by free carriers in the channel, to thermionic emission, where charge injection across the Schottky barrier at the metal/channel interface governs the current flow in the channel. Therefore, this transition can be understood as a consequence of the interplay between the intrinsic transport properties related to n and μ, and the extrinsic impact of the contact resistance due to the Schottky barrier [16]. The presence of the Schottky barrier, implied by these observations, will be confirmed through additional analysis as discussed later.

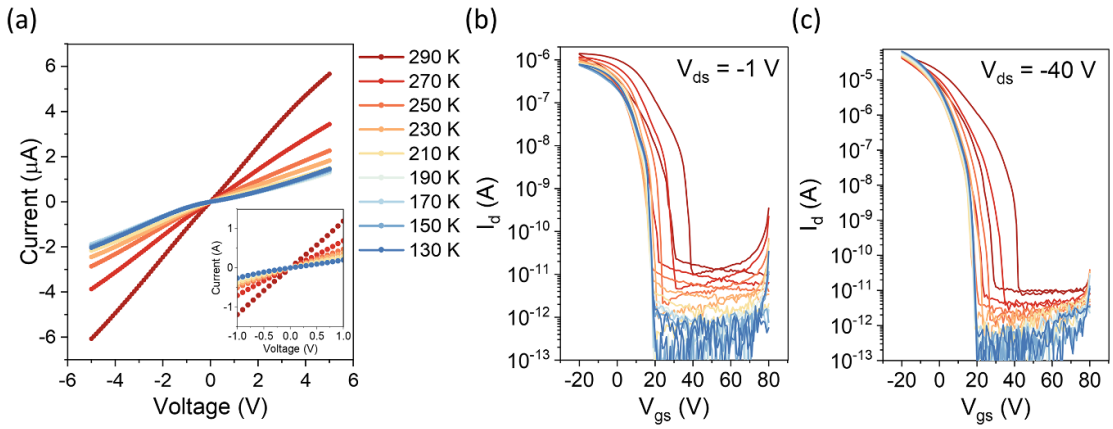

Figure 2. (a) Temperature-dependent *I–V* curve of PEA_2SnI_4 transistor measured with the gate terminal (V_{GS}) left floating. (b) Transfer characteristics in the linear region. (c) Transfer characteristics in the saturation region of the PEA_2SnI_4 TFTs.

To gain deeper insights into the transport properties of PEA_2SnI_4, FET characteristics were measured over the temperature range to explore the temperature dependence of FET mobility. The transfer curves were extracted in both the linear (figure 2(b)) and saturation regimes (figure 2(c)) with the two operational regimes divided according to the measured output curves (figure S3).

The transfer curves in the linear regime (figure 2(b)) showed clear on/off behaviour, with the on/off ratio improving from 10^5 at 290 K to 10^6 at 130 K. This improved on/off ratio agrees with the lower 2-terminal conductivity measured at lower temperatures as shown in figure 2(a).

Below 190 K, the on-current in the linear regime slightly decreased, and hysteresis effects were noticeably reduced, indicating more stabilized device operation at lower temperatures. This could be attributed to a reduction in ion migration effects along the vertical direction under low-temperature conditions [30]. Additionally, pulsed-gate measurements confirmed a further suppression of hysteresis with a negative V_{th} shift (figure S4), which can be attributed to the halide migration effect that induces gate field screening [31]. In the saturation regime (figure 2(c)), the device exhibited characteristics like those observed in the linear regime. However, a key difference is that the on-current, which increased as the temperature decreased. This trend may be attributed to the Joule heating effect, which induces a localised temperature gradient at high gate bias, thereby increasing current flow[32].

The transfer curves in the two different regimes show some similar behaviours as temperature decreases. Firstly, the subthreshold swing value decreases from 1.6 V dec^{-1} (1.2 V dec^{-1}) at 290 K to 0.9 V dec^{-1} (0.7 V dec^{-1}) at 100 K for linear (saturation) regime. Secondly, both the transfer curves in the linear and saturation regimes show a shift in the threshold voltage, V_{TH}, towards the negative gate voltage (V_{GS}). This can be corresponded to the varying intrinsic carrier concentration in the PEA_2SnI_4 channel (i.e. lower V_{TH} for lower temperature) and therefore the surface charge density at the channel/dielectric interface [33, 34].

From the transfer curves in figure 2(b) FET mobility values can be extracted at the different V_{GS} for different temperatures, according to the gradual channel approximation formalism, with the expression for linear FET mobility, $\mu_{lin} = \frac{L}{WC_iV_{DS}}\left(\frac{\partial I_{DS}}{\partial V_{GS}}\right)$ [35, 36]. Here, L and W are the length and width of the accumulation channel, C_i is the gate-channel capacitance per unit area, applicable at $|V_{GS} - V_{TH}| \gg |V_{DS}|$ ($V_{DS} = -1$ V). As shown in figure 3(a), it is evident that the linear mobility of PEA_2SnI_4 decreases with decreasing temperature from the peak value of 0.93 $cm^2\ V^{-1}{\cdot}s^{-1}$ at 290 K to the peak value of 0.59 $cm^2\ V^{-1}{\cdot}s^{-1}$ at 100 K (1.6-fold decrease). In contrast, as shown in figure 3(b) the saturation FET mobility given by $\mu_{sat} = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{|I_{DS}|}}{\partial V_{GS}}\right)^2$ which is applicable at $|V_{GS} - V_{TH}| < |V_{DS}|$, exhibits a notable increase, characterised by a much steeper increase as the temperature decreases; 1.28 $cm^2\ V^{-1}{\cdot}s^{-1}$ at 290 K to the peak value of 3.35 $cm^2\ V^{-1}{\cdot}s^{-1}$ at 100 K (2.6-fold increase) (figure S5). We neglected data above 300 K due to significant device degradation observed in the channel possibly due to the volatile nature of organic halide (figure S6) [37].

The combined analysis of the temperature dependence of the mobility plot, as shown in figure 3(c), reveals a noticeable divergence between the mobility trends extracted in the two different regimes with decreasing temperature. Specifically, while the linear mobility is suppressed at lower temperatures, the saturation mobility is enhanced. This intriguing coexistence of opposing temperature dependencies within a single system highlights the role of a significant extrinsic factor that may obscure the intrinsic transport

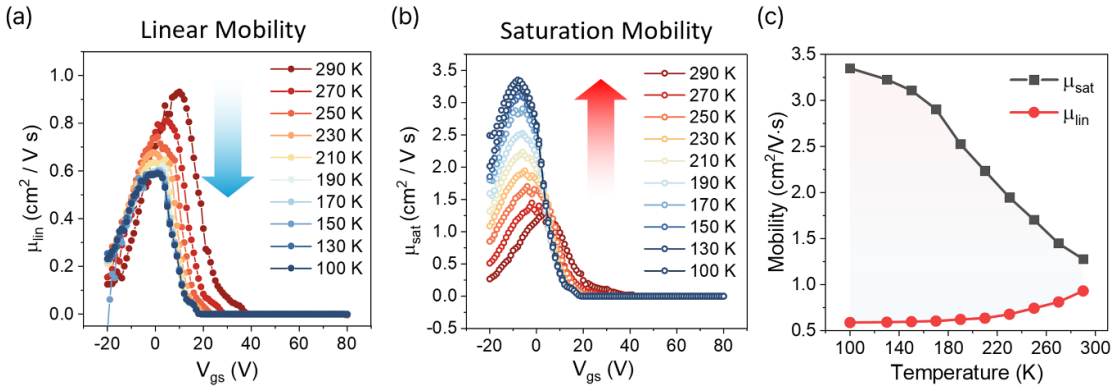

Figure 3. Temperature dependent mobility of PEA_2SnI_4 perovskite extracted at (a) linear, (b) saturation region. (c) Comparison of linear and saturation mobility by different temperature.

properties of PEA_2SnI_4 FETs. Notably, as shown in figure S7, the linear mobility follows an Arrhenius-like behaviour, yielding an activation energy of 24.3 meV, indicating a thermally activated transport mechanism. In contrast, the saturation mobility exhibits band-like transport behaviour, following a power-law decay of $\mu \propto T^{-1.54}$, consistent with its temperature-dependent trend [38]. Considering these clearly contrasting mechanism, it is more plausible that the observed discrepancy arises from an extrinsic origin rather than intrinsic properties of the PEA_2SnI_4 channel.

A key extrinsic factor likely contributing to these behaviours is the influence of contact resistance at the interface between the PEA_2SnI_4 channel and the Au metal electrodes [39]. This contact resistance would significantly impact charge injection properties and play a crucial role in shaping the temperature dependence of both linear and saturation mobility. In the linear regime, contact resistance becomes particularly prominent but is often overlooked in traditional mobility calculations, leading to potential inaccuracies in the extracted values [39, 40]. This oversight can lead to significant inaccuracies, particularly when the contact resistance is large or strongly gate-dependent. To address this, a refined formula that accounts for both channel resistance (R_{Ch}) and contact resistance (R_C) can be expressed as the following:

$$\mu_{Lin} = \frac{L}{WC_i(R_{Ch}+R_C)^2}\left(\frac{\partial R_{Ch}}{\partial V_{GS}} + \frac{\partial R_C}{\partial V_{GS}}\right). \tag{1}$$

Based on this formula, when R_C becomes comparable to R_{Ch}, mobility can be significantly underestimated. Conversely, if the contact resistance exhibits a strong gate dependence, it can lead to overestimation of mobility [41]. This gate-dependent contact resistance effect has been reported to induce a mobility peak followed by a sharp decline, a behaviour that is clearly observed in both figures 3(a) and (b).

Additionally in the saturation regime, i.e. a high V_{DS} regime, the inaccuracies can become even more pronounced. During the transfer scan, the applied gate field modulates the depletion region (pinch off) width, facilitating carrier emission or tunnelling across the Schottky barrier. This modulation of the injection barrier by the gate field results in significant gate-dependent variations in the contact resistance, where an increase in $\frac{\partial R_C}{\partial V_{GS}}$ can substantially influence the calculated mobility. Previous studies have noted that strong gate dependence in contact resistance within the saturation regime can distort the apparent mobility, potentially leading to significant overestimation of the extracted values [40, 41].

Given the significant impact of the contact resistance on device performance across both linear and saturation regimes, a comprehensive analysis of the carrier injection behaviour is essential. To address this, we analysed the carrier injection properties by assuming the PEA_2SnI_4 channel/Au contact with Schottky-Barrier FET model. The Schottky barrier height between the injection electrode and the perovskite channel was determined using the thermionic emission equation as follows [42, 43]:

$$I_{DS} = AA^{\star}T^{1.5}e^{-\frac{q\phi_{B0}}{k_BT}}\left(1-e^{-\frac{qV_{DS}}{k_BT}}\right) \tag{2}$$

where I_d represents the drain current, A is the contact area, $A^{\star}$ is the Richardson constant, q is the elementary charge, ϕ_{B0} is the barrier height, k_B is Boltzmann's constant, and T is the temperature. For $qV_{DS} \gg k_BT$, the equation simplifies to:

$$J = A^{\star}T^{1.5}\exp\left[-\frac{q\phi_{B0}}{k_BT}\right]. \tag{3}$$

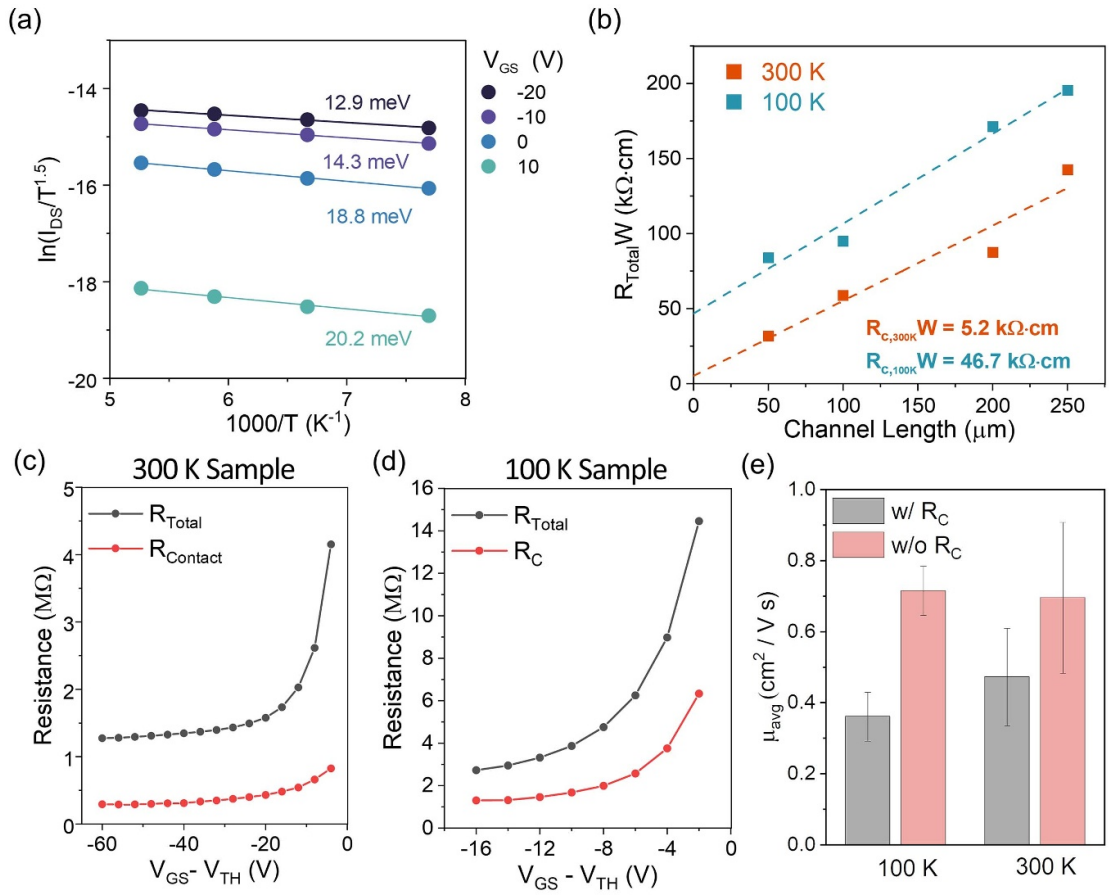

Figure 4. (a) Arrhenius plot of the Au/PEA_2SnI_4 contact under varying gate voltages, demonstrating thermionic emission behaviour and gate-dependent activation energy. (b) Contact resistance (R_C) as a function of temperature, extracted using the transmission line method (TLM). (c), (d) Gate-dependent contact resistance (R_C) analysed at different temperatures using the gated-TLM, which was calculated based on the same geometry as the previously measured FET. (e) Intrinsic mobility data at 100 K and 300 K corrected for contact resistance.

This simplified equation was applied to fit the Arrhenius plot (figure 4(a)), confirming that carrier injection in PEA_2SnI_4 follows a thermionic emission mechanism rather than ohmic contact (as shown in figure 2(a)). These results suggest the formation of a Schottky barrier at the Au contact, supported by the temperature-dependent drain current behaviour and the thermionic emission model. At lower temperatures, the dominance of thermionic emission over the Schottky barrier leads to an increase in contact resistance, particularly in the ON region of the FET where efficient charge injection is critical.

In addition to these observations, the effect of the contact resistance in the device characteristics was quantitatively treated by directly measuring the contact resistance values at 300 K and 100 K using TLM (figure 4(b)). FET devices with 4 different channel lengths (50 μm, 100 μm, 200 μm, 250 μm) were fabricated and the conductivity of each sample was measured. The results revealed that the contact resistance increased by approximately one order of magnitude, from 5.2 kΩ cm to 46.7 kΩ cm, as the temperature decreased from 300 K to 100 K. This observation, which is consistent with the Arrhenius analysis (figure 4(a)), indicates that the significant increase in the contact resistance at lower temperatures stems from a reduced thermionic emission across the Schottky barrier.

Building on previous findings that demonstrate the significant effects of contact resistance on device operation due to the Schottky barrier, gated-TLM measurements were conducted to further investigate the temperature and gate-dependent influence of contact effects on perovskite device performance.

As shown in figures 4(c) and (d), at 300 K, the proportion of the contact resistance relative to channel resistance were relatively small (∼30%), indicating that the channel resistance dominated the total resistance ($R_{Ch} = 980\ k\Omega$ and $R_C = 290\ k\Omega$, respectively). However, at 100 K, the contribution of contact resistance increased significantly, approaching a comparable ratio with the channel resistance (∼30% to ∼90%). This demonstrates that at lower temperatures, the impact of contact resistance becomes much more pronounced, becoming a critical component in the overall resistance of the device.

In addition to these temperature-dependent contact resistance measurements, channel-length-dependent FET characterization was conducted with a range of width-to-length (W/L) ratios (e.g. 5, 10, 25, and 50). FETs with shorter channel lengths exhibit a pronounced decrease in the extracted mobility (figure S8). This behaviour is attributed to the contact resistance (R_C) increasingly dominant as the channel length is reduced. This observation is consistent with predictions from mobility model that incorporates R_C.

The above quantitative results render themselves to an important question of how much the FET mobility values extracted can represent the intrinsic carrier mobility values of PEA_2SnI_4 channel. For this, we attempted to compare the mobility values before and after the correction for the contact resistance, as measured by gated-TLM from figures 4(c) and (d). Using the gated-TLM analysis for different gate voltages values like the data shown in figure 4(b), we extracted the contact resistance for the specific gate voltage values for the devices with the channel lengths 50, 100, 200 and 250 μm.

As seen in figure 4(e), the effective channel mobility at 100 K and 300 K exhibited a minimal difference, both maintaining the value of approximately 0.7 $cm^2\ V^{-1}{\cdot}s^{-1}$, which is notably higher than the mobility value extracted from the linear regime. This finding implies that the observed reduction of the extracted mobility in the linear regime or increase in the saturation regime at lower temperatures is primarily due to the increased contact resistance, rather than reflecting the actual temperature dependence of the intrinsic mobility of PEA_2SnI_4.

Therefore, these findings reveal that the intrinsic mobility of PEA_2SnI_4 FETs may not decrease with lowering temperature, contrary to the apparent trends influenced by the contact resistance (figure 3(c)). Importantly, this study demonstrates that neglecting the influence of the contact resistance in mobility calculations can lead to significant deviations from intrinsic behaviour, resulting in misinterpretation of the temperature-dependent mobility trends.

Beyond PEA_2SnI_4, our results provide a critical foundation for understanding charge transport physics in 2D perovskite materials and other perovskite materials. By highlighting the necessity of accounting for the contact resistance effects, this work offers valuable guidance for refining charge transport models for which experimental results for temperature dependence of mobility can provide a crucial dataset and enhancing the device performance of perovskite-based electronic devices that are expected to be severely contact-limited.

4. Conclusion

This study provides a comprehensive analysis of the temperature-dependent charge transport in 2D RP tin-halide perovskite, PEA_2SnI_4, FETs, with a focus on disentangling intrinsic mobility from extrinsic contact resistance effects. By employing temperature-dependent TLM and gated-TLM analyses, we demonstrated that contact resistance at the Au/PEA_2SnI_4 interface plays a dominant role in shaping the mobility trends observed in both linear and saturation regimes. Our findings reveal that the intrinsic mobility of PEA_2SnI_4 remains largely independent of temperature, in stark contrast to the significant deviations caused by contact resistance, particularly at lower temperatures. The results emphasise the need for a careful treatment of the contact resistance in mobility extraction to avoid misinterpretation of intrinsic charge transport properties. This work provides critical insights into construction of accurate charge transport models of perovskite materials that can be extended beyond PEA_2SnI_4 or 2D perovskites, and the refined methodologies and findings presented here offer valuable guidance for the design and evaluation of perovskite-based electronic devices, paving the way for their reliable implementation in next-generation electronics.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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