Device-Circuit Interactions and Impact on TFT Circuit-System Design

Xiang Cheng, *Student Member, IEEE,* Sungsik Lee, *Member, IEEE,* Reza Chaji, *Member, IEEE,* and Arokia Nathan, *Fellow, IEEE*

***Abstract*—This paper reviews the importance of device-circuit interactions (DCI) and its consideration when designing thin film transistor circuits and systems. We examine temperature- and process-induced variations and propose a way to evaluate the maximum achievable intrinsic performance of the TFT. This is aimed at determining when DCI becomes crucial for a specific application. Compensation methods are then reviewed to show examples of how DCI is considered in the design of AMOLED displays. Other designs such as analog front-end and image sensors are also discussed, where alternate circuits should be designed to overcome the limitations of the intrinsic device properties.**

***Index Terms*—Small signal model, s parameter, TFT, cutoff frequency, V_T shift**

I. Introduction

Although the ever-evolving TFT technology continues to produce devices with improved performance, such as higher mobility, steeper subthreshold slop and lower V_T [1]–[9], circuit implementation is still somewhat constrained. This applies for most of the material families including metal-oxides, organics, and amorphous silicon (a-Si:H) although much less so with low temperature poly-silicon (LTPS). Here, a key design consideration is the device-circuit interaction (DCI), which has to be accounted for when circuits are designed with devices of poor performance and high degree of non-ideality [10]–[19] as compared to the CMOS counterpart. This is particularly true when the intrinsic performance of TFTs does not the meet the requirements of a desired application. As shown in Fig. 1, if the performance of the desired application is much lower than the maximum achievable intrinsic performance of the TFT, it is then possible to design the circuit independently without considering device non-idealities. For example, when the error in the TFT's output current created by V_T shift is much lower than the required accuracy, the V_T shift problem is not of concern. However, when the performance requirement needs to be higher than the intrinsic performance, the designer should seek a compensation solution based on DCI or wait for improvements in the technology. We will discuss the intrinsic performance of TFTs in Section II along with compensation methods in Section III.

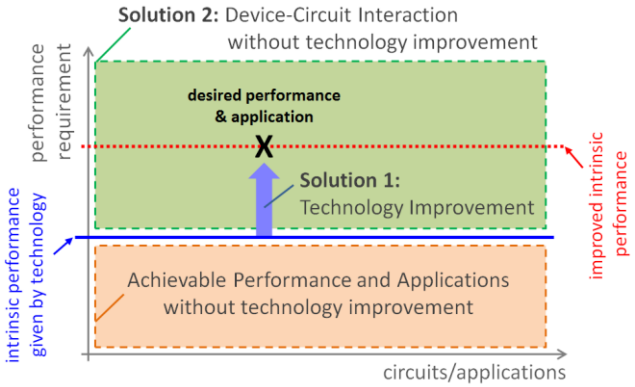

Fig. 1 Illustration of DCI in relation to performance requirements of a desired application

Another aspect of DCI stems from the material and processing attributes of the TFT which usually come with specific, and often self-limiting, properties. For example, in analog front-end and digital designs, alternative circuit architectures are needed to match the properties of the CMOS counterpart [20]–[24]. This will be discussed in Section IV along with

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X. Cheng, S. Lee, and A. Nathan are with the Electrical Engineering Division, Department of Engineering, University of Cambridge, Cambridge CB3 0FA, U.K. (e-mail: xc260@cam.ac.uk; sl684@cam.ac.uk; an299@eng.cam.ac.uk).

R. Chaji is with IGNIS Innovation Inc., Waterloo, ON, N2V 2C5 Canada(e-mail: rzchaji@gmail.com)

solutions to deal with, for example, light-induced non-ideality in oxide TFTs.

II. Impact of TFT properties

The TFT is the major building blocks of active thin film circuits and its properties determine circuit performance. In applications such as displays and analog front-end circuits, the accuracy of the output signal strongly affects the quality of the displayed image without mura (luminance non-uniformity) or in processing analog signal without significant error. The critical parameters for TFTs (e.g. mobility, C_{OX}, V_T, etc.) determine the performance of the circuit and are more often discussed when comparing TFT behavior or modelling a single transistor's terminal characteristics [12], [25]–[31]. However, other issues such as stability, temperature sensitivity and process variations can also limit the overall performance and may even affect the functionality of the circuit. There has been significant effort devoted to the study and modeling of bias induced V_T-shift [11], [15], [16] and V_T-shift compensation in AMOLED pixel circuits [32]–[35]. We will analyze the sensitivity of drain current on V_T-stability and temperature and process variations with the aim of establishing guidelines on the level of accuracy that can be achieved without applying compensation methods (i.e. the intrinsic performance) as well as identify the parameters that contribute most to error and how this can be improved with processing.

1) Temperature dependence

The parameters of the TFT are affected by material properties and on temperature, which in turn impacts the terminal current-voltage (I-V) behavior. According to the I-V model of the TFT:

$$I_{DS} \approx \frac{1}{2+\alpha_p}\frac{\mu_0^*}{Q_{ref}^{\alpha_p-1}}\frac{W}{L}C_{ox}^{\alpha_p}\left(V_{GS}-V_T\right)^{(\alpha_p+1)} \equiv K\times\left(V_{GS}-V_T\right)^{(\alpha_p+1)}, \quad (1)$$

where,

$$K \equiv \frac{1}{2+\alpha_p}\frac{\mu_0^*}{Q_{ref}^{\alpha_p}}\frac{W}{L}C_{ox}^{\alpha_p} \quad (2)$$

The variations can be specified as three key parameters: K, V_T and α_p. By considering these parameters as functions of temperature, the derivative of I_{DS} as a function of temperature can be expressed as follows:

$$dI_{DS}(T) = \left(V_{GS}-V_T\right)^{(\alpha_p+1)}\frac{\partial K}{\partial T}dT - K(\alpha_p+1)\left(V_{GS}-V_T\right)^{\alpha_p}\frac{\partial V_T}{\partial T}dT + K\ln\left(V_{GS}-V_T\right)\left(V_{GS}-V_T\right)^{(\alpha_p+1)}\frac{\partial \alpha_p}{\partial T}dT \quad (3)$$

Therefore the temperature sensitivity of the overall current can be separated into three parts, in which each part of the function is determined by the temperature sensitivity of K, V_T or α_p. The contribution of each parameter can then be calculated through extraction of the temperature sensitivity of the three parameters.

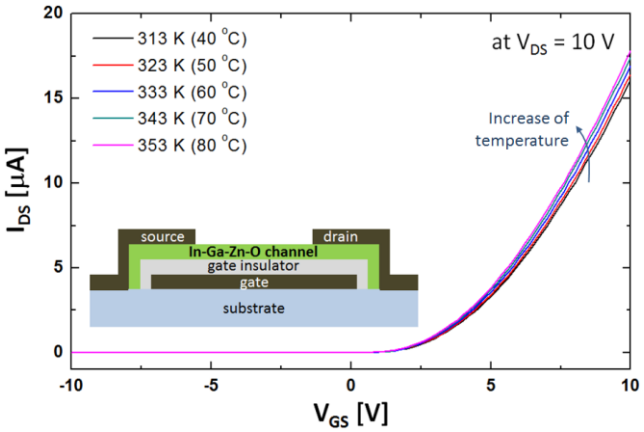

Fig. 2 I-V characteristics of the examined TFT under different temperatures.

Consider the transfer characteristic for an indium-gallium-zinc-oxide (IGZO) TFT, measured every 10°C from 40°C to 80°C, shown in Fig. 2. The results show that the overall current would increase when temperature increases. To further investigate the degree of influence of the three parameters, their values have been extracted from the measured transfer characteristics according to Eq. (1). Here, we extract the threshold voltage (V_T) independently from a multi-derivative method [36], and then use it to calibrate the gate voltage as $V_{GS} - V_T$. With this, I-V data is plotted in log-log plot. In this plot, all the data turns into a linear behavior, where the intercept on the y-axis, log(I_{DS}), is log(K), with slope α_p. From

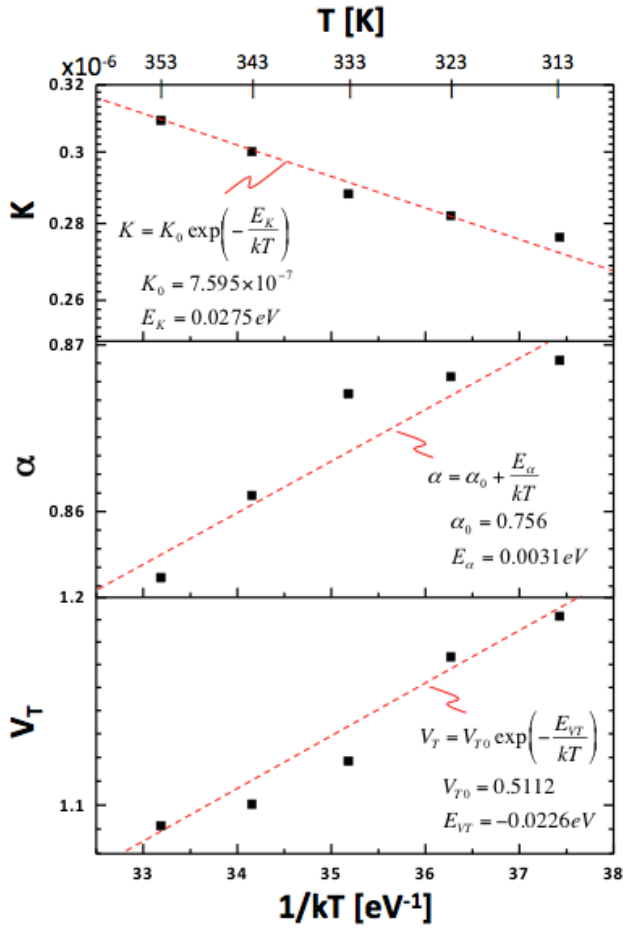

Fig. 3 Extracted values of K, α_p and V_T at the different temperatures.

this, we will get K and α_p independently. The results are shown in Fig. 3. As can be seen, all three parameters are approximately linearly related to 1/kT in the temperature range considered.

Therefore, through a linear fitting of the parameters, we get the empirical models of the parameters with the following relations:

$$\alpha_P(T) = \alpha_0 + \frac{E_\alpha}{kT} \tag{4}$$

$$K(T) = K_0 \exp(-\frac{E_K}{kT}) \tag{5}$$

$$V_T(T) = V_{T_0} \exp\left(-\frac{E_{VT}}{kT}\right) \tag{6}$$

Combining Eq. (4), (5), (6) and Eq. (3), the current sensitivity can be derived as:

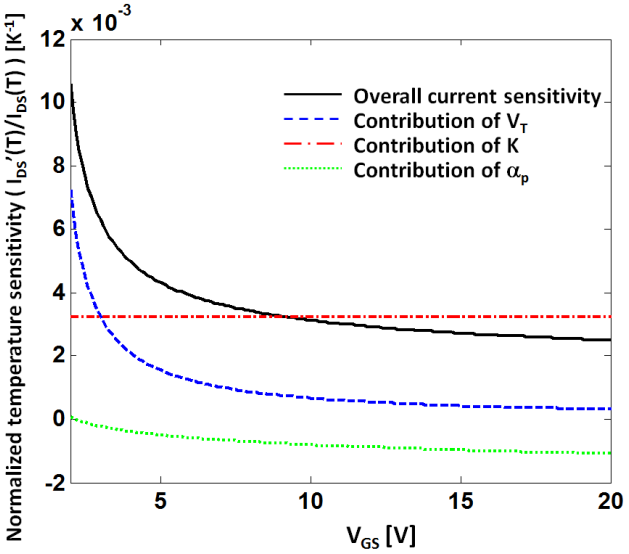

Fig. 4 Normalized temperature sensitivity of current and the contribution of different parameters at 313K.

$$\frac{dI_{DS}(T)}{dT} = (V_{GS} - V_T)^{(\alpha_p+1)} K_0 \frac{E_K}{kT^2} \exp(-E_K / kT)$$
$$- K(\alpha_p + 1)(V_{GS} - V_T)^{\alpha_p} V_{T_0} \frac{E_{VT}}{kT^2} \exp(-E_{VT} / kT) \tag{7}$$
$$- K \ln(V_{GS} - V_T)(V_{GS} - V_T)^{\alpha_p+1} \frac{E_\alpha}{kT^2}$$

Note that the three terms at the RHS of Eq. (7) define the contribution of K, V_T and α_p, respectively.

To understand how much the overall current is affected by ambient temperature and the associated contribution of the different parameters, the normalized temperature sensitivity is shown in Fig. 4. As can be seen, the overall temperature sensitivity drops with increase in V_{GS} due to the fact that the contribution of V_T drops while V_{GS} increases. This tendency starts to saturate when V_{GS} increases to 4V, when the contribution of K becomes dominant. This analysis suggests that TFTs can be very unstable when biased at a voltage near V_T. Although higher stability can be achieved through intentionally biasing the transistor at higher voltage levels, the maximum achievable level will be determined by the temperature sensitivity of K. As the temperature dependence of α_p has a negative contribution to current with respect to temperature and its contribution increases at higher bias, the temperature dependence of K can be compensated by α_p resulting in decreased sensitivity. However, a higher bias level

implies increased power consumption of the circuit. Therefore, an appropriate bias point should be chosen for enough stability with acceptable power consumption.

2) Geometric dependence

Apart from time- or temperature-dependent variations in device parameters, processing-induced spatial variations should be considered especially in pixelated arrays or analog circuit applications. These variations would cause pixel non-uniformity in displays or imagers and create error or undesired behavior in analog circuit design. Note that the non-uniformity can be global (i.e. between panels) or local (i.e. between transistors). The latter is harder to deal with especially when transistor matching is of concern (such as in differential pairs or current mirrors). This paper will focus on local non-uniformity and discuss the contribution of the different parameters in creating current mismatch.

Analysis of geometric dependence can follow a similar route as with temperature dependence. As different parameters would follow a certain probability distribution, the overall current will be determined by the randomness of all three parameters according to Eq. (1). As variations are usually smaller than the respective mean values, the mismatch in I_{DS} can be expressed as a first order approximation:

$$\begin{aligned}\Delta I_{DS} &= (V_{GS}-V_{T0})^{(\alpha_{p0}+1)}\Delta K \\ &\quad - K_0(\alpha_{p0}+1)(V_{GS}-V_{T0})^{\alpha_{p0}}\Delta V_T \\ &\quad + K_0\ln(V_{GS}-V_{T0})(V_{GS}-V_{T0})^{(\alpha_{p0}+1)}\Delta\alpha_p\end{aligned} \tag{8}$$

Here, K_0, V_{T0} and α_{p0} are the mean values of the parameters, and ΔK, ΔV_T and $\Delta\alpha_p$ their respective variations. Assuming K, α_p and V_T are independent variables and that all follow a normal distribution, the variance of I_{DS} can be expressed as:

$$\begin{aligned}\sigma^2{}_{I_{DS}} &= (V_{GS}-V_{T0})^{2(\alpha_{p0}+1)}\sigma^2{}_K \\ &\quad + K_0{}^2(\alpha_{p0}+1)^2(V_{GS}-V_{T0})^{2\alpha_{p0}}\sigma^2{}_{V_T} \\ &\quad + K_0{}^2[\ln(V_{GS}-V_{T0})]^2(V_{GS}-V_{T0})^{2(\alpha_{p0}+1)}\sigma^2{}_{\alpha_p}\end{aligned} \tag{9}$$

where σ_K, σ_{α_p} and σ_{V_T} are the standard deviation

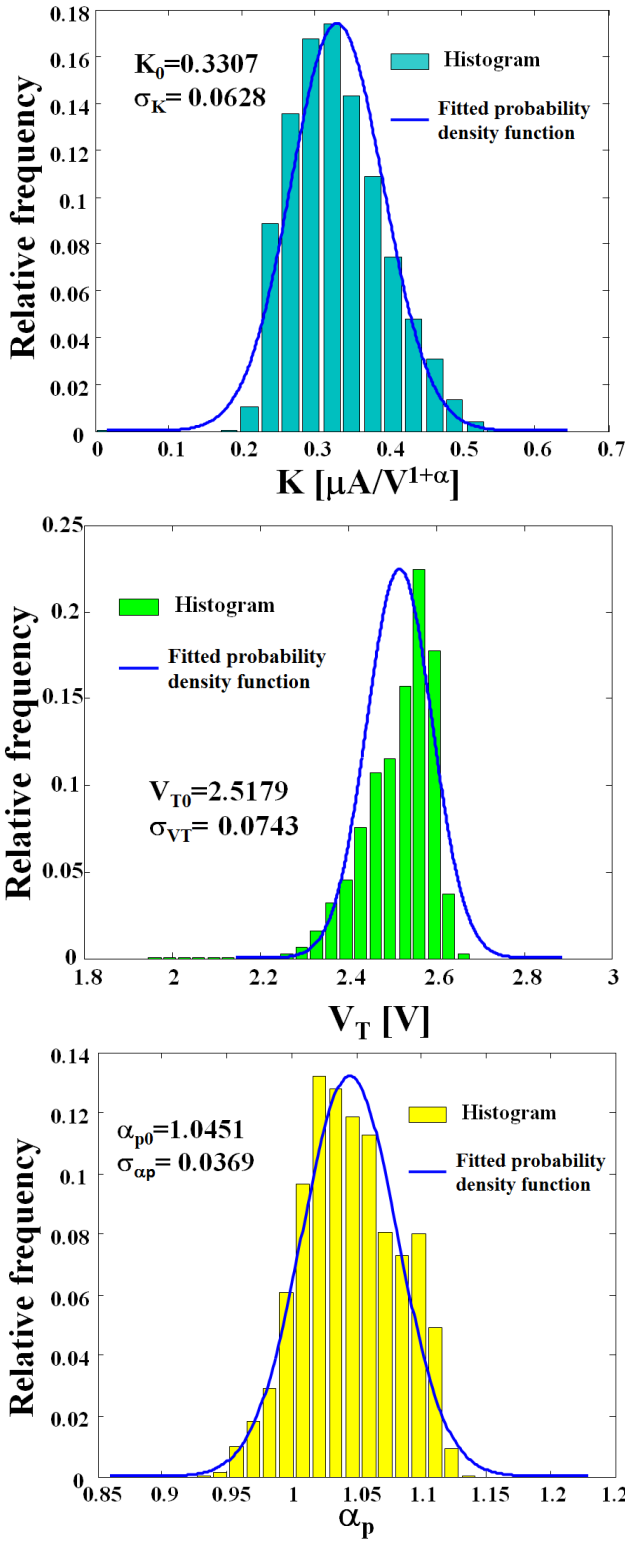

Fig. 5 Probability distribution and histogram of (a) K, (b) V_T and (c) α_p. The data was extracted at room temperature from a 1080*1920 RGBW AMOLED panel with pixel circuits as described in Fig. 7.

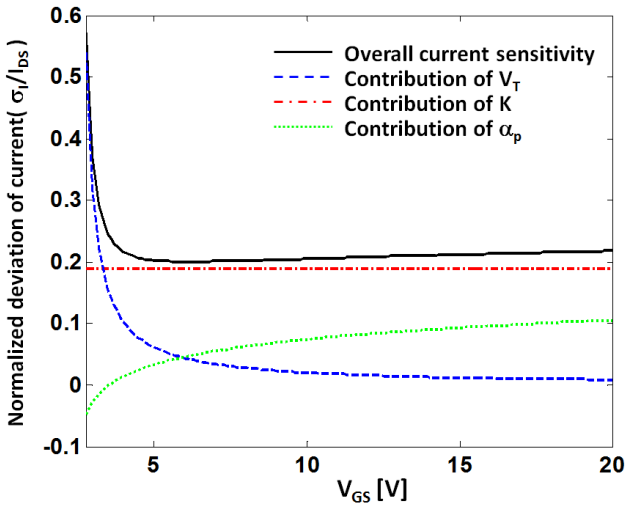

Fig. 6 Normalized standard deviation of current and the contribution of different parameters.

of K, α_p and V_T, respectively. As expected, the standard deviation of the overall current is determined by the deviation of all three parameters.

To analyze the variation sensitivity of the overall current, we need statistical data for all three parameters. Here, we acquired statistical data of the transfer characteristics by measuring a 1080*1920 RGBW OLED display panel. By using the pixel circuit described in [32], which will be reviewed in the next section, we could extract the I-V characteristics of the driver TFTs within the panel and extract statistical data for the three parameters. Here, the TFTs for driving the green OLED pixels are used as shown in Fig. 5. The probability density functions are fitted to a normal distribution using MATLAB. With the fitted mean values and standard deviations, we calculate the relative contributions of each parameter to the current variance using Eq. (9).

The standard deviation of I_{DS} and the contribution of each parameter are shown in Fig. 6. We see a similar overall curve in the sense that the sensitivity is higher when biased near V_T. However, unlike the temperature dependence where sensitivity drops with increasing bias, the dependence on geometric shows a minimum at around V_{GS}=6V. This is due to the decreasing contribution of V_T and the increasing contribution of α_p. Therefore, analog designers can intentionally choose a bias point close to the minimum point for the output transistor, when designing circuits to reduce the output current sensitivity to process variations.

The analysis of temperature and geometric dependence here is done using a generic approach since the current-voltage behavior is estimated by three key parameters, namely K, V_T and α_p. This is adaptable to most TFT types because of the similar working principle albeit with different parameter values. Therefore, the methodologies and derivations presented here are generic and empirically approached for applicability to other material families including OTFTs and related material families.

III. Compensation Methods in Circuits & Applications

The intrinsic performance of TFTs does not always meet the requirements of specific applications. For example, the threshold voltage shift in TFTs creates visible shadows or ghosting in displays or imagers after extended operation. The resulting non-uniformity creates mismatch in output characteristics especially in matrix architectures (displays or sensors). These kinds of defects have proven difficult to improve by processing, and thus need to be compensated through circuit solutions. Here, we will discuss V_T shift and non-uniformity compensation methods such as on-pixel programming and by off-pixel feedback. The compensation methods can also be extended to other circuit applications.

1) On pixel programming

The most common way of compensating TFT defects in active matrix arrays is through on-pixel compensation. The methods were first developed for a-Si:H TFTs in AMOLEDs as this family of TFTs have severe V_T shift under positive bias, which leads to big errors when supplying current to the OLED [37].

V_T compensation techniques can be categorized into two kinds: current programming [34], [38]–[44] and voltage programming [45]–[52]. The basic working principles of these have been reviewed in [37], [53]. Recent progress in voltage programming

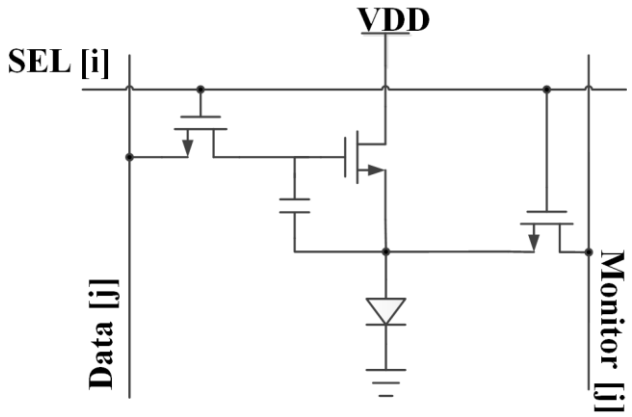

Fig. 7 AMOLED pixel structure for off-pixel defect extraction and feedback

has been reported in [35], [54]. Here, the working principle is slightly different from the original idea in that the technique does not capture the cut-off point of a diode-connected transistor. Instead, it uses a TFT to discharge a pre-charged capacitor with fixed gate bias in a fixed time period to capture the TFT's property (i.e. V_T). This technique can provide faster V_T extraction and is good particularly when the speed of the circuit is of concern.

2) Off pixel feedback

Another way of defect compensation is based on off pixel feedback. Since in display applications the driving period of each pixel can be separated into several phases, it is possible to use part of the driving sequence to extract all of the defect and aging data present in the pixel and then drive with revised extracted parameters as feedback [32], [55]–[60].

A pixel structure for defect extraction reported in [32] is shown in Fig. 7. The pixel circuit shows a similar structure as the simple 2T1C structure – the only difference being addition of a monitor line to monitor the TFT and OLED characteristics and extract their defect and aging status. The driving sequence for this pixel circuit is similar to the 2T1C except for the addition of a defect extraction phase. Defect extraction starts after the SEL signal selects the pixel and before writing data to it. The extraction phase consists of two parts – the driver TFT and the OLED, respectively (shown in Fig. 8).

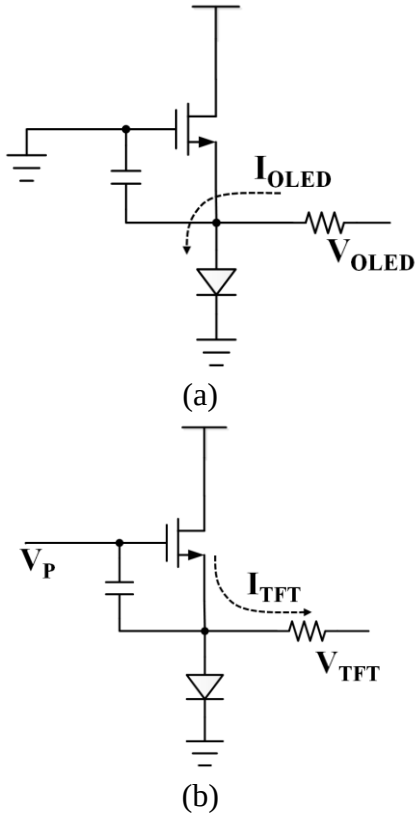

Fig. 8 Equivalent circuit for the defect extraction phase when extracting (a) OLED and (b) TFT status.

Fig. 8(a) shows an equivalent circuit of the extraction phase for the OLED. In this phase the gate voltage of the driver TFT is set to ground level to turn it off and the monitor line is set to a higher voltage of V_{OLED}. The current flowing through the OLED can then be captured by measuring the current flowing into the monitor line. As the I-V characteristic of the OLED can be a signature of its efficiency, the aging of OLED can then be captured from pre-acquired data for this type of OLED.

In Fig. 8(b), the gate voltage of the driver TFT is set to a higher level of V_P. The TFT is then turned on and part of the drain current flows to the monitor line. Combining the extracted I-V characteristic data of the OLED and the voltage and current measurements in this phase, the I-V characteristic of the driver TFT can be extracted.

After capturing the defect and aging data for both the driver TFT and OLED, the data voltage for the desired luminance can be calculated and applied to the pixel by external circuitry.

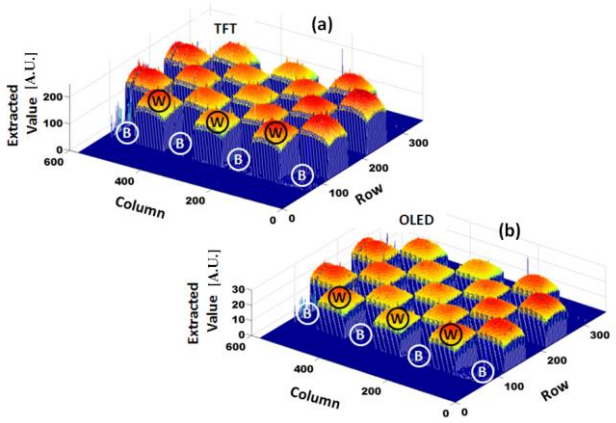

Fig. 9 Extracted aging parameters for (a) TFTs and (b) OLEDs after continuously displaying a checker board (W: displayed with white squares, B: displayed with black squares)

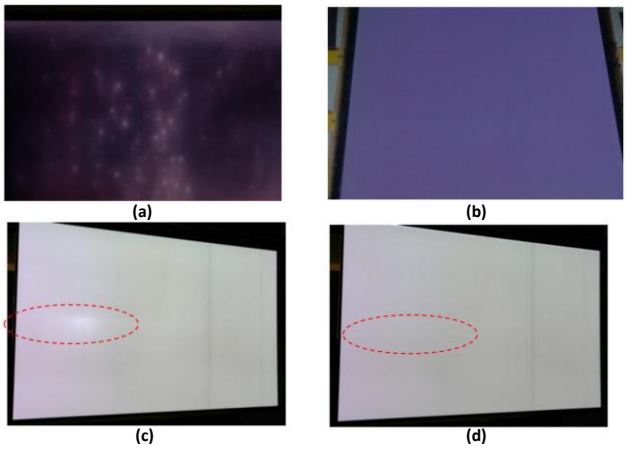

Fig. 10 Defect compensation in display panels (a) display panel as fabricated without compensation (b) display panel after defect compensation (c) hot spot induced by TFT back plane (d) hot spot

The aging and defect status of TFTs and OLEDs extracted through the monitor lines are shown in Fig. 9(a) and Fig. 9(b), respectively. The sharp hazards that happen randomly among the panel show the fabrication defects of the pixels. And the patterns in red, yellow and green color express the aging of each device. As the center of the displayed white square has higher temperature due to self-heating of the surrounding pixels, the aging of these pixels will be faster compared to other pixels.

The display panel using this method has the ability of compensating all kinds of defects that can be extracted through the monitor line. The compensation results are shown in Fig. 10 depicting the defect status in Fig. 10(a)&(b) and temperature compensation in Fig. 10(c)&(d).

This method provides a generic solution for TFT compensation and will be particularly useful in compensation of mechanically-induced (reversible) defects or aging in flexible displays. As measurement of the TFTs can be done in a monitoring phase, the obtained parameters can then be used to bias the TFTs to have an ideal overall performance. The geometric dependence of transistors can also be extracted from this pixel, as during the sequence described in Fig. 8(a) & (b) one can also apply voltage sweep to obtain the measured I-V characteristics for both TFT and OLED devices.

In summary, defects of TFTs can be compensated through separating the working sequence into several phases and by adding a compensation phase to extract and compensate non-idealities. To apply this method to other analog circuits, it is possible to intentionally separate the working sequence and apply similar methods. Here, switch-capacitor circuits can be a promising candidate. An example of this applied to analog building blocks was reported in [61].

IV. Specific Device Properties and Alternate Circuit Architectures

Devices processed using different thin film technologies usually have a specific property, which can sometimes be self-limiting. This requires the use of alternate circuit architectures. For example, most TFT technologies lack complementarity, thus the circuits have to be designed using mono-type devices, which means the designs cannot benefit from the well-established CMOS architectures. Specifically, the load of an analog amplifier needs to be redesigned to achieve high gain as the complementary load is not applicable. Another example is persistence photoconductivity in oxide TFTs, which, while ideal for image capture, requires a sharp gate a pulse to reset for high frame rates. We will discuss these examples in the following.

1) Analog gain stage with mono-type TFTs

CMOS gain stages benefit from the complementary structure [62]–[64]. For example, in

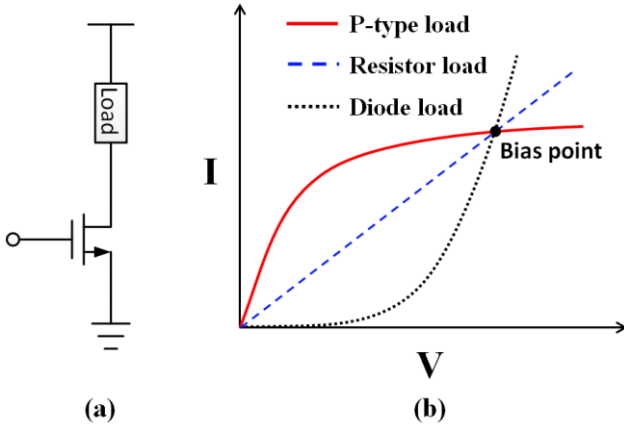

Fig. 11 (a) Common-source gain stage of an amplifier (b) sketch of different type of loads passing through the same bias point

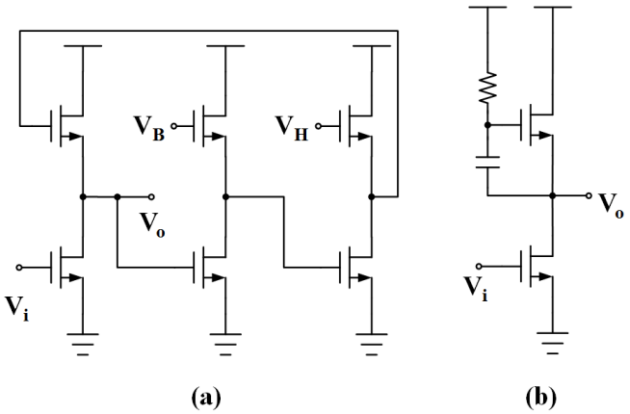

Fig. 12 Gain stage of an amplifier with (a) feedback load [22], [24] (b) boost strap load [20]

the case of NMOS as the input stage and PMOS as the load, the gain of the stage can be boost up to the order of magnitude of $g_m r_o$. The use of PMOS load provides large enough bias current with small voltage and, at the same time, big small signal resistance. These requirements are hard to be achieved with only one type of transistors.

To simplify the problem, we consider a single common source amplifier stage as shown in Fig. 11(a). Here, the load is considered as a two terminal device. Assuming the bias conditions of the driver TFT is fixed (to maintain g_m for fair comparison between different loads), the load of this gain stage would have fixed bias current. Here, we consider a fixed bias point of the load for comparison, i.e. the I-V characteristic of the load should pass a fixed point in the I-V plot (Fig. 11(b)). As the gain stage needs a higher small signal resistance of the load to produce high gain (i.e. derivative at the bias point should be close to zero), the current is better a concave function of voltage which means p-type load is more beneficial. Note that for other type of loads, the same small signal resistance can only be achieved by moving the bias point to the right hand side, i.e. increase the voltage bias of the load. However, a higher voltage bias would yield higher power consumption. From this standpoint, we conclude that for high gain, a p-type load with fixed gate bias (concave function) is more beneficial than a resistive load (linear function) and, subsequently, a diode or diode-connected TFT load (convex function) as it yields higher gain at the same power consumption.

The most familiar concave function in TFT behaviors is the output characteristic (I_D-V_{DS} characteristic with fixed V_{GS}). However, the design is limited by the connection of n-type devices as the source terminal of the load TFT is connected to the output node of the gain stage. Thus, the gate terminal of the TFT cannot be chosen as a fixed level but should follow the change of the source terminal.

One straight forward solution is to use a depletion mode load and short circuit the load transistor's source and gate terminals. (Depletion mode transistor can work in saturation regime with zero V_{GS}.) Amplifiers have been designed around 1980s to achieve high gain with depletion and enhancement NMOS transistors [64]–[66]. However, in TFT circuit area, this approach is limited by process complexity. By far, only digital circuits have been fabricated out of depletion load [67]–[69].

In order to use only enhancement mode TFTs while still obtaining high enough gain, it is also possible to use feedback loop to maintain a fixed V_{GS} for high small signal resistance of the load. One approach is reported in [22], [24]. The circuit reported is shown in Fig. 12(a). Here, an analog adder is designed for the DC bias of the load transistor. The feedback circuit, in effect, adds a bias voltage to the source terminal of the load transistor and applies the resulting voltage to the gate terminal. Here, the feedback voltage at the gate terminal of the load TFT can be calculated as:

$$V_F = V_H - V_B + V_o \tag{10}$$

Here, V_H and V_B are external bias voltages and Vo is the output of the gain stage (which is also the source terminal voltage of load). As the feedback voltage contains the output, this topology has a positive feedback.

Another approach using positive feedback has been reported by H.Marien et al [20]. The load of their gain stage is designed with boost strap structure. Other than maintaining the V_{GS} level of the load TFT, the structure successfully separates the DC bias and the small signal resistance and as a result obtains a higher gain for small signals at a higher frequency. The circuit needs a large capacitor for the load (a high pass filter) to reduce its lower 3dB frequency close to DC range. This also makes the circuit hard to work at very low frequencies, especially when the original signal is close to DC. An NMOS version of the circuit has been shown in Fig. 12(b). Other approaches regarding positive feedback are also reported in [23].

To summarize, positive feedback is used for gain-enhancement in single type TFT amplifiers. The major problem of this kind of approach is that positive feedback sacrifices the phase margin (PM) of the amplifier and would potentially cause instability. Although a cascode technique can be chosen to enhance the gain without sacrificing PM, it is not preferred in TFTs since a much higher supply voltage is needed because of the high threshold voltage of TFTs.

2) Persistent Photoconductivity

This can arise depending on the channel composition in oxide transistors when the transistor is under exposure to ambient light or when subject to negative bias illumination stress (NBIS) [21]. As the drain current of the TFT increases after exposure to ambient light, it is possible to use this characteristic for photo-sensing applications. In this application, the variation of current is not a defect that needs to be compensated. However, to use this property, the slow recovery process makes it hard to capture the changing image at high frame rate or to restore the TFT's initial state. Fig. 13(a) depicts the drain current of an IGZO TFT under periodic luminance

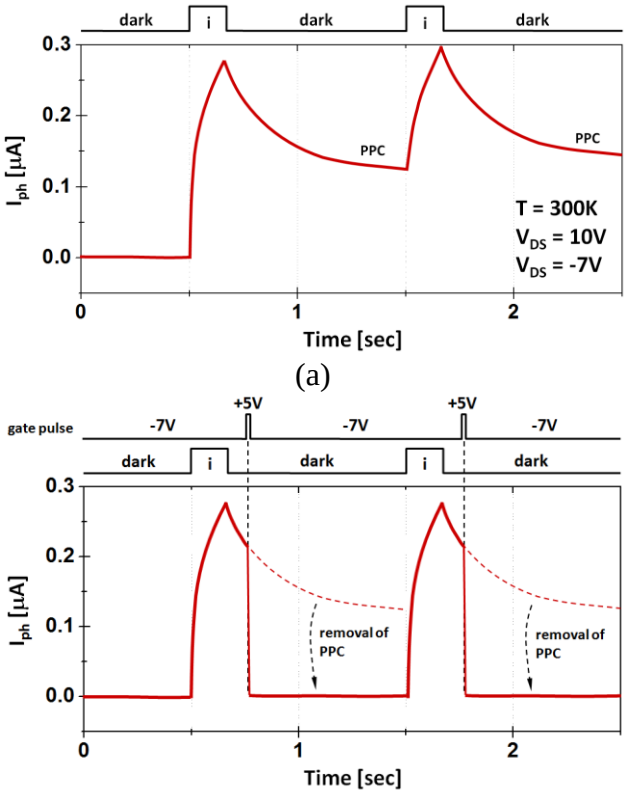

Fig. 13 (a) Observation of persistent photoconductivity (PPC) as a slow recovery and (b) removal of PPC with a positive gate pulse to get fast recovery.

and darkness. The results show the drain current recovering only slowly even in a completely dark environment..

In order to remove the persistent photoconductivity and recover the TFT to its original state, it has been found that by applying a positive pulse to the gate of the TFT, the PPC can be eliminated very quickly. The results in Fig. 13(b) show that fast PPC removal is possible after the gate pulse technique.

The phenomenon of PPC is explained by the band diagram shown in Fig. 14. As the ambient light excites the electrons in defect states to the conduction band, ionized oxygen defects are created. The excited electrons effectively increase the conductivity of the device as the electron concentration is increased. In order to accelerate the recovery process, the recombination of photo-induced electrons and ionized oxygen defects V_O^{2+} needs to be accelerated. By applying a positive

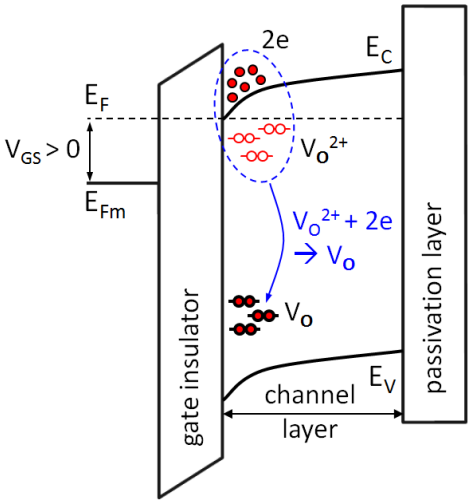

Fig. 14 Band diagram to explain the effect of positive gate pulse on recovery.

voltage pulse to the gate of the transistor, the electrons are swept away from the conduction band to recombine with the ionized oxygen defects thus removing the PPC.

PPC removal is a great example of device circuit interaction as the defect (i.e. light induced instability) of a TFT can actually be utilized to sense luminance signal, i.e. as a photo sensor. Indeed DCI should be considered not only to enhance circuit performance and/or overcome difficulties in the design but also to utilize specific properties stemming from the operating environment.

V. Conclusion

This paper reviewed and analyzed the intrinsic parameters of TFTs and proposed ways of analyzing the maximum achievable current accuracy of TFTs and to help determine when compensation becomes mandatory to enhance reliability and combat ageing. We presented techniques for extraction of defects and aging in devices using closed-loop feedback techniques and discussed their extension to other applications.

In summary, device circuit interactions are crucial when designing high performance circuits and systems to either utilize or minimize the impact of intrinsic adversaties associated with low temperature thin film technology. Consideration of device circuit interactions in design of TFT systems is even more compelling than the case of CMOS technology because of the wide range of materials imperfections, which give rise to device instability and large area processing-induced non-uniformity. Of specific importance to mechanically flexible systems is the impact of bending-induced (reversible) defects and associated aging, which makes compensation even more compelling. The techniques presented here can extend the current application of TFTs from active matrix pixelated arrays to newly-emerging application area that require TFT operation in analog operation mode.

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