Graphical Abstract

Comprehensive electrical analysis of interface states in Al_2O_3/OH-terminated (111) diamond MOSCap

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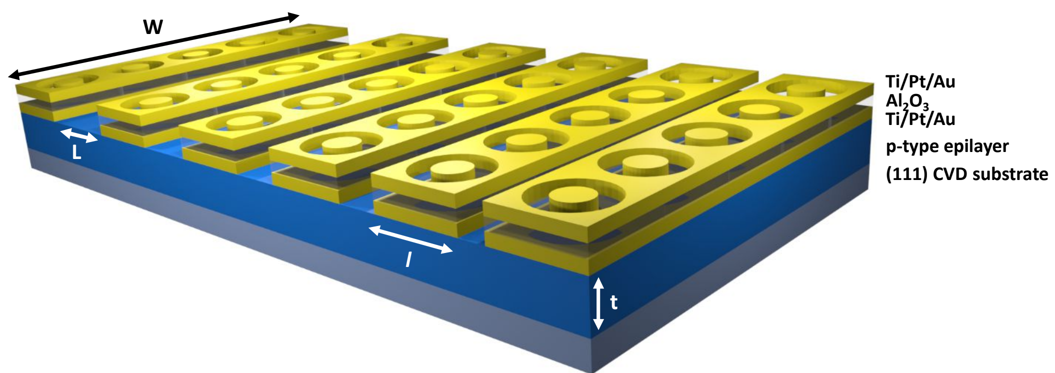

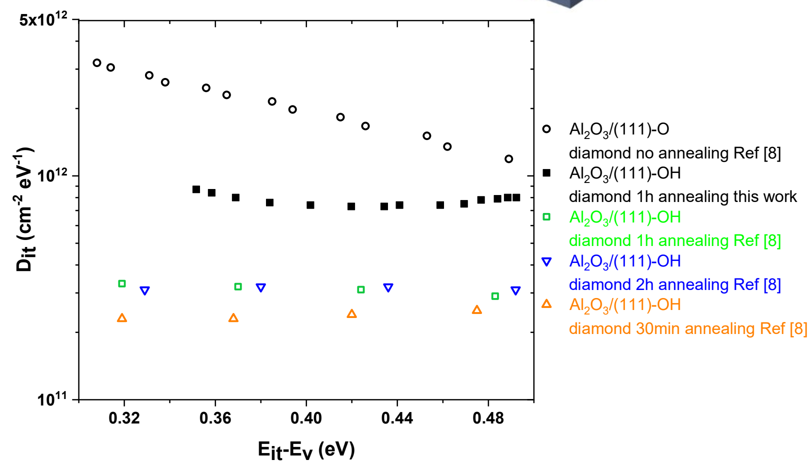

Highlights

Comprehensive electrical analysis of interface states in Al_2O_3/OH-terminated (111) diamond MOSCap

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- Original method combining transfer length measurements with capacitance-voltage and frequency analysis to extract the interface trap density and their energy distribution.

- Demonstration of an high quality Al_2O_3/OH-terminated (111) diamond interface.

- First experimental value of electron affinity for OH-terminated (111) diamond.

- Extraction of experimental value of specific contact resistivity for OH-terminated (111) diamond.

Comprehensive electrical analysis of interface states in Al_2O_3/OH-terminated (111) diamond MOSCap

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Abstract

Diamond, with its exceptional electrical and thermal characteristics, is a promising wide bandgap material for high-performance electronics in extreme environments. However, the efficiency of diamond-based metal oxide semiconductor devices is often hindered by interface states between the diamond and the oxide layer, which can degrade mobility, threshold voltage, and gate control. Al_2O_3 is commonly used as the insulating layer due to its compatibility with diamond, but its interface with diamond can introduce undesirable states that affect device performance. This work focuses on the OH-terminated (111) diamond/Al_2O_3 interface, which has shown potential for normally-off metal oxide semiconductor field effect transistor with limited interface state density. The paper details the fabrication of OH-terminated (111) diamond/Al_2O_3 metal oxide semiconductor capacitors, describes an original method combining transfer length measurements with capacitance-voltage and frequency analysis, and discusses the extraction of interface trap density (D_{it}) and their energy distribution. The energy distribution of D_{it} was estimated using the conductance method, indicating that D_{it} was in the range of (0.7-0.9) $\times$ 10^{12} $cm^{-2}eV^{-1}$ within 0.34-0.49 eV from E_V of diamond. Lastly the electron affinity was estimated to be $e\chi_{(111)-OH}$ = 0.36 eV, the first experimental value for the electron affinity of OH terminated (111) oriented diamond. The results are compared with existing literature to provide insights into the optimization of diamond-based metal oxide semiconductor devices.

Keywords: Diamond, MOS structure, interface states

1. Introduction

The integration of wide bandgap materials in electronic devices has garnered increasing interest due to their potential to operate in extreme environments, such as high temperatures, intense radiation, and high-power conditions. Among these materials, diamond stands out for its exceptional electrical and thermal properties, such as high carrier mobility, high thermal conductivity, and remarkable chemical stability. However, the effective utilization of these properties in Metal-Oxide-Semiconductor (MOS) devices requires a deep understanding of the interface states between diamond and the oxide layer, which play a crucial role in determining the electrical characteristics of the devices.

Interface states, often caused by crystalline defects, impurities, or dangling bonds, can trap charge carriers and thus affect mobility (Ref.[1]), threshold voltage (Ref.[2]), or even create Fermi level pinning, rendering the gate ineffective. Al_2O_3, a high-k dielectric oxide, is frequently used as an insulating layer in these devices due to its compatibility with diamond in terms of band alignment and excellent dielectric properties (Ref.[3]). Nevertheless, the interface between diamond and Al_2O_3 can introduce undesirable interface states that degrade the electrical performance of the device.

Several types of surface termination have been studied (O-terminated, H-terminated, or OH-terminated Refs.[4, 5, 6, 7, 8, 9]) to achieve 2D gas transistors or bulk conduction transistors with gate control of the transistor. In the latter case, there may be an interest in combining bulk conduction in an epitaxy with that of a two-dimensional gas at the interface with the oxide

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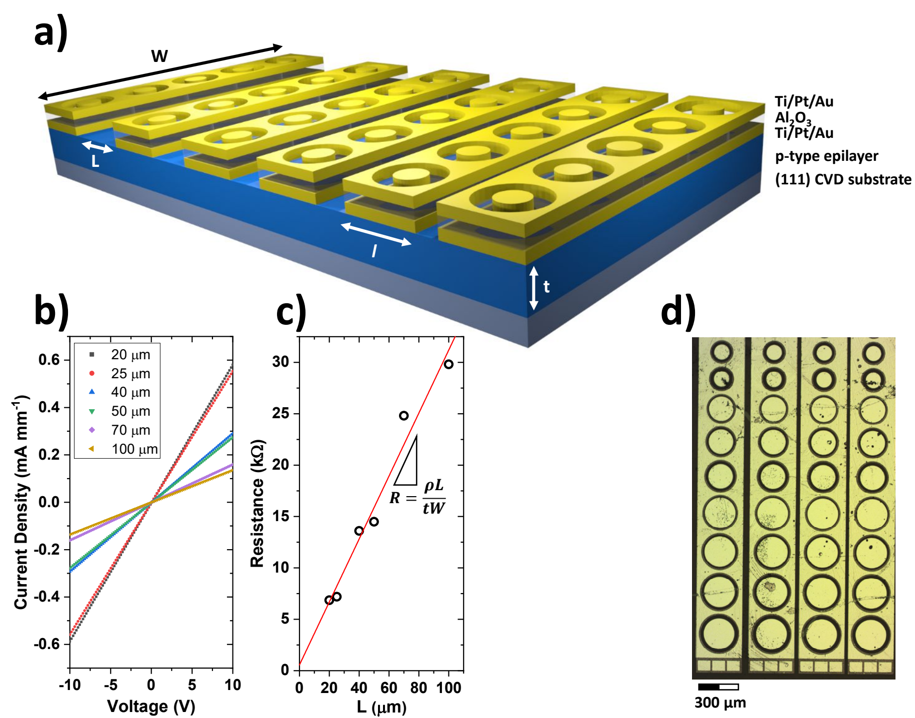


Figure 1: a) 3D schematics of the sample with the key lengths: W = 2.5 mm, l = 0.3, t= 400 nm and L. b) I-V characteristics for the different gaps L (20, 25, 40, 50, 70, 100 μm) performed after the first metal deposition. c) Extracted resistances as a function of the gap L fit. d) Top view optical microscope image of the fabricated MOSCap.

(Ref.[10]). Additionally, it is important to have reliable characterization methods that allow understanding the influence of interface states on the electronic properties of the components.

The diamond/Al_2O_3 interface has been recently intensively studied for both (111) and (100) surfaces. In particular, the (111) surface with OH termination allows obtaining a normally-off state MOSFET while limiting the interface state density. This paper aims to propose a new method to study the electrical analysis of MOS capacitance type, complementing the recently published studies in this field (Refs.[7, 8, 9]).

In a first part, we will present the experimental details of the fabrication of the OH-terminated (111) diamond/Al_2O_3 MOSCap. In a second part, the method based on the combination of the transfer length method with capacitance versus bias voltage and frequency will be described. In a third part, the extraction of interface trap density and their energy distribution will be discussed and compared to the state of the art. Finally, the paper will be summarized.

2. Experimental methods

2.1. Fabrication Process

A 400 μm thick (111) diamond mono-crystal grown by chemical vapor deposition provided by Excellent Diamond Products corporation was used as substrate. The level of residual impurities was measured using secondary ion mass spectrometry and found to be below 0.5 ppm nitrogen concentration, as well as being below the detection limit for boron and silicon atoms. A p-doped epilayer was grown by microwave plasma enhanced chemical vapor deposition with targeted Boron concentration of [B]= $10^{16} cm^{-3}$ and thickness t= 400 nm. A Ti/Pt/Au (20/30/20 nm) multi-layer metal deposition was performed, with titanium in contact with the diamond surface to form titanium carbide (TiC) and reach ohmic contact properties on p-layer. A first annealing at 600 $^\circ C$ under high vacuum (10^{-8} mBar) during 1 hour has been done to favor TiC bonding and reduce the contact resistance. To form OH-terminated surfaces, the water vapor (wet) annealing was used (Refs.[8, 11]). The annealing treatment occurred under an atmosphere of argon bubbled through ultra-pure water in a chamber with the sample holder heated at 600 $^\circ C$ during 1 hour. The flow of the argon gas was 300 sccm. Then, the sample was immediately transferred to the Atomic Layer Deposition (ALD) system, where alumina (Al_2O_3) was deposited at 380 $^\circ C$ with a targeted thickness of t_{ox} = 50 nm (Ref.[12]). A 500 $^\circ C$ annealing in high vacuum (10^{-8} mBar) during 30 min was performed. Finally, a second Ti/Pt/Au (20/30/20 nm) multi-layer metal was deposited on top of the oxide. The metal-oxide-metal stack formed is then electrically broken by applying an high bias voltage. Top view optical microscope image of the fabricated Metal Oxide Semiconductor Capacitors (MOSCap) is shown in Fig.1d. Figures 1a and 2a illustrate 3D schematics of the sample and vertical section of a single MOSCap, respectively. Among the 6x9 MOSCap that have been fabricated, two are exhibiting functional electrostatic control of the MOSCap without leakage current with a detection limit in the range of 1 pA. This low yield of functional MOSCaps is due to numerous difficulties encountered during the clean room process, caused by the non parallel face of the sample.

2.2. Experimental measurements

Two types of electrical measurements were performed: *i*) static current voltage I-V measurements using the technique of the Transfer Length Method (TLM) and *ii*) capacitance voltage capacitance versus voltage C-V and versus frequency C-f measurements. The electrical measurements setup used in this study consisted of an under vacuum ($\approx 10^{-4}$ mbar) probe station and the multi-source 2612B Keithley SourceMeter for I-V. TLM measurements were performed after the first metal deposition, taking advantage of the fact that the rectangular-shaped columns with W = 2.5 mm and with l = 0.3 mm of the ohmic contacts of the MOSCAPs were subsequently realised with gaps of various length L ranging between 20 μm and 100 μm (see Fig. 1a). For C-V and C-f measurements a Modulab XM MTS was used, able to probe at frequencies from 1 Hz to 1 MHz and at DC voltages up to 100 V. The software is converting the measured impedance to capacitance using a parallel RC equivalent circuit. Capacitance measurements were performed after the second metal deposition and the metal-oxide-metal stack was electrically broken by applying an high bias voltage. A second TLM measurement was performed after braking the oxide layer to confirm that the resistance due to the broken oxide is negligible. All measurements have been performed at room temperature (298 K).

3. Results and discussion

3.1. Transfer Length Method (TLM)

Fig.1b shows different I-V characteristics for the different gaps L. The current follows a linear trend for all gaps L, indicating ohmic contact behaviour. The extracted resistances R are subsequently plotted in the graph in Fig.1c as function of L. Assuming that the substrate is insulating and not participating to the conduction between two contacts and that the whole thickness of the epilayer is homogeneously conducting, a linear fit was done to extract the resistivity ρ of the p-doped layer using the formula

$$R = \frac{\rho L}{tW} + 2R_c \tag{1}$$

a resistivity ρ = 40 Ω·cm was extracted. This value, considering the targeted p-layer doping, can give us an estimate of the compensation N_D (Ref.[13]) which is between 5% and 10%. Using Eq. 1 we can also extract the contact resistance R_c = 280 Ω at RT. The specific contact resistivity expressed as:

$$\rho_C = R_c \cdot S_C \quad \text{with} \quad S_C = L_T \cdot W \tag{2}$$

S_C is the surface contact area. In a lateral geometry, the current only crosses the contact edge up to the transfer length L_T, which is determined by the intersection of the x-axis of the line fitted to the distance dependence of resistance shown in Fig.1c. The transfer length extracted from the fit is $L_T = 1 \pm 1 \mu m$,

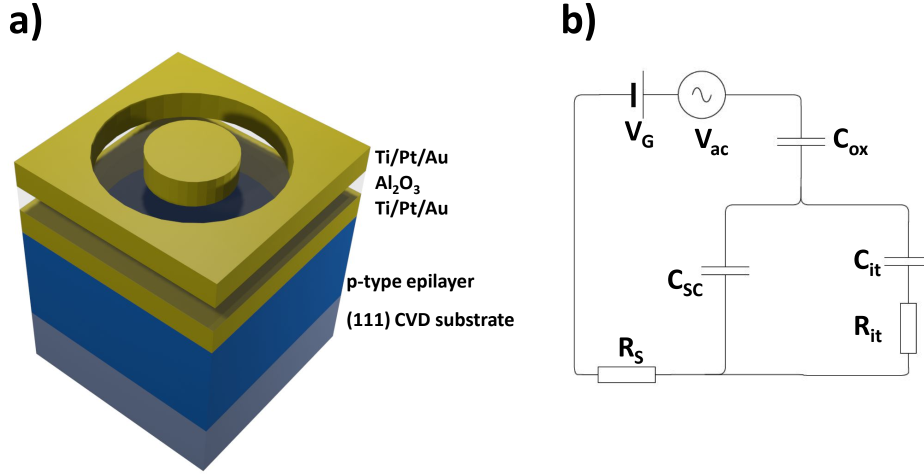


Figure 2: a) Schematic of the vertical section of a single MOSCap. b) Equivalent circuit taking into account oxide capacitance C_{OX}, space charge region capacitance C_{SC}, interface state traps capacitance C_{it} and resistance R_{it}, and p-layer resistance R_S.

subsequently used to calculate $\rho_C = 7 \cdot 10^{-2}\Omega.\text{cm}^2$. Reports on the (111) p-type diamond/metal interface are much less numerous than those on the (001) interface because difficulties in fabricating high-quality p-type diamond (111). Nevertheless, some results show similarities between the two types of interface (Ref.[14]). We can compare the value of ρ_C obtained with the (001) data (Ref.[14]) and it fits in the trend of ρ_C as function of the boron doping concentration. With this result, we can further confirm the similarities between the two types of interface. In particular for the specific contact resistivity, the factor that has the greatest impact on it is the doping concentration and not the surface crystalline orientation.

3.2. MOS Capacitance

The equivalent electrical circuit of a MOSCap depends on various physical parameters. In our case, the series resistance R_S and the presence of interface states are two parameters that cannot be neglected, unlike the leakage trough the oxide, which can be neglected since below 1 pA. In that case, the equivalent circuit is the one of Fig.2b (Ref.[15]) including the capacitance of the oxide C_{OX}, the one of the p-layer due to the space charge region C_{SC} which is in parallel with the capacitance and the resistance caused by the presence of the interface state traps, C_{it} and R_{it}. Finally to close the circuit, the current pass through the p-layer with a resistance R_S.

When characterizing a MOSCap, one has to be cautious on the effect of all these factors, because the measured capacitance C_M can be significantly different than the ideal capacitance C, i.e. the capacitance of the oxide in series with that of the semiconductor, $\frac{1}{C} = \frac{1}{C_{OX}} + \frac{1}{C_{SC}}$.

3.2.1. MOSCap frequency dependence

First, the effect of the serial resistance R_S will be considered. If the effect of interface state traps is neglected, the circuit is equivalent to an R_SC series circuit, an high-pass filter. The measured capacitance C_M becomes:

$$C_M = \frac{C}{\sqrt{1 + (\omega R_S C)^2}} = \frac{C}{\sqrt{1 + (\frac{\omega}{\omega_{cutoff}})^2}} \tag{3}$$

with ω the angular frequency and $\omega_{cutoff} = \frac{1}{R_S C}$, the angular cutoff frequency. In order to avoid the parasitic effect of the serial resistance, it is necessary to lower the frequency measurement to meet the condition $\frac{\omega}{\omega_{cutoff}} \ll 1$, limiting the frequency range than can be probed. This effect can be clearly seen in Fig.3a where the values of C_M normalized to C_{ox} as a function of frequency for various values of V_G are represented. $C_{ox} = 11.5$ pF was theoretical calculated using the equation:

$$C_{ox} = \frac{\epsilon_0 \epsilon_{Al_2O_3} S}{t_{ox}} \tag{4}$$

with ϵ_0 the vacuum permittivity, $\epsilon_{Al_2O_3} = 8.5$ the relative dielectric constant of the Al_2O_3 (Ref.[16]) and $S = 7.9 \cdot 10^{-5}$ cm^2 the surface of the metallic gate contact on the oxide. This value is in good agreement with the capacitance value of the MOSCap measured at $V_G = -9$ V and at low frequency (< 10 kHz). Under these experimental conditions, the MOSCap should reach the accumulation regime, reducing the capacity of the MOSCap to that of the oxide. If we consider the curve for $V_G = -9$ V, the capacitance measured at high frequency decreases with a slope of -20 dB/decade. Moreover, the measured cut-off frequency $f_{cutoff} = \frac{\omega_{cutoff}}{2\pi}$ at -3 dB equals 12 kHz. Introducing the resistivity ρ, extracted from TLM measurements, R_S has been evaluated to be 1.5 MΩ and using $C_{ox} = 11.5$ pF from eq. 4 as the capacitance C (for $V_G = -9$ V), the calculated cutoff frequency f_{cutoff}= 9 kHz is in good agreement with the measured one. Fig.3b shows the phase of the impedance of the MOSCap as a function of frequency for different gate voltage V_G. At $V_G = -9$ V, the circuit behaves like an RC series circuit. For $f < 1$kHz, the phase is $-\frac{\pi}{2}$, characteristic to a purely capacitive behavior, and at f_{cutoff} the phase is $-\frac{\pi}{4}$, in good agreement

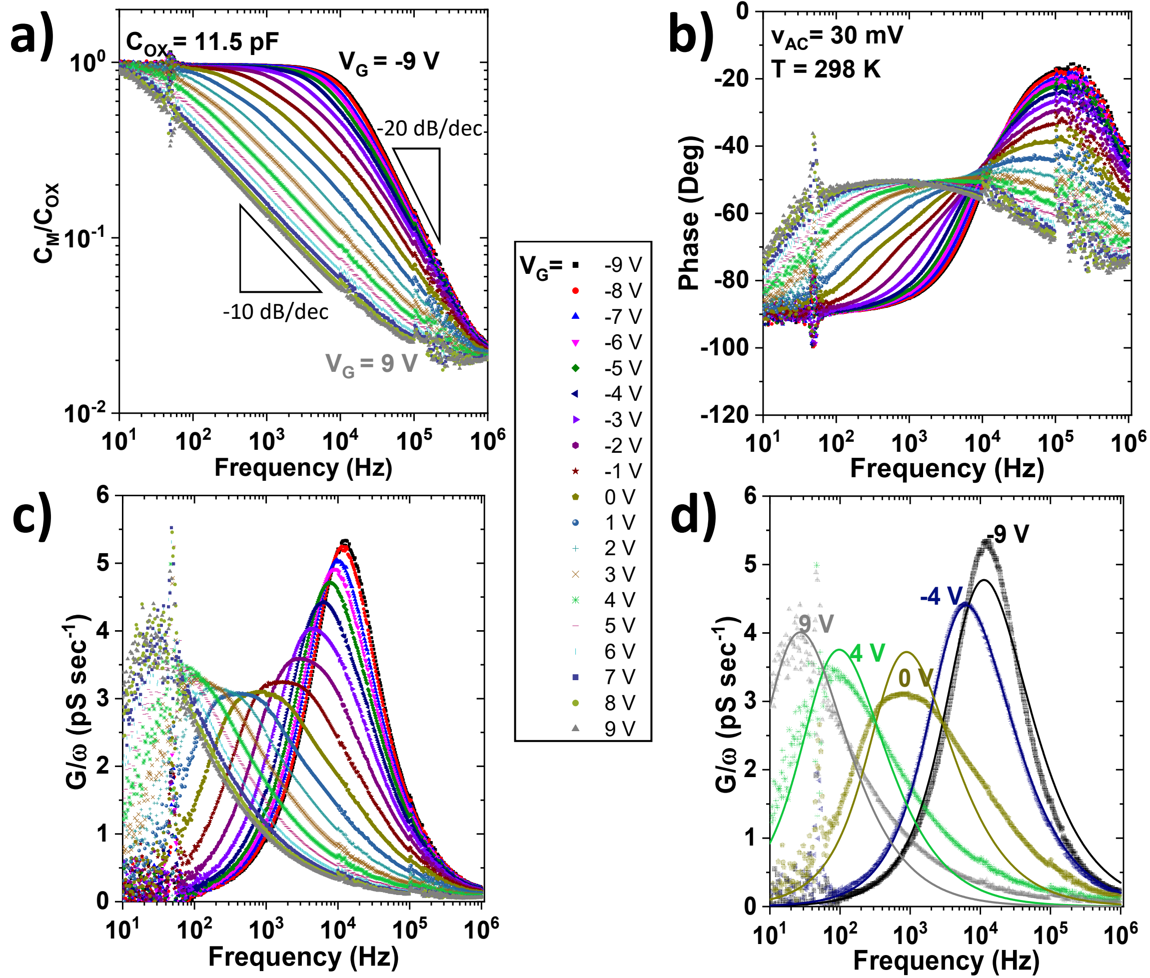


Figure 3: a) Measured capacitance C_M normalized to C_{ox} as a function of frequency for different gate bias V_G. b) Measured impedance phase as a function of frequency for different gate bias V_G. c) Normalized conductance $\frac{G}{\omega}$ as a function of the frequency for different gate bias V_G. d) Fit using Eq. 6 of the normalized conductance $\frac{G}{\omega}$ for some representative V_G values. All the measurements have been done at $T = 300$ K and with an AC signal amplitude of $v_{AC} = 30$ mV and varying the gate voltage V_G from -9 V to 9 V as described in the central box of the figure. The data at 50 Hz are perturbated due to the utility frequency, which is 50 Hz in Europe.

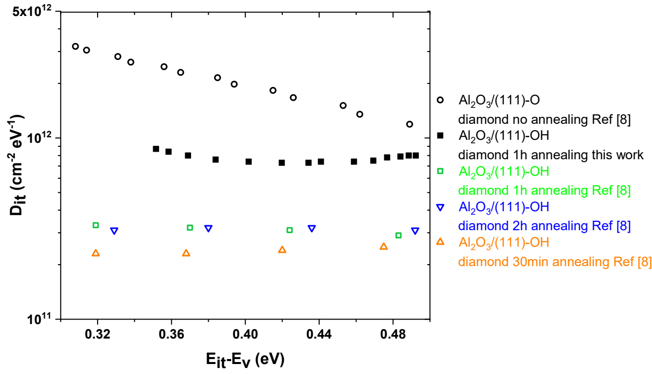


Figure 4: Energy distribution of interface trap density D_{it}. Solid data represent this work, empty ones Ref.[8] work. In the latter the capacitance-voltage based method (or quasi-static method) was used to extract D_{it} values for different vapor annealing treatments duration (30 min, 1 h and 2 h)

with a first order high pass filter. For voltages $V_G \geq -1$ V, at low frequencies, the trends previously described are no longer valid. The effect caused by the presence of the interface state traps needs to be taken into account, modeled by C_{it} and R_{it}.

The presence of this density of states introduces an additional charge Q_{it} in the system which play an important role in the frequency and bias MOSCap dependencies. The interface state emission time constant is described by thermal generation of carriers from the valence band (Ref.[17]) to the trap energy level by:

$$\tau_{it} = \frac{1}{\sigma v_{th} N_V} e^{\frac{E_{it}-E_V}{k_B T}} \tag{5}$$

with k_B the Boltzmann constant, T the temperature, σ the hole capture cross section of the trap, typically in the order of 10^{-16} cm^{-2} to 10^{-20} cm^{-2} for repulsive traps (Ref.[18]), $v_{th} = \sqrt{3k_BT/m^*} = 1.2 \cdot 10^7\ cm/s$ the mean hole thermal velocity, N_V the equivalent valence band density of state and E_{it} and E_V the trap energy and the top of valence band levels, respectively. In Fig.3c the normalized conductance $\frac{G}{\omega}$ as a function of the frequency are reported for different gate bias. Using the conductance method D_{it}, the interface trap density, and τ_{it} can be extracted from the fit by using the expression of $\frac{G}{\omega}$ in the case of a continuum of interface states (Ref.[19]):

$$\frac{G}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} ln(1 + (\omega\tau_{it})^2) \tag{6}$$

D_{it} and τ_{it} have been extracted from the fit of the data in Fig.3d for different V_G, as well as the value of the position of the trap relative to the valence band $E_{it} - E_V$, using the capture cross section of Ref.[8] $\sigma = 10^{-17} cm^{-2}$. The values of D_{it} as a function of $E_{it} - E_V$ are reported in Fig.4. For completeness, the values of $E_{it} - E_V$ using different σ are reported below. For $\sigma = 10^{-18} cm^{-2}$ $0.29\ eV \leq E_{it} - E_V \leq 0.43\ eV$ and for $\sigma = 10^{-16} cm^{-2}$ $0.41\ eV \leq E_{it} - E_V \leq 0.55\ eV$.

Finally,the conductance caused by the boron acceptors G_B (Ref.[20]) was evaluated, to verify that their contribution to the signal is negligible. The $G_B(\omega)$ are 2 to 3 orders of magnitude lower than the G's depending on the frequency.

3.2.2. MOSCap voltage dependence

In the previous sections, the contribution of the serial resistance and the interface states have been clarified. To avoid both effects and so evaluate the capacitance $\frac{1}{C} = \frac{1}{C_{OX}} + \frac{1}{C_{SC}}$ of the MOSCap, for gate voltage $V_G < -1V$, we selected the low frequency range, i.e. from 10 to 100 Hz, values of $C(f)$ in order to measure C_{ox}. Indeed, the high-pass filter composed by the MOS capacitance in series with the serial resistance has a cut-off frequency around 12 kHz as discussed in the previous section and so does not disturb the measurement. While the high pass filter formed by $R_{it}C_{it}$ can lead to two possibilities. Since the $R_{it}C_{it}$ constant is at higher frequencies, as shown by the $\frac{G}{\omega}$ curve, the interface states can be modeled by a pure C_{it} capacitance, which must be compared with C_{ox} and C_{SC} in order to understand its effect. If $C_{it} > C_{ox}$, then the resulting capacitance of these two capacitances in series is the smaller of the two, i.e. C_{ox}. If $C_{it} < C_{ox}$, since the measured value is equal to C_{ox}, this would mean that $C_{SC} > C_{ox}$, which corresponds to the accumulation regime. The experimental data for $V_G < -1V$ do not allow us to conclude that accumulation has been reached. However, they suggest that the Fermi level could be around the value of 0.35 eV above the valence band. For voltages above $V_G > -1V$, the situation is different. Two phenomena are superimposed: i) the MOSCap is in the depletion regime and so the capacitance of the space-charge region decreases versus bias, ii) as the Fermi level at the interface moves away from the valence band, the time constant of the interface states increases, which decreases the frequency of the low-pass filter due to interface states. Moreover, we observe a shift in the cut-off frequency towards high frequencies due to the series resistance. Consequently, the -20 dB/decade dependence of the measured capacitance disappears and is replaced by a -10 dB/decade dependence due to the low-frequency cutoff discussed above for the interface state. This cut-off frequency decreases down to below 100 Hz for $V_G > 4V$.

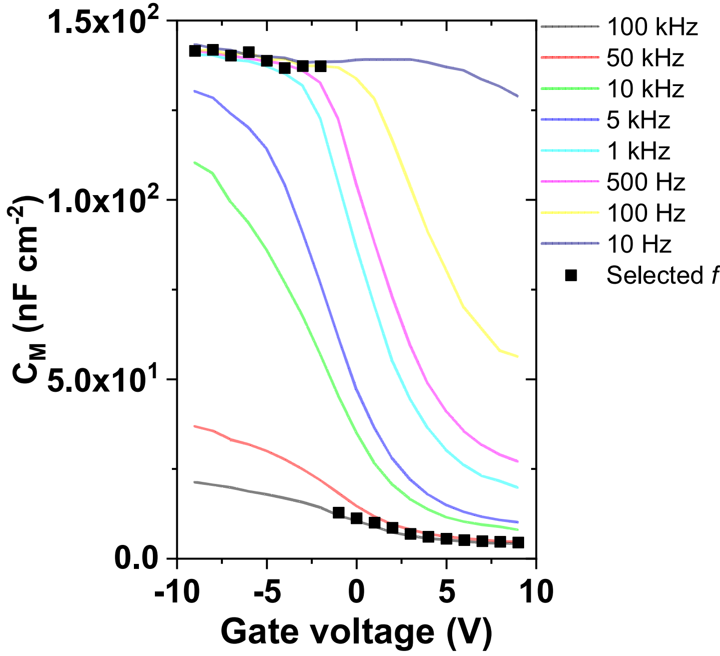
Then, in this high frequency range, the C_{SC} can be considered in parallel with R_{it} and highest frequencies should be favored to limit the R_{it} effect. We have therefore chosen capacitance values measured at 100 kHz for $V_G > -1V$. Fig.5a shows C_M normalized by the surface S as a function of V_G. Thanks to the voltage dependence of C_M, the acceptor doping level of the B-doped epilayer can be measured.

Fig.5b shows the plot of $\frac{1}{C^2} - \frac{1}{C_{ox}^2}$ commonly referred as Mott-Schottky plot, yields a linear dependence as function of V_G for positive voltage, in depletion region. The slope is proportional to $N_A - N_D$ and crosses the x-axis at the flatband voltage V_{FB}:

$$N_A - N_D = \frac{2}{q\frac{d1/C^2}{dV_G}\epsilon_0\epsilon_{diam}S^2} \tag{7}$$

The doping level extracted from the fit is $N_A - N_D = 3 \pm 0.2 \cdot 10^{16} cm^{-3}$ which is in agreement with the target boron concentration of the grown p-doped layer. Moreover, using the resistivity value, a compensation of 6.6% was estimated using the same approach as in Section 3.1(Ref.[13]).

The flat band voltage extracted from the fit is $V_{FB} = -1.2 \pm 0.2$ V. There are no reports in the literature on the work function



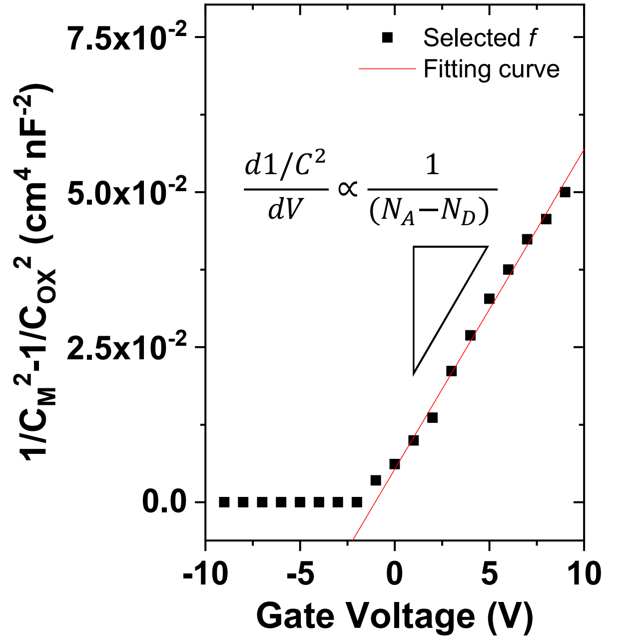


Figure 5: a) Measured surface capacitance C_M (normalized by the surface $S = 7.9 \cdot 10^{-5}\ cm^2$) as a function of V_G for different frequencies f. Solid square dots represent C_M for selected f: 100 kHz for $V_G > -1V$ and from 10 to 100 Hz for $V_G < -1V$. b) Mott-Schottky plot for selected f and linear fit for $V_G > -1V$ using equation 7.

of diamond (111) OH terminated $\Phi_{(111)-OH}$ to compare with our results. However, considering the work function of Titanium $e\Phi_{Ti} = 4.33$ eV and assuming the absence of charge in the oxide, $e\Phi_{(111)-OH} = e\Phi_{Ti} - eV_{FB} = 5.5 \pm 0.2$ eV can be estimated. The hole density $p = 10^{13} cm^{-3}$ has been calculated thanks to the charge neutrality equation for p-type (Ref.[13, 21]) using the value of acceptor concentration and compensation extracted previously. Moreover, using the equation

$$p = N_V e^{-\frac{E_F - E_V}{K_b T}} \tag{8}$$

with $N_V = 10^{19} cm^{-3}$ the effective density of states in the valence band, the value of $E_F - E_V = 0.36$ eV can be calculated. Thanks to the equality $e\Phi_{(111)-OH} + (E_F - E_V) = e\chi_{(111)-OH} + E_g$ with $E_g = 5.5$ eV the energy gap of diamond, the value for the electron affinity of OH terminated (111) oriented diamond $e\chi_{(111)-OH} = 0.36$ eV can be finally extracted. This value lies between the theoretically and experimentally calculated ones for H and O terminated diamond, ranging between -2 eV for H and +2 eV for O (Ref.[22, 23, 24]). Note that this value was obtained using the capture cross section of Ref.[8] $\sigma = 10^{-17} cm^{-2}$.

4. Conclusion

In summary we introduced an original new method combining TLM with capacitance-voltage and frequency analysis to study the electrical analysis of MOSCap, complementing the recently published studies in this field. Thanks to transfer length method, the resistivity $\rho = 40\ \Omega$·cm and the specific contact resistivity for (111) p-type diamond/metal interface $\rho_C = 7 \cdot 10^{-2} \Omega.\text{cm}^{-2}$ were extracted and compared to (001) diamond oriented data. The C-V and C-f characteristics from 10 Hz to 1 MHz and from $V_G = -9$ V to $V_G = 9$ V at 298 K were examined. Thanks to the conductance method, we showed that interface states exist at energy levels 0.34-0.49 eV from E_V with an energy distribution of the interface states D_{it} in the range of (0.7-0.9) × 10^{12} cm^{-2}eV^{-1}. Moreover, thanks to the Mott-Schottky plot, a value for the flat band voltage equal to $V_{FB} = -1.2 \pm 0.2$ V was extracted, together with the first experimental value for the electron affinity of OH terminated (111) oriented diamond $e\chi_{(111)-OH} = 0.36$ eV. . These data, since there is a lack of statistics on OH terminated (111) oriented diamond, can be valuable in terms of the design of future devices.

To conclude, this comprehensive electrical characterization and analysis carried out, led us to have a better understanding in the physical mechanisms of gate controlled OH-diamond MOSCAPs, which is necessary for the future optimization of diamond-based MOS devices.

Acknowledgement

This work is part of the project "Large Size Diamond MOSFET", which has been partially funded by the French Agency

for Research under Grant Agreement No ANR (ANR-21-CE50-0036). The author would like to thank Arnaud Claudel and NanoFab Team from Institute NEEL for technical formations, supports and scientific advice for this work.

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