Promoting Low-Voltage Saturation in High Performance a-InGaZnO Source-Gated Transistors

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Abstract: As oxide semiconductors increase in popularity with emerging flexible electronics, advances in material performance may lead to parasitic and non-ideal effects becoming more prominent. Specifically, in source-gated transistors, and other contact-controlled devices, the influence of the lateral drain field produced by drain bias leads to an overwhelming increase in charge density at the source edge and obliterates their signature flat saturation at low drain voltages. Here, we present high current density amorphous InGaZnO (a-IGZO) source-gated transistors (SGTs) in a bottom contact architecture using Pt source and drain electrodes. The devices were fabricated by ensuring an oxygen-rich atmosphere to prevent the formation of oxygen vacancies at the Pt/a-IGZO interface. Incorporating a field relief structure within the source contact improves drain current saturation, towards behavior predicted by the saturation coefficient. In the device architecture considered, the screening was less effective for a field plate insulator thickness under 30 nm, possibly due to increased tunnelling. Field plate incorporation is one of the strategies that ensures flat saturation and the suitability of contact-controlled transistors for a multitude of current driving and amplification applications.

Index Terms: Amorphous oxide semiconductors, contact-controlled, drain relief, amorphous InGaZnO, field plate, thin-film transistor, source-gated transistor, Schottky barrier.

1. Introduction

Amorphous oxide semiconductor (AOS) thin-film transistors (TFTs) are one of the most proliferous devices in research [1], [2]. Notably, amorphous InGaZnO (a-IGZO) TFTs, from their first demonstration [3], were rapidly adopted into commercial displays, due to their ability to deliver high drive current with low leakage off-state [4]. Yet, with the constant pursuit to deliver a-IGZO TFTs with higher field-effect mobility $\mu_{FE}$, often device non-idealities can result in an unwanted increase in drain current, such as short channel and hot-carrier effects, which degrade the saturation behavior [5]–[7]. Such device non-idealities would restrict the development of analog applications based on a-IGZO TFTs.

An emerging TFT architecture, the source-gated transistor (SGT) [8], is a type of contact-controlled device, that deliberately employs contact energy barriers at the source electrode to induce source-side pinch-off. This device, along with subsequent evolutions [5], [9], is capable of achieving the lowest saturation voltages with the highest output impedance [10]–[12]. The trade-off in attainable
transconductance $g_m$ (when compared with an Ohmic contact TFT of the same geometry) does not significantly impact its intrinsic gain $A_v = g_m / g_d$, as its output conductance $g_d$ is several orders of magnitude lower than that produced by conventional types [10], [13]. Aside from high intrinsic gain and power-efficient operation, SGTs also are highly robust to electrical and mechanical stress, as well as a higher degree of device-to-device uniformity of operation [11], [14]–[17]. These devices would particularly benefit analog applications, such as current drivers or amplifiers [18]–[20].

Although the SGT is celebrating its 20th anniversary since its invention by Shannon and Gerstner in 2003 [8], uptake of the architecture by other groups has been a relatively recent development [13], [21]–[28]. Even though the SGT architecture controls some non-idealities regarding geometry and material variability well, designing high-performance SGTs is not without its own challenges [29], especially in AOS [12], [13], [30].

Thus, when fabricating these devices, there is a set of design rules to be followed [31], especially if process optimization involves higher mobility materials, such as a-IGZO. Conversely, it has been frequently seen that as researchers start exploring alternative geometrical structures or materials for TFTs, they could unintentionally create source-gated transistors through creating the right electrical conditions for the source contact to dominate the conductivity within the device in the desired region of operation [7], [32]–[36]. For example, in Tu et al. [7], devices with SGT behavior were observed when a field plate was added to the source contact of an a-IGZO TFT.
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It is well known that in high mobility materials, or certain geometries, SGTs might require shielding of the source contact from the lateral field induced by biasing the drain [11], [12], [31], [37], primarily to ensure flat saturation but also to mitigate hot-carrier effects [5] or self-heating [38].

Here, we present top gate, bottom contact (TGBC) SGTs realized using RF sputtered a-IGZO active layers (Fig. 1a), which achieve their predicted saturation characteristics [12] when a field plate is introduced at the source edge (Fig. 1b and 1c) [37]. These transistors also attain a comparatively high drain current per unit width compared with previous reports. We discuss some of the design considerations of the field plate architecture itself [11], [23], [24], [37], as well as alternative saturation improvement strategies. This analysis should prove useful in cases when device development does not initially yield the expected saturation behavior [12], [22], [30], [39], particularly in transistors with short source-gate overlaps, which are more prone to influence of the drain electric field [31].

2. Experimental Methods

A. Source-Gated Transistor Fabrication

Bottom contact, top gate staggered-electrode structure SGTs (Fig. 1d) were fabricated either on a Corning 7059 glass or SiO$_2$/Si substrates, both excluding (as in Fig. 1e) and including (as in Fig. 1f) field-plates after contact deposition. The fabrication process was as follows: the bottom contacts, (Ti/Pt, thickness $t = 7/40$ nm) was deposited using a Lesker electron-beam (e-beam) evaporator. The field plates (Al$_2$O$_3$, extension $FP_{ext} \sim 5$ μm (3 μm by design, but increased during alignment), and height $FP_{ins} \sim 10, 15, 30$ nm) were deposited from an aluminum target in an Ar/O$_2$ atmosphere using a high target utilisation sputtering (HiTUS) system, at a pressure of $3 \times 10^{-3}$ mbar, RF power of 1 kW, Ar/O$_2$ flow of 40/25 sccm, achieving a deposition rate of 2.5 nm per minute. The semiconductor (a-IGZO, $t_s = 22$ nm) was deposited from a ceramic target (In$_2$O$_3$:Ga$_2$O$_3$:ZnO = 1:1:1) in an RF magnetron sputter coater, at a pressure of $5 \times 10^{-3}$ mbar, RF power 50 W, Ar flow of 19 sccm, achieving a deposition rate of 3.4 nm per minute. A post-deposition annealing of a-IGZO was performed on a hot plate at 200 °C in air for 30 minutes. The dielectric layer, Al$_2$O$_3$ ($t_i = 70$ nm), was deposited using atomic layer deposition (ALD) at 200 °C from trimethyl aluminium and water (Savannah system, Cambridge Nanotech). Finally, the gate electrode ($t = 60$ nm) was deposited from a Mo target in a d.c. sputter coater, at a pressure of $3.5 \times 10^{-3}$ mbar, RF power of 100 W, Ar flow of 30 sccm. The metal contacts, field plates, channel layer were patterned using photolithography and lift-off methods, whereas the dielectric layer was patterned using photolithography and wet-etching.

Device dimensions are as follows for SGTs without field plates (Fig. 1e): $W = 110$ μm; $S = 6, 15, 51$ μm; $d = 6.5, 42.5$ μm. For SGTs with field plates (Fig. 1f), the features are: $W = 100$ μm (96 μm to account for misalignment of active and contact window); $S = 3, 12, 48$ μm, as defined by the contact window; $d = 12, 48$ μm. Even though the dimensions vary due to the mask design, the features are broadly similar and would not contribute greatly to any comparisons in this study, as $S$ is similar and drain current should not vary with $d$.

B. Device and Materials Characterization

Devices were electrically characterized using a Wentworth probe station and Keysight B2902A source/measure unit (SMU). Two arrays consisting of the three $S$ and two $d$ combinations were measured for each sample. The gate leakage of all devices is well below $10^{-12}$ A, which is the noise floor of the SMU.
For structural characterisations, film thickness was determined using a Gaertner He–Ne (633 nm) ellipsometer and Veeco Dektak profilometer. The resistivity and mobility of the films were determined at ambient temperature using an MMR Technologies Hall Effect Measurement System on thicker α-IGZO films ($t = 200$ nm) deposited on 0.8 cm × 0.8 cm glass substrates with Au top contacts, using van der Pauw structures. The sputtered thin film has a carrier concentration $\sim 10^{19}$ cm$^{-3}$ and a Hall mobility $\sim 12$ cm$^2$V$^{-1}$s$^{-1}$. After a post annealing at at 200 °C in air for 30 minutes, the carrier concentration and Hall mobility decrease to $\sim 6 \times 10^{15}$ cm$^{-3}$ and $\sim 6$ cm$^2$V$^{-1}$s$^{-1}$ respectively.

3. Results and Discussion

We first consider the device fabricated without a field plate. From the $g_m$ (Fig. 2a), it would seem, at first inspection, that an Ohmic contact has been formed at the α-IGZO/Pt interface. The output characteristics in Fig. 2b show poor saturation and Fig. 2c shows that there is no emergent trend with $S$, but there is a reduction in current with increased $d$. This would certainly be more fitting of an Ohmic contact device, or a device where the channel resistance dominates over contact resistance [40]. The output curves in Fig. 2b also reveal a small current crowding, but not a Schottky barrier, despite the use of high work function metal (Pt) contacts. It has been reported that formation of a Schottky junction with AOS is difficult and oxygen treatment of metal surface is necessary [41], [42]. The α-IGZO TFT exhibits a threshold voltage of $V_{th} = 7.5$ V, a sub-threshold slope of approximately 270 mVdec$^{-1}$, a switching ratio of $\sim 10^7$ and a field effect mobility $\mu_{FE} \sim 4.5$ cm$^2$V$^{-1}$s$^{-1}$. This $\mu_{FE}$ value is comparatively low for a conventional α-IGZO TFT, yet for SGTs it would certainly be in the expected range [12], [43]. Given the contact dominated behavior, $\mu_{FE}$ cannot be meaningfully extracted from SGT characteristics [43]. However, the fact that a somewhat lower than expected value is obtained by applying the conventional mobility extraction methods serves as an indicator of contact-controlled behavior. Thus, while creating a Schottky barrier in AOS can be challenging, it is likely that a rectifying contact exists at the α-IGZO/Pt interface.

Fig. 2. a) Transfer and b) output characteristics of the SGT without a field plate. There are no defining features of SGT behavior, as the device shows high transconductance and poor saturation. c) There is no emerging trend of increased drain current for longer $S$, but there is a reduction of drain current for longer $d$, which is a hallmark of field-effect transistor (FET) operation. Results such as these would only be indicative of a conventional Ohmic-contact thin-film transistor (TFT) rather than a contact-controlled SGT with a Schottky source.
When a field plate is introduced (Fig. 3), we can see the effects of both reduction in drain current (Fig. 3a) and an improvement in saturation as the field plate insulator \( FP_{\text{ins}} \) is increased (see Fig. 3b-d and Table I). The role of the field plate is to screen the source area from the lateral electric field produced by drain-source bias, which may lead to an effective lowering of the energy barrier at the source edge.

<table>
<thead>
<tr>
<th>Metric</th>
<th>No FP</th>
<th>10 nm ( FP_{\text{ins}} )</th>
<th>15 nm ( FP_{\text{ins}} )</th>
<th>30 nm ( FP_{\text{ins}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Threshold voltage, ( V_{\text{th}} )</td>
<td>7.5</td>
<td>6.2</td>
<td>8.1</td>
<td>11.8</td>
</tr>
<tr>
<td>( dV_{\text{DSAT1}}/dV_{\text{GS}} )</td>
<td>1</td>
<td>1</td>
<td>0.29</td>
<td>0.12</td>
</tr>
<tr>
<td>Output conductance</td>
<td>(</td>
<td>g_d</td>
<td>)</td>
<td>( \sim10^{-5} )</td>
</tr>
<tr>
<td>(( V_{\text{GS}} = 20 \text{ V} ))</td>
<td></td>
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</tbody>
</table>

**A. Field Plate Design and Saturation Behaviour**

In SGTs, charge injection takes place along the source, promoted by the drain-source voltage \( V_{\text{GS}} \) reverse biasing the source energy barrier. At sufficient \( V_{\text{GS}} \), the semiconductor adjacent to the source edge becomes fully depleted (Fig. 1b). If source-side depletion is not complete (due to a high charge carrier density being transported through this region, a low source energy barrier, and/or a very thick active layer), as in Fig. 1a, then the device cannot pinch-off and saturate at the expected \( V_{\text{DSAT1}} \) as given by (1).

\[
V_{\text{DSAT1}} = \left( V_{\text{GS}} - V_{\text{th}} \right) \left( \frac{C_i}{C_i + C_s} \right) + K
\]  

\[ (1) \]

The second term of (1) in parentheses is known as the saturation coefficient \( \gamma \), whereby the series specific capacitances of the depleted semiconductor \( C_s \) and gate insulator \( C_i \) determine early voltage saturation. After pinching off at the source end, the channel will saturate at \( V_{\text{DSAT2}} \), which is given by the first term in parentheses and is the same value as when the FET in the channel would pinch-off. \( K \) is a constant representing the drain bias required to deplete the semiconductor/insulator interface from excess charge carriers at \( V_{\text{GS}} = V_{\text{th}} \). Hence, the permittivities and thicknesses of the layers are useful in not only designing the SGT for a specific function, but also for troubleshooting a process when the extracted \( dV_{\text{DSAT1}}/dV_{\text{GS}} \) does not match \( \gamma \) [12]. In this case, the constituent layers predict a saturation coefficient of \( \gamma = 0.18 \), which is higher than the measured \( dV_{\text{DSAT1}}/dV_{\text{GS}} = 0.12 \) (Fig. 3d) when the field plate insulator \( FP_{\text{ins}} = 30 \text{ nm} \). The mismatch is comparatively small and could be due to higher charge density at the insulator interface [12], noting the onset of a negative differential resistance (negative slope) in the output characteristics. The higher charge density does not necessarily move the pinch-off point, which is determined by the constituent materials and structural geometry, but any excess carriers will prevent the full depletion of charges at the semiconductor-insulator interface.
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The depletion envelope at the source edge of Fig. 1a highlights this case. Fig 1b illustrates how the nature of the depletion envelope changes to ensure full pinch-off at $V_{DSAT1}$ can take place, while screening off the injection area in the source-gate overlap region. At low $FP_{in}$, it is likely the depletion envelope does not fully extend across the semiconductor width at the field plate edge, but as the $FP_{in}$ increases, the depletion envelope would also increase until the device can fully pinch-off.

![Graph](image_url)

**Fig. 2.** a) Transfer and b) output characteristics of the SGT without a field plate. There are no defining features of SGT behavior, as the device shows high transconductance and poor saturation. c) There is no emerging trend of increased drain current for longer $S$, but there is a reduction of drain current for longer $d$, which is a hallmark of field-effect transistor (FET) operation. Results such as these would only be indicative of a conventional Ohmic-contact thin-film transistor (TFT) rather than a contact-controlled SGT with a Schottky source.

According to a previous study in low-temperature polycrystalline Si (LTPS) Schottky barrier SGTs [37], the field plate should be designed to be as near to the active layer as possible to increase the electric field, thereby producing strong depletion in the semiconductor in the region close to the tip of the field plate. The choice of material will influence the overall effectiveness of the field relief, hence permittivity and quality will be important factors to consider. Essentially, the effective field plate relief $FP_{eff}$ will determine when and how the device saturates, described schematically in Fig. 4. Additionally, the extension $FP_{ext}$ should be long enough to allow this newly created depletion region to form away from the edge of the source electrode which is in contact with the semiconductor (Fig. 1c). This way, the $S$ region is shielded from any changes in potential as $V_{DS}$ is increased past $V_{DSAT1}$. The beneficial effects are twofold.

Firstly, the charge injected in the depletion region at the edge of the source is kept at a constant rate, irrespective of $V_{DS}$, as it is subjected to a practically constant electric field.

Secondly, the same depletion region keeps a similar two-dimensional shape at all $V_{DS}$ in saturation, and implicitly has no noticeable change in its resistance, therefore the potential distribution in the accumulation layer in the $S$ region remains the same, resulting in the same amount of current being obtained from the bulk of the source. Together, these manifest as an insensitivity of the saturated output curves to drain-source voltage changes.
To place these statements in context, we briefly review the operation of SGTs, as distinct from conventional TFTs, in which contact effects may be present but do not dominate as means of current control.

B. Field Plate Design and Charge Injection

In SGTs, there are two modes of charge injection. Mode I injection occurs via thermionic-field emission over the reverse-biased energy barrier at the source edge. This component of drain current is highly dependent on the applied electric field [44]. Hence, the drain-induced electric field contributes deleteriously to injection, in addition to the gate-induced field, by lowering the source barrier, qualitatively similar to drain-induced barrier lowering (DIBL) [45]. Therefore, when S is short (empirically less than 10-20 times the semiconductor thickness), Mode I injection dominates and lateral (drain-induced) field screening would be highly beneficial. Mode II current, on the other hand, is resistance or diffusion dominated, rather than being restricted by the barrier thermionic limit [40]. Charge injected along the bulk of S at the contact interface encounters the vertical resistance of the active layer, followed by the lateral resistance at the accumulated insulator interface. At each point along the source contact, a fraction of \( V_{DSAT1} \) is dropped resistively, until there is insufficient vertical potential difference across the semiconductor layer to promote charge injection. In high mobility materials, this can occur within the first few microns of S. In lower mobility or disordered semiconductors, this can be a few tens on microns. The point at which there is no further contribution of S towards overall drain current is known as \( S_{SAT} \) [13], [31]. It is clear then, that the introduction of a field relief structure would be beneficial regardless of dominant mode of operation in the SGT, by helping to keep the source region under a constant bias even as \( V_{DS} \) varies.

C. Drain-Field Design and Alternatives

According to the findings above, the thinner \( FP_{ins} \) with low permittivity insulators (e.g. \( \text{SiO}_2 \)) should produce the most favorable results (as investigated in a previous simulation-based study [37]), yet the opposite is witnessed here. One possible explanation is that trap-assisted tunnelling [46] could be occurring at the field plate edge, brought about by the high electric field in the region. Another explanation could be the existence of pinhole defects, due to quality of the field plate insulator.

Concerning the length of the field relief structure, the fabricated devices have a 5 \( \mu m \) (nominally 3 \( \mu m \)) field plate extension \( FP_{ext} \), with a suitable shielding effect. The study by Tu et al. [7] demonstrated saturation of \( dV_{DSAT1}/dV_{GS} \sim 0.4 \), which is far from \( \gamma = 0.025 \) expected from the 470 nm \( \text{SiO}_2/\text{SiN}_x \) gate insulator stack and 50 nm of a-IGZO used. The \( FP_{ext} = 230 \) nm used in their investigation appears sufficiently thin to be effective, as it is substantially thinner than the gate insulator. The \( FP_{ext} = 40 \) \( \mu m \) contributes to translating the field-plate induced pinch-off region far away from the edge of the source, as in [23]. However, as seen in the present report and in [37], a shorter \( FP_{ext} \) can be highly effective and may even increase the transconductance above threshold by allowing a stronger accumulation of the channel between the source and the drain at low \( V_{GS} \) [37]. Shortening the field plate structure means that the channel can also be much shorter [13], a desirable feature since the targeted application is pixel driving, where circuit footprint is valuable real-estate. Indeed, field relief contributes to augmenting the many benefits of SGTs as pixel drivers, as discussed in e.g. [18], [43], [47].

Drain relief in the form of a field plate is only one route to ensure that devices undergo hard saturation at \( V_{DSAT1} \). The following paragraphs discuss other design elements which promote SGT operation close to ideal.
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A complementary approach would be to ensure that the SGT operates in Mode II or low-field mode by designing $S$ to be comparatively long \([48]\).

Often, in research environments, shadow mask patterning of electrodes can be employed on doped Si/SiO$_2$ wafers, to take advantage of the highly doped Si and native thermal oxide as a global gate electrode and gate insulator, respectively. This technique, while useful for optimization of an active layer in TFTs, is quite restrictive when other design considerations, in particular geometric overlaps and electrode profile, are taken into consideration. Thus, especially when fabricating devices using shadow masks with coarse feature sizes, field relief is not entirely necessary, as $S$ is usually close to or above $S_{\text{SAT}}$. For example, in Zhang et al. [13], $S$ was 1200 $\mu$m, ensuring devices operated in Mode II, which dominates over any contribution from Mode I, even without field relief and sub-micron source-drain gaps. As such, a record intrinsic gain of $A_v = 29,000$ was achieved.

Another factor that plays a role in attaining high $A_v$ and the scale of $S_{\text{SAT}}$ is the height of the source energy barrier $\Phi_B$ [13], [31]. Higher $\Phi_B$ in the bulk likely reduces vertical potential drop in the semiconductor and reduces current density this way. The lower overall current (which ultimately passes through the depletion region at the edge of the source) means that it is easier to pinch off at the source, allowing for better electrostatic control of both mode I and, dominantly, mode II injection. Higher $\Phi_B$ is also associated with higher intrinsic gain [10], [20]. Aside from the long $S$ in Zhang et al. [13], it is likely that the energy barrier was significantly high to ensure flat saturation. In their study, the shadow mask was 2 mm wide, producing a drain current of 0.5 nA$\mu$m$^{-1}$ at $V_{GS} = 20$ V. For comparison, the device in Fig. 3d produces 11.5 nA$\mu$m$^{-1}$ at the same gate-source bias. Even though $S$ is 10 times shorter than [13], the device produces over 20 times more drain current. This is indicative of either a lower energy barrier or higher mobility a-IGZO layer.

Both devices (in Zhang et al. [13] and Fig. 3d) have a $dV_{GSSAT}/dV_{GS}$ approximates their respective predicted $\gamma$ value [12]. Although barrier inhomogeneities would lead to increased charge injection in regions with locally lower $\Phi_B$, this does not likely explain the higher current density achieved here, as one would expect a degradation of saturation sharpness. Generally lower barriers would produce an...
increase in charge carriers travelling through the accumulation layer and require an even higher $V_{DS}$ to fully pinch-off the source. The higher performance is likely a combination of improved current density or $\mu_{FE}$ of the a-IGZO layer. That being the case, unless there is a field plate incorporated on the devices reported here, the SGTs would fail to pinch off at the source and produce behavior of an Ohmic contact TFT [40], albeit with poorer performance chiefly in terms of on-current, due to the energy barrier.

Indeed, the presence of negative differential resistance (NDR) in the output characteristics (Fig. 3c and 3d) indicates the existence of traps states, which is not present in Zhang et al. [13], hence there is ample opportunity to improve the process and performance and uniformity (Fig. 5) of the devices reported here. It is worth noting that NDR has been observed in SGTs in several material systems [22], [43] and will be investigated separately. Certainly, should the NDR be eliminated from the output characteristics, the devices here may also achieve similar record high intrinsic gain values.

While use of shadow masks can simplify fabrication and accelerate iteration in a research environment, commercial applications would need to fit with standard manufacturing processes. In practice, shorter $S$ would be desired in order to optimize layout area. Thus, it is important to study devices with plausible dimensions, since, for the reasons outlined above, the behavior seen in “long-source” SGT is unlikely to translate identically to scaled devices.

4. Conclusion and Outlook

Interest in the source-gated transistor architecture has only recently grown, as researchers look towards developing these devices in contemporary technologies. Oxide semiconductors, however, are leading the way in terms of mobility within the growing family of emerging thin-film semiconductors. Yet, producing rectifying Schottky contacts in a thin-film transistor is not sufficient to guarantee source-gated device behavior. Even though the barrier exists, if charge density at the source is too great, early saturation is confounded. Among several strategies to mitigate drain field influence, source field plates appear to be an effective option for ensuring flat saturation, particularly for devices with short source-gate overlaps. Here, negative differential resistance (NDR) was observed, likely due to interfacial effects. Should NDR be suppressed, the field plate inclusion would lead to extremely flat output characteristics, with important applications in analog circuits for signal conditioning and conversion. However, high electric fields developed vertically between the semiconductor channel and the tip of the field plate mean that, in practice, extremely thin field-plate insulators are prone to tunnelling, and thus ineffective at performing the shielding function. Thus, in cases where high permittivity field plate insulators are used, there may be a need to increase the thickness to ensure no tunnelling occurs, depending on the quality of the oxide.

References


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