ADVANCED INTELLIGENT SYSTEMS
Open Access
www.advintellsyst.com

An Interface-Type Memristive Device for Artificial Synapse and Neuromorphic Computing

Sundar Kunwar, Zachary Jernigan, Zach Hughes, Chase Somodi, Michael D. Saccone, Francesco Caravelli, Pinku Roy, Di Zhang, Haiyan Wang, Quanxi Jia, Judith L. MacManus-Driscoll, Garrett Kenyon, Andrew Sornborger, Wanyi Nie, and Aiping Chen**

Interface-type (IT) metal/oxide Schottky memristive devices have attracted considerable attention over filament-type (FT) devices for neuromorphic computing because of their uniform, filament-free, and analog resistive switching (RS) characteristics. The most recent IT devices are based on oxygen ions and vacancies movement to alter interfacial Schottky barrier parameters and thereby control RS properties. However, the reliability and stability of these devices have been significantly affected by the undesired diffusion of ionic species. Herein, a reliable interface-dominated memristive device is demonstrated using a simple Au/Nb-doped $SrTiO_3$ (Nb:STO) Schottky structure. The Au/Nb:STO Schottky barrier modulation by charge trapping and detrapping is responsible for the analog resistive switching characteristics. Because of its interface-controlled RS, the proposed device shows low device-to-device, cell-to-cell, and cycle-to-cycle variability while maintaining high repeatability and stability during endurance and retention tests. Furthermore, the Au/Nb:STO IT memristive device exhibits versatile synaptic functions with an excellent uniformity, programmability, and reliability. A simulated artificial neural network with Au/Nb:STO synapses achieves a high recognition accuracy of 94.72% for large digit recognition from MNIST database. These results suggest that IT resistive switching can be potentially used for artificial synapses to build next-generation neuromorphic computing.

1. Introduction

A brain-inspired neuromorphic computer with superior computational capabilities and reduced energy consumption is viewed as a viable answer to next-generation computing technology's speed and energy requirements.[1,2] Digital computers are built on von Neumann architecture, which consists of a separate processing and memory units connected by a communication bus. Thus, continuous data transfer between processor and memory units is required, resulting in a significant power loss and data transfer delay during computational operation, known as the von Neumann bottleneck. This has posed significant challenges for large-scale data processing in the Internet of Things, artificial intelligence applications, artificial neural networks, and machine learning systems.[3,4] Until recently, the semiconductor industry has been evolving according to Moore's law, which describes how the billions of complementary metal oxide semiconductor (CMOS) transistors that are integrated into a small chip scale exponentially to continuously enhance the

S. Kunwar, Z. Jernigan, Z. Hughes, C. Somodi, P. Roy, D. Zhang, W. Nie, A. Chen
Center for Integrated Nanotechnologies (CINT)
Los Alamos National Laboratory
Los Alamos, NM 87545, USA
E-mail: sundar@lanl.gov; apchen@lanl.gov

M. D. Saccone, F. Caravelli
T-4
Los Alamos National Laboratory
Los Alamos, NM 87545, USA

The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/aisy.202300035.

© 2023 The Authors. Advanced Intelligent Systems published by Wiley-VCH GmbH. This is an open access article under the terms of the Creative Commons Attribution License, which permits use, distribution and reproduction in any medium, provided the original work is properly cited.

DOI: 10.1002/aisy.202300035

H. Wang
School of Materials Engineering
Purdue University
West Lafayette, IN 47907, USA

P. Roy, Q. Jia
Department of Materials Design and Innovation
University at Buffalo - The State University of New York
Buffalo, NY 14260, USA

J. L. MacManus-Driscoll
Department of Materials Science and Metallurgy
University of Cambridge
27 Charles Babbage Road, Cambridge CB3 0FS, UK

G. Kenyon, A. Sornborger
CCS-3
Los Alamos National Laboratory
Los Alamos, NM 87545, USA

computing power and downscale of the computer size.[5] However, the ultrahigh integration of CMOS transistors is approaching its practical limits because of exponential increase in leakage current with the reduction of source-drain channel widths, high power density per unit area, and rapid increase in fabrication costs.[6] In this regard, a brain-inspired neuromorphic computing architecture with adaptive learning ability, massive parallelism, high speed, and energy-efficient operation may be crucial for achieving the challenges of speed and energy in next-generation computing technologies.[3,7,8]

In recent years, emerging memristive switching devices have been a subject of interest for resistive random access memory (ReRAM) and neuromorphic computing, because of their low power consumption, fast switching speed, and high-density device integration.[8–10] Memristors are two terminal devices that have a dielectric (switching) layer sandwiched between top and bottom electrodes. Such a device is not only capable of storing information, but it can also emulate biological synaptic functions, and thus it can serve as a fundamental hardware element in the neuromorphic computing.[8,11] In a biological synapse, two neurons (presynaptic and postsynaptic neurons) are connected by a synapse, and the analog reconfiguration of synaptic plasticity (connection strength) due to synaptic spikes is key to learning and memory in a human brain.[12–14] Similarly, a two-terminal memristor can structurally and functionally mimic biological synaptic features such as the conductance (G), corresponding to a synaptic weight, which is updated based on the history of its input potential.[15–18] Despite the wide range of advantages of memristive devices in neuromorphic computing, there are still several challenges at the device level such as poor stability, high variability, poor retention, and endurance.[19]

So far, various types of RS materials including oxides, polymers, organic, and 2D materials have been reported for the artificial synapse and their operation mechanisms can be broadly classified as follows: redox (TiO_x, HfO_x, TaO_x, $SrTiO_x$, $SrFeO_x$), phase change ($Ag_4In_3Sb_{67}Te_{26}$, $Ge_2Sb_2Te_5$), and magnetic and ferroelectric ($La_{0.67}Sr_{0.33}MnO_3$, HfO_x, $BiFeO_3$, $BaTiO_3$).[20–26] Among these, the redox or conductive filament (CF) and phase change RS memory generally require filament formation/rupturing and melting/quenching process, respectively.[18,27] Because of the stochastic and abrupt nature of these processes, large device-to-device and cycle-to-cycle variations have frequently been observed.[2,19] This further results in wide variations in the set/reset voltage, on/off ratio, endurance, retention and switching speed, and therefore, hindering their practical realization.[28–31] More recently, significant attention has been given to interface-type (IT) RS devices, which exhibit uniform and nondestructive resistance change induced by an interface Schottky barrier modulation.[29,32,33] Furthermore, IT switching is filament-free, homogeneous, and consumes low energy, making it a promising alternative for neuromorphic applications.[9,32] The metal/oxide Schottky interface is altered by oxygen vacancy (V_o) drift or electron trapping/detrapping effects at the interface, which is analogous to synaptic weight updated by the charged neurotransmitters (Ca^{2+}, or K^+ ions) in a biological synapse. Thus, IT memristive devices can emulate the synaptic plasticity by changing conductance based on the Schottky barrier parameters. Most of the IT devices studied thus far have utilized metal/thin oxide layers Schottky interface where the migration of V_o is exploited to achieve the desired resistance state. However, controlling V_o migration in oxides is challenging as it can be influenced by multiple factors including film thickness, defect concentration, temperature, and grain boundaries, resulting in device reliability and uniformity issues.

In this work, a simple Au/Nb:STO memristive device with reliable IT switching characteristics is explored for biological synaptic function. Different from other IT devices where switching mechanism is mostly driven by V_o migration in oxide layers, the proposed IT device is fully interface controlled and takes advantage of charge trapping and detrapping at the Au/Nb:STO interface. The Au/Nb:STO interface plays critical role in determining the resistance states of the device in which an external voltage stimulation inherently alters Schottky barrier parameters due to the charge trapping and detrapping effects. The switching mechanism of such systems has been explored carefully.[34–36] Our previous work has shown that protons-assisted electron trapping and detrapping are likely responsible for the switching at metal/Nb:STO interfaces.[34] By altering voltage polarity, amplitude, and duration, a multilevel nonvolatile analog resistance window is demonstrated. The proposed artificial synapse accurately emulates various critical functions of biological synapse, including paired-pulse facilitation (PPF), short-term potentiation/depression (STP/STD), long-term potentiation/depression (LTP/LTD), and spike timing dependent plasticity (STDP). Furthermore, the Au/Nb:STO device exhibits high stability, low variability, and continuous conductance change during LTP and LTD cycles. The artificial neural network simulated with such synapses leads to image recognition accuracy of 94.72% for handwritten digits from MNIST. These characteristics are superior to previously reported CF-based artificial synapses and thus we have identified interface-controlled Au/Nb:STO memristive device as a promising candidate for future neuromorphic applications.

2. Results and Discussions

Figure 1a,b depicts a schematic of the Au/Nb:STO memristive device and a biological synapse that the device emulates. The biological synapse is made up of presynaptic and postsynaptic neurons connected at the synaptic cleft whose weight changes depending on the transmission of neurotransmitters in response to correlated pre- and postsynaptic spikes. This process is similar to that of the Au/Nb:STO memristive device, in which the flow of charge carriers through the device varies depending upon the interface resistance. To demonstrate the synaptic performance of the Au/Nb:STO, RS properties should first be thoroughly explored. Figure 1c shows a typical current–voltage (I–V) characteristic of an Au/Nb:STO device measured with voltage sweep of $0\,V \rightarrow +3\,V \rightarrow -6\,V \rightarrow 0\,V$. A bipolar RS was observed as the device was set (on), i.e., HRS to LRS at $+3$ V and reset (off), i.e., LRS to HRS at -6 V. The on and off transitions occurred at positive and negative voltages, respectively, without an electroforming process, which is a typical characteristic of interface-type RS devices.[35,37–39] The Au/Nb:STO device exhibits a high on/off ratio of $\approx 10^5$ at $+0.4$ V, indicating a large memory window for potential multilevel data storage applications. To confirm the device reliability, different Au/Nb:STO devices were prepared and their I–V characteristics along with the on/off ratio were

© 2023 The Authors. Advanced Intelligent Systems published by Wiley-VCH GmbH

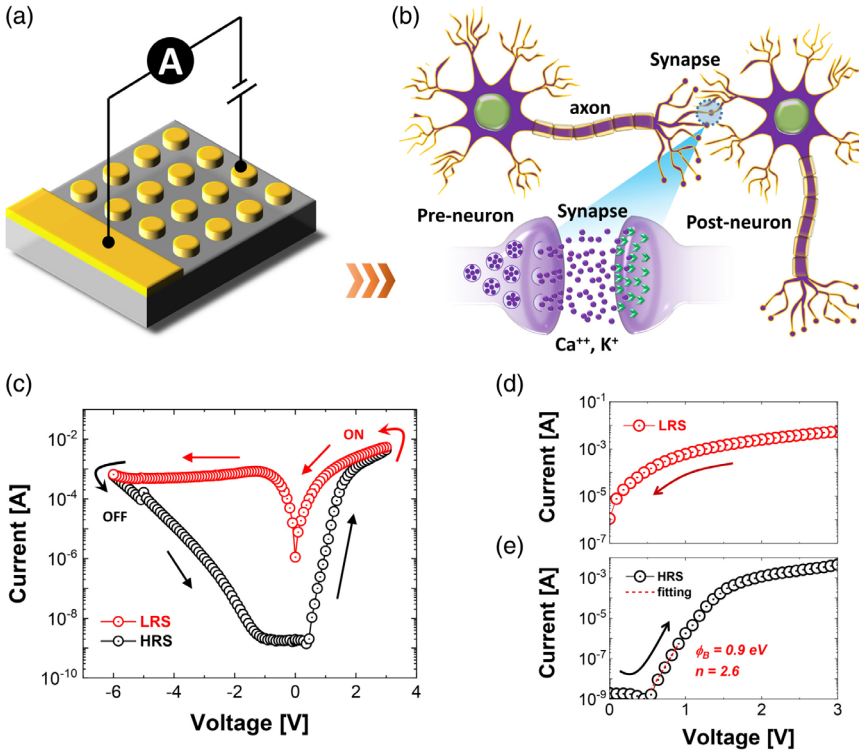


Figure 1. a) Schematic of Au/Nb:STO/Au memristive device with Au disks as active electrodes and Au bar as a reference electrode. b) The schematic diagram of a biological synapse that can be emulated by Au/Nb:STO/Au device. c) Current–Voltage (*I–V*) characteristic of the device with a voltage sweeping sequence of 0 V → +3 V → 0 V → −6 V → 0 V. d,e) Low-resistance state (LRS) and high-resistance state (HRS) of the device under positive bias. The dotted lines show the fitting of *I–V* curve in the low-voltage region.

analyzed in Figure S1, Supporting Information. All devices exhibited large *I–V* hysteresis with device-to-device, cell-to-cell (same device), and cycle-to-cycle (same cell) on/off ratio variabilities of ≈40, 32, and 9.7%, respectively. This suggests that the Au/Nb:STO IT memristive devices possess good reproducibility, reliability, and stability as compared to FT memristors. These characteristics make the device suitable for artificial synapses and neuromorphic applications.[40–42] The RS effect in our device is mediated by charge trapping/detrapping and a corresponding modulation in Schottky barrier parameters (i.e., barrier height, Φ_B and depletion width, W_d) at the Au/Nb:STO interface.[35,37] A single-crystal Nb:STO substrate was intentionally chosen to mitigate undesired effects from defects, grain boundaries, and oxygen vacancies migration. However, localized surface trap states such as lattice distortion and point defects can be generated during electrode deposition, which would facilitate the charge trapping/detrapping at the Au/Nb:STO interface. The low forward voltage region under the HRS was fitted based on Schottky emission theory.[35] The extracted value for Φ_B and ideality factor (n) under the HRS were 0.9 eV and 2.6, respectively, which suggests that the voltage-dependent charge trapping/detrapping process controls the RS at the Au/Nb:STO interface.[36,37] A detailed study on the RS mechanisms in the Au/Nb:STO interface-type device is presented in our previous work, which explored the critical roles of protons (from moisture) in charge trapping/detrapping and Schottky barrier modulation.[34]

Figure 2 presents analog RS characteristics of the Au/Nb:STO device under different set/reset voltage ranges. By changing the voltage sweep range between 1 and 3 V for set and between −2 and −6 V for reset, different shapes/sizes of *I–V* hysteresis were realized, as shown in Figure 2a. Despite different voltage sweep ranges, the device sets to the LRS at positive voltage and resets to the HRS at negative voltage. Furthermore, the Au/Nb:STO device exhibited good stability at each set and reset voltage range as confirmed by 50 consecutive *I–V* loop measurements. It was also observed that *I–V* hysteresis was gradually enlarged with increased set/reset voltages, resulting in higher on/off ratios. Specifically, the LRS current was significantly increased while the HRS current was slightly reduced with increased set/reset voltages. This process can be correlated to the extent of charge trapping/detrapping at the Au/Nb:STO Schottky interface based on the magnitude of applied voltage. Such analog and stable set/reset operation of the Au/Nb:STO IT device lay a foundation for the artificial synapse and neuromorphic computing applications. The current ratio between HRS and LRS at fixed −0.2 V readout is extracted in Figure 2b, which clearly shows the multilevel storage ability of Au/Nb:STO based on the amplitude of set/reset voltages. Furthermore, we analyzed the reliability of the device with an endurance test under different read voltages (−0.2, −0.4, and −1 V) and fixed set/reset at +3 V/−6 V, as shown in Figure 2c. A stable on/off current ratio of 10^3, 10^4, and 10^5 was achieved (>100 cycles) at read voltages of −0.2, −0.4, −1 V, respectively. Similarly, a readout operation can be

© 2023 The Authors. Advanced Intelligent Systems published by Wiley-VCH GmbH

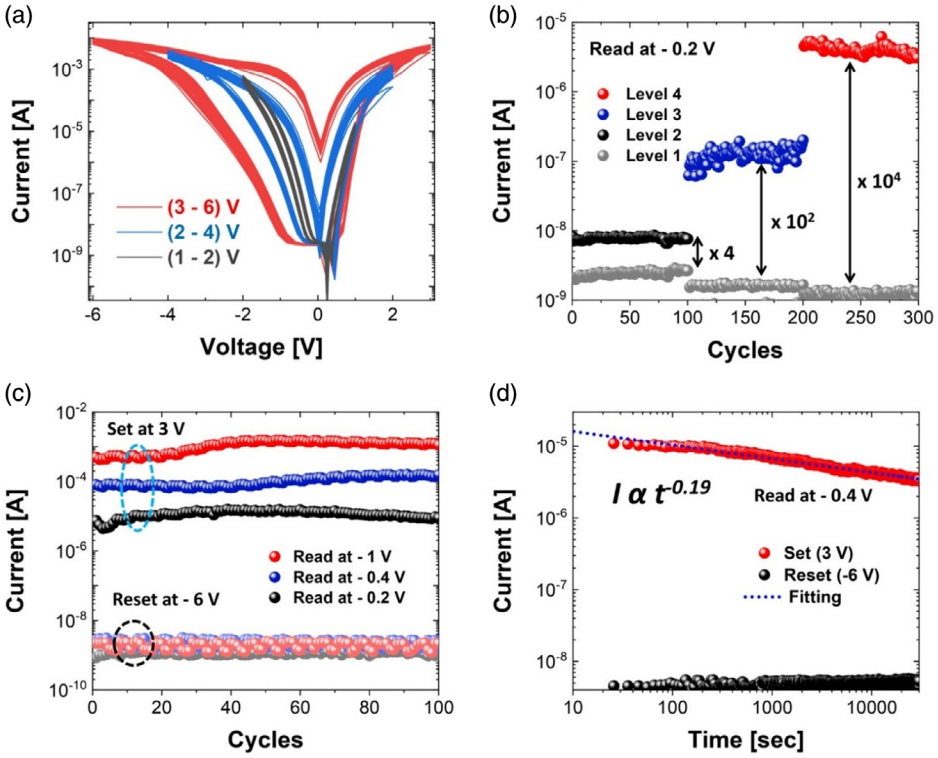


Figure 2. a) Fifty consecutive *I–V* curves of the Au/Nb:STO memristive device with different set and reset voltages. b) Multilevel current measured at a fixed voltage of −0.2 V with different set and reset voltages shown in (a). c) Multilevel current measured at different read voltages (−0.2, −0.4, and −1 V) with fixed set and reset voltages at 3 and −6 V, respectively. d) Retention curve of the device at −0.4 V read voltage and fixed set/reset at 3/−6 V.

performed with a positive read voltage (0.2 V), as shown in Figure S2, Supporting Information. No obvious differences were observed in the HRS and LSR current distributions with ±0.2 V read voltages. To further verify the stability of the device, an endurance measurement was carried out at −0.4 V for $>10^4$ cycles, as shown in Figure S3, Supporting Information. Although the LRS current was slightly decreased, the on/off ratio of $>10^4$ was still maintained after more than 10 000 consecutive read/write cycles. Figure 2d and S4, Supporting Information, show the retention properties of the device in which the current versus time *(I–t)* curves were measured at ±0.4 V with an interval of 1 s after set/reset at 3 V/−6 V, respectively. The HRS current was found to be generally stable even after 30 000 s while the LRS current gradually decayed over time. The LRS current with respect to time followed a power law with $I(t) \alpha t^{-0.19}$ at −0.4 V and $I(t) \alpha t^{-0.06}$ at 0.4 V.[36] This minor current decay may be due to the progressive trapping of charges which were detrapped during the set process.[34] As the negative read voltage promotes charge trapping process, LRS current decay was much faster with −0.4 V readout than with +0.4 V readout. The device maintained a high on/off ratio of $\approx 10^4$ at −0.4 V and 10^5 at 0.4 V. The performance of the Au/Nb:STO IT devices was comparable or even better than that of some other metal oxide-based FT memristors.[41,43] From these experiments, it was confirmed that the Au/Nb:STO device offered dynamic resistance (conductance) as well as partially volatile/nonvolatile memory and thus can be used to emulate biological synaptic functions. Different from memory device applications which often require nonvolatile characteristics, biological synapses exhibit some volatility. Long decay times (as observed in Au/Nb:STO) are critical for long-term memory in the brain.

Figure 3 presents the synaptic plasticity of the Au/Nb:STO memristive device, which involves strengthening or weakening of the conductance (synaptic weight) in response to training pulses. Similar to biological synapses, whose synaptic weight changes due to the flow of neurotransmitters (Ca^{2+} ions) between two neurons in response to patterns of pre- and postsynaptic spikes, our device also changed its postsynaptic current/conductivity by voltage-induced charge migration. To explore such synaptic behavior in the Au/Nb:STO, we performed systematic *I–V* measurements under sweep and pulsed modes. As shown in Figure 3a,b, the device current successively increases and decreases with repeated voltage sweep of 0 V→ +1 V and 0 V→ −1 V, respectively. Corresponding current and voltage versus time *(I–t, V–t)* plots are shown in Figure 3c,d to demonstrate the change in weight with 10 consecutive voltage sweep cycles. An obvious increase (decrease) in current maxima is observed after implementing consecutive positive (negative) voltage sweeps, indicating subsequent changes in the conductance/weight of the device. Such analog behavior of the Au/Nb:STO device is essential to emulate the biological synaptic functions. Furthermore, the device weight can be altered by applying pulsed voltage signals. As shown in Figure 3e,f, the current of the device was successively increased or decreased by 50 consecutive voltage pulses (10 ms pulse width) of 1.5 and −1.5 V, respectively. These characteristics of the device can be associated with long-term

© 2023 The Authors. Advanced Intelligent Systems published by Wiley-VCH GmbH

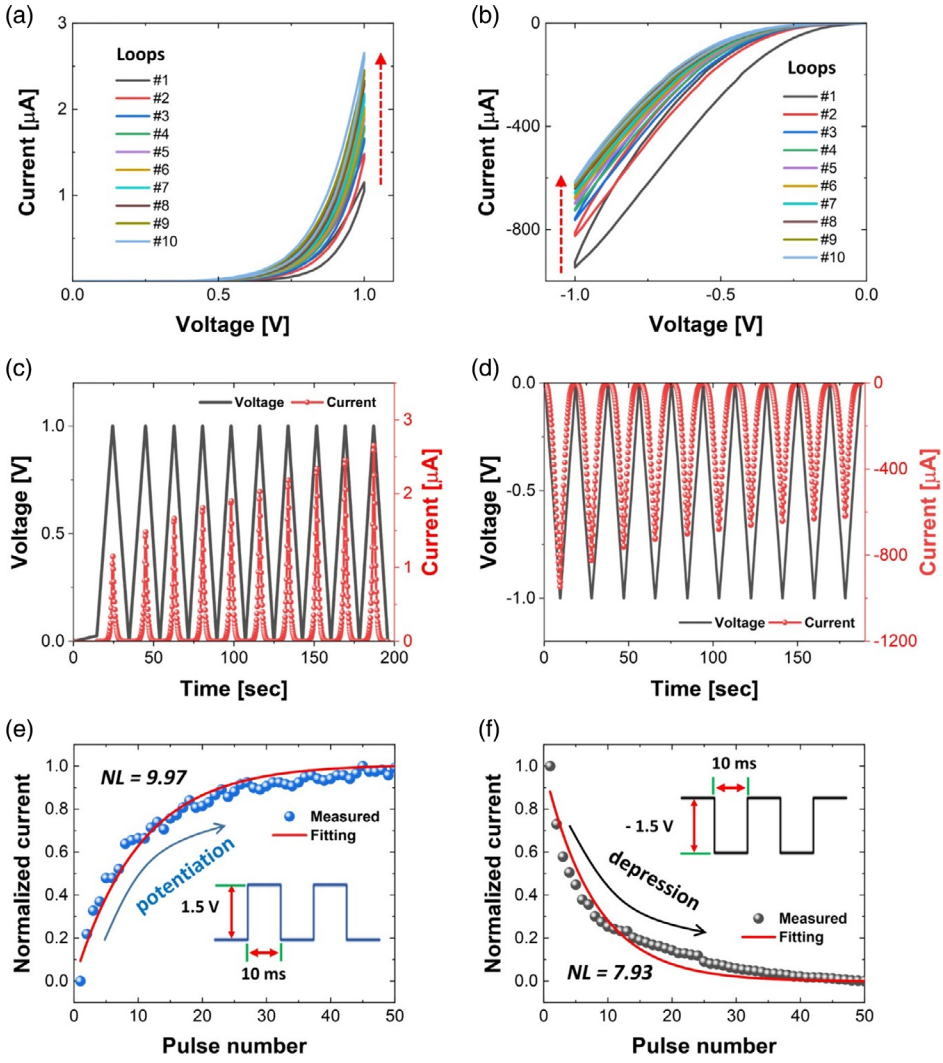


Figure 3. Memristive characteristics of the Au/Nb:STO device measured under different voltage sweeps and write pulses. a,b) Ten consecutive *I–V* loops with voltage sweeps in positive (0 V → 1 V → 0 V) and negative (0 V → −1 V → 0 V) directions, respectively. c,d) Current and voltage versus time (*I–V–t*) characteristics from (a) and (b). e,f) Normalized current versus the number of voltage pulses showing potentiation and depression behavior of the Au/Nb:STO at 1.5 and −1.5 V pulse of 10 ms, respectively.

potentiation (LTP) and long-term depression (LTD) in the biological synapse. Nonlinear current behavior with the number of pulses (P) during potentiation (I_p) and depression (I_d) can be modeled by the following relations[44,45]

$$I_p = I_{min} + \left(\frac{I_{max} - I_{min}}{1 - e^{\frac{-P_{max}}{A}}}\right)\left(1 - e^{\left(\frac{-P}{A}\right)}\right) \quad (1)$$

$$I_d = I_{max} - \left(\frac{I_{max} - I_{min}}{1 - e^{\frac{-P_{max}}{A}}}\right)\left(1 - e^{\left(\frac{P - P_{max}}{A}\right)}\right) \quad (2)$$

Where, I_{max}, I_{min}, P_{max}, and A are the maximum current, minimum current, and maximum number of pulses (resp.) required to switch the device between the minimum and maximum conductance state and A is the fitting parameter that controls its nonlinear behavior. The extracted nonlinearity (NL) values for the potentiation and depression curves are 9.97 and 7.93, respectively.

We further investigated dynamic weight update in our device based on postsynaptic voltage amplitude and duration. As shown in **Figure 4**a,b, the device current at 0.8 V readout was gradually increased and then tended to saturate with repetitive stimulation of constant voltage pulses. Meanwhile, with increasing amplitude of voltage pulses from 2 to 3.5 V and duration from 2 to 10 ms, the device current range was also increased. In general, the current increment occurred rapidly for first few write pulses and then mildly increased for a higher number of training pulses, which is similar to the synaptic response in the form of LTP under the potentiating stimulus. These features of our device mimic the synaptic weight change in the biological neurons depending upon the amplitude and duration of stimulation pulses. Moreover, the Au/Nb:STO memristive device has been

© 2023 The Authors. Advanced Intelligent Systems published by Wiley-VCH GmbH

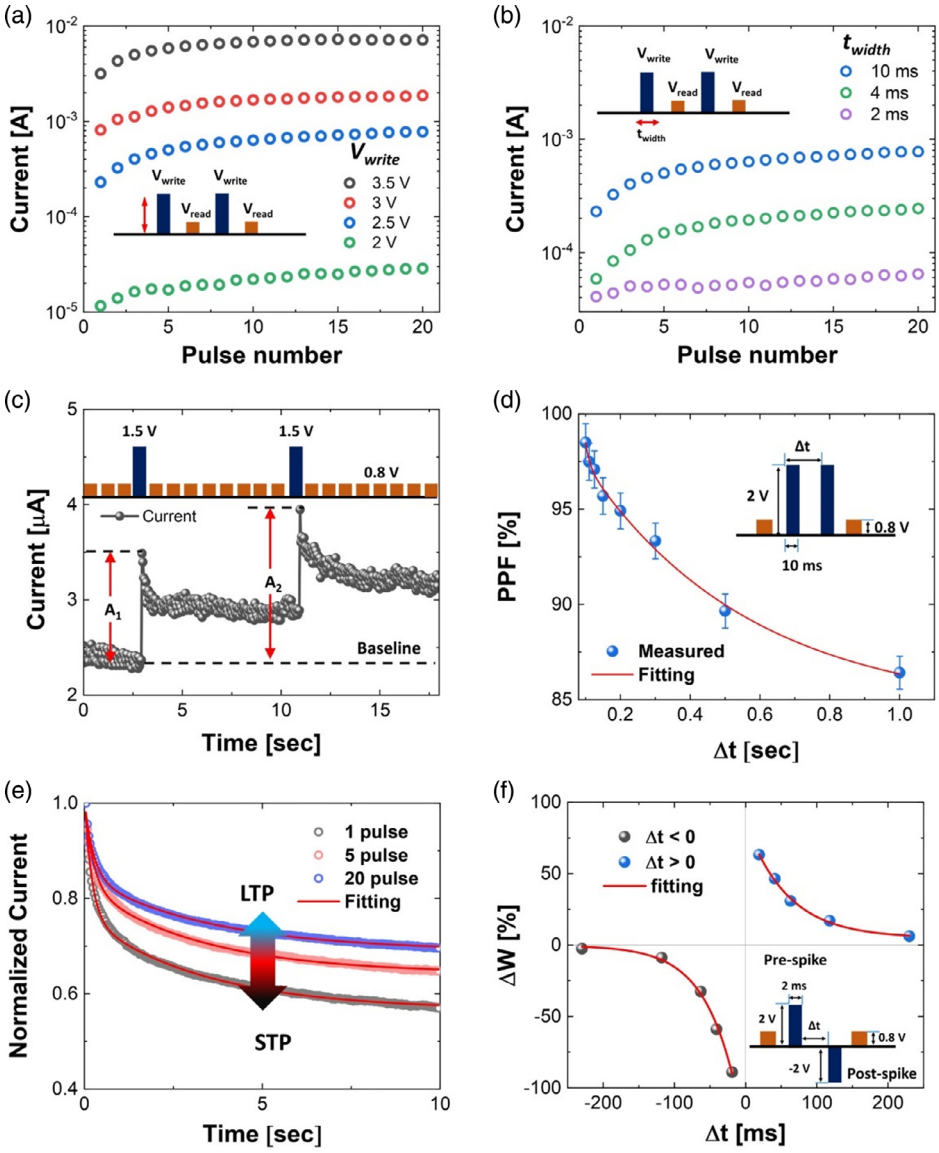


Figure 4. a) Evolution of current with different amplitude of write voltages (2 to 3.5 V of 4 ms pulse width). b) Current evolution with write voltage pulse of 2 V and varying width between 2 and 10 ms. The read voltage in (a) and (b) is 0.8 V. c) Excitatory postsynaptic current (EPSC) stimulated by a pair of 1.5 V/4 ms pulses. d) Paired-pulse facilitation (PPF) index with respect to the time interval ($\Delta t = t_{second} – t_{first}$) between voltage spikes of 2 V. e) EPSC decay curves measured after applying different number of 2.5 V/4 ms pulses. The inset shows implementation of paired voltage spikes and read voltages. f) Synaptic weight (ΔW) change as a function of pre- and postspike timing (Δt). The inset shows the prespike, postspike, and readout voltage.

explored to emulate more complicated biological synaptic plasticity such as excitatory postsynaptic current (EPSC), paired-pulse facilitation (PPF), and spike timing dependent plasticity (STDP). In a biological synapse, an EPSC denotes a shot-term plasticity (STP) caused by the influx of Ca^{2+} ions by the stimulation of a presynaptic spike.[13] An EPSC manifests as an enhancement in the amplitude when two presynaptic spikes are rapidly evoked. As shown in Figure 4c, the second EPSC current amplitude (A_2) was higher than the first EPSC current amplitude (A_1) when two 1.5 V pulses were applied in quick succession to the Au/Nb:STO device. Such synaptic function is also known as PPF, which is the basis for temporal information encoding of auditory or visual signals.[46] The value of the PPF index is directly related to the time interval of the two presynaptic spikes. To mimic PPF function from our device, two successive pulses with fixed amplitude and width were applied while the interval between the two spikes was increased from 0.1 to 1 s. Read pulses of 0.8 V were set before and after the two presynaptic spikes, as shown in the inset of Figure 4d. The read voltage was chosen in such a way that it would not affect the device conductance. The PPF index as a function of time interval ($\Delta t = t_2 – t_1$) is shown in Figure 4d. Weight change with respect to paired voltage pulses was calculated based on the equation[43]

© 2023 The Authors. Advanced Intelligent Systems published by Wiley-VCH GmbH

$$\text{PPF}\,[\%] = \frac{A_2 - A_1}{A_1} \times 100\,\% \tag{3}$$

Where, A_1 and A_2 are current amplitudes before and after the paired pulse stimulation, respectively. The PPF index decreases with increase in the pulse time interval, which is similar to the PPF in biological synapse. The dependence of PPF index on Δt can be well-fitted by the double-exponential function[47]

$$\text{PPF}[\Delta t] = A_1\, e^{-\frac{\Delta t}{\tau_1}} + A_2\, e^{-\frac{\Delta t}{\tau_2}} + Y_o \tag{4}$$

Where, τ_1 and τ_2 are the fast and slow relaxation time constants, respectively. τ_1 and τ_2 for our device were found to be 13 and 475 ms. The relaxation time constant in our Au/Nb:STO system is similar to the brain.[48,49]

Figure 4e shows the EPSC with different numbers of training pulses. The EPSC decay rate is significantly reduced with increased training pulses. Such behavior is associated with learning and longer memory retention (STP to LTP) with frequently repeated training in biological synapses.[50] The temporal current behavior in response to different numbers of training pulses was well-fitted by Equation (4). τ_1 and τ_2 were successively increased from 0.2 to 0.25 s and from 3.31 to 3.53 s as the number of training pulses was increased from 1 to 20, respectively. The increase in relaxation time constants with training pulses indicates occurrence of LTP from STP. Furthermore, the Au/Nb:STO IT device has been used to emulate STDP, which is a basis for asymmetric Hebbian learning rule.[14,51] In STDP, the weight of a synapse will be affected by the relative time difference ($\Delta t_{\text{post-pre}} = t_{\text{post}} - t_{\text{pre}}$) between the presynaptic and postsynaptic spikes. Specifically, if the presynaptic spike arrives before a postsynaptic spike ($\Delta t_{\text{post-pre}} > 0$), the synaptic weight will increase and otherwise the weight will decrease. To emulate STDP in the Au/Nb:STO device, the Au disk electrode was defined as the presynaptic neuron whereas the Au bar was defined as the postsynaptic neuron. The measurement scheme for STDP is shown in the inset of Figure 4f where 0.8 V read pulse was set before and after the synaptic spikes and the weight change (ΔW) was calculated based on Equation (5). Based on the time difference between the presynaptic and postsynaptic spikes, the synaptic weight update is summarized in Figure 4f. When $\Delta t_{\text{post-pre}}$ is positive (negative), the weight increased (decreased), confirming the STDP behavior of the Au/Nb:STO IT memristive device. In addition, the synaptic weight change (ΔW) was studied with respect to the Δt between pre- and postspikes, which showed a decreasing weight trend with increased time interval that can be fitted by the equation.[52]

$$\Delta W = W_o + Ae^{\left(-\frac{\Delta t}{\tau}\right)} \tag{5}$$

Figure 5 shows LTP and LTD properties of the Au/Nb:STO IT memristive device based on different training pulse schemes. The LTP and LTD are important synaptic functions for bidirectional weight update in neuromorphic computing. The LTP in our device was characterized either by a train of positive pulses with increasing amplitudes or by the train of fixed positive pulses. Similarly, LTD was realized with negative voltage pulses. Three types of training pulse sequence were implemented, as shown in Figure 5a,c,e. For reading, a fixed voltage of 0.8 V was used that induced as limited conductance change in the device. Figure 5a shows the type I training sequence with increasing voltage pulses from 0.8 to 2.45 V for potentiation and decreasing voltage pulses from −0.1 to −1.8 V for depression. The current gradually increased with the positive voltage train and then decreased with the negative voltage train, as shown in Figure 5b,c, shows the type II (1 to 3 V for potentiation and fixed −0.5 V for depression) and Figure 5e shows type III (fixed 1.6 V for potentiation and −1 V for depression) training pulse configurations. Figure 5d,f shows the corresponding current response. Although all three types of training sequences showed potentiation/depression process, it has been reported that linearity has a strong influence on learning accuracy for neuromorphic computing.[53] Furthermore, the potentiation/depression processes were cyclically reproduced without significant cycle-to-cycle variation, as shown in Figure S5–S7, Supporting Information. Minimal cycle-to-cycle variation in potentiation/depression is desired for high learning efficiency in the neuromorphic computing. Thus, Au/Nb:STO IT memristive devices serve as an excellent candidate for practical applications.[54]

Finally, the device response to various training pulses was implemented in CrossSim to determine how linearity of the conduction response of a crossbar array of such devices affects the performance for MNIST digital number recognition. CrossSim uses the backpropagation (i.e., gradient descent computation) algorithm to train the neural network.[55] Every image of the input MNIST digits was chopped to a 28×28 pixel array which feeds the 784 input neurons, as shown in **Figure 6**a. The 10 output neurons correspond to the 10 output digits. The realization of such a neural network requires two crossbar arrays, as shown in Figure 6b. Response data for over 80 set/reset cycles was used in CrossSim to better represent the device's stochastic switching nature. Among different training schemes implemented in our Au/Nb:STO device, the type I training scheme provided the best linearity and symmetry for LTP/LTD. Thus, the LTP/LTD based on type I training was chosen for creating artificial neural network and related detail analysis. The ΔG versus G plots for potentiation and depression cycles for type I response data can be seen in Figure 6c and conduction responses for the other two training configurations are shown in Figure S10, Supporting Information. From these graphs, it appears that the device has a tight range of ΔG values as G is varied in response with type I potentiation/depression cycles. Although it is often believed that the linearity of the conduction response plays a critical role on prediction accuracy, the qualitative correlation between conduction response and prediction accuracy is largely unexplored. Figure 6d shows the recognition accuracy of 28×28 pixel MNIST digital images with type I training configurations, which is compared with the numerical model. After training the simulated crossbar array for 25 epochs, the Au/Nb:STO synapse crossbar array attained a prediction accuracy of 94.72% whereas the numerical model with ideal linear potentiation/depression response showed an accuracy of 98.2%. A confusion matrix for the 25th training epoch was generated for the type I potentiation/depression response, as shown in Figure 6e. The confusion matrix compares the actual value of the digit to the predicted value of the digit. A well-trained neural network should produce a diagonal line in the confusion matrix, representing high recognition accuracy, as shown in the Figure 6e. In addition, a smaller ($64 \times 36 \times 10$ neurons) neural network was simulated for the

© 2023 The Authors. Advanced Intelligent Systems published by Wiley-VCH GmbH

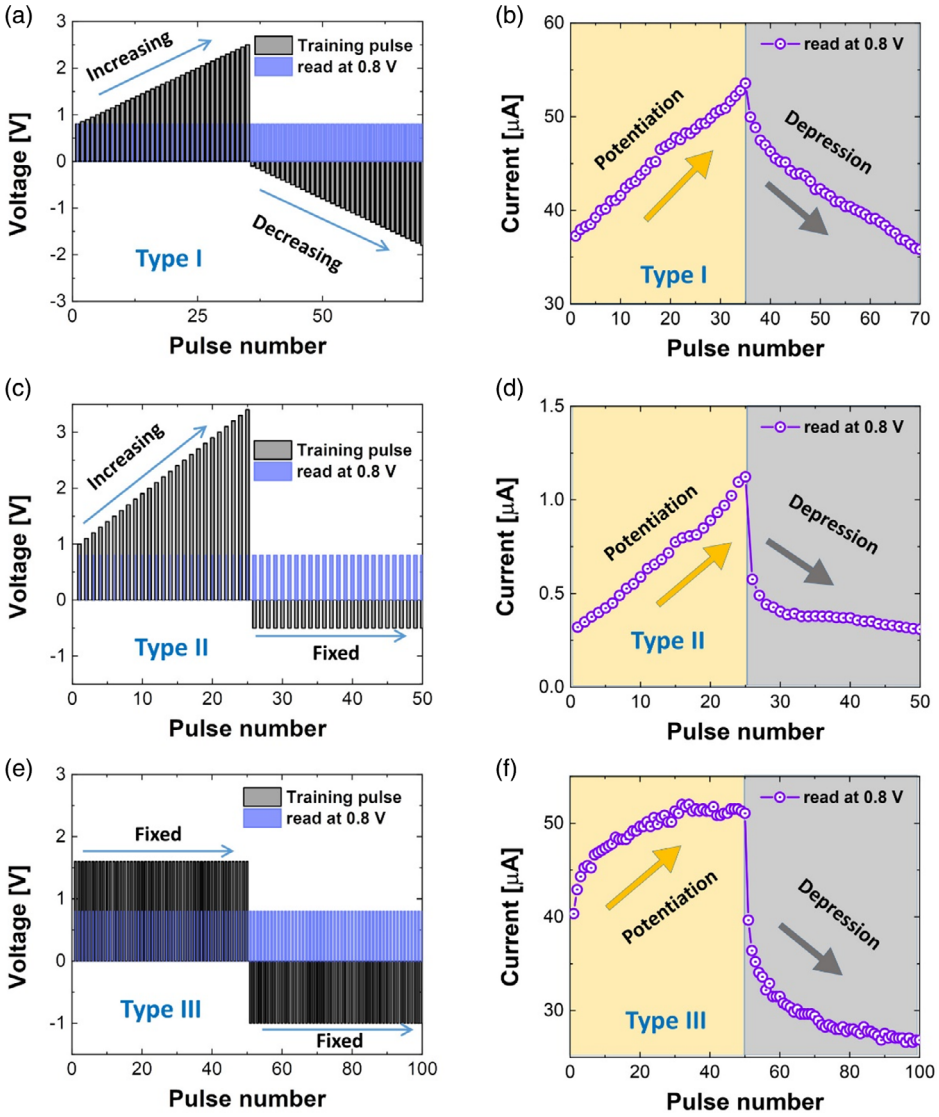


Figure 5. Tuning the learning behavior of Au/Nb:STO device through training pulse modulation. The voltage pulse width is fixed at 40 ms. a) Increasing voltage pulse train from 0.8 to 2.45 V for potentiation and from −0.1 to −1.8 V for depression. b) Corresponding change in potentiation and depression current. c) Increasing voltage pulse train from 1 to 3.4 V for potentiation and fixed −0.5 V for depression. d) Corresponding current trend. e) Fixed voltage pulse train of 1.6 V for potentiation and −1 V for depression. f) Corresponding current trend. The readout voltage is fixed at 0.8 V. The potentiation/depression sequence in (b), (d), and (f) are indicated as type I, II, and III hereafter.

recognition of an 8×8 pixel image as shown in Figure S11, Supporting Information. After training the simulated crossbar array with 8×8 pixel images for 25 epochs, the Au/Nb:STO synapse crossbar array attained a recognition accuracy of 94.71% whereas the ideal numeric model obtained accuracy of 96.16%, as shown in Figure S11c, Supporting Information. Similarly, type II and type III potentiation/depression cycles with higher nonlinearity exhibit recognition accuracies of 93.66 and 92.94% at 25 epochs, respectively. The image recognition accuracy varied within 1.7% under different potentiation/depression conditions, indicating that the device can be adapted to diverse programming pulses. It should also be mentioned that the performance of the Au/Nb:STO synapse-based artificial neural network compared favorably or even better than that of CF-RRAM,[56–58] and I-RRAM memristors,[32,59] which can be correlated to the well-controlled device resistance state change based on the voltage-dependent charge trapping and detrapping at the Schottky interface. Furthermore, **Table 1** summarizes the performance parameters of a recently reported IT memristive devices-based artificial synapse, where the RS is mainly contributed by the diffusion of V_o at the Schottky interface. Controlling V_o migration in oxides could be challenging. Thus, an interface-dominated charge trapping/detrapping phenomena could provide alternative solutions to improve the stability, uniformity, and reliability of the interface-type memristive devices and related applications. Comparing the performance parameters with various IT memristive devices, the Au/Nb:STO device proposed in this work stands out as a superior candidate for neuromorphic

© 2023 The Authors. Advanced Intelligent Systems published by Wiley-VCH GmbH

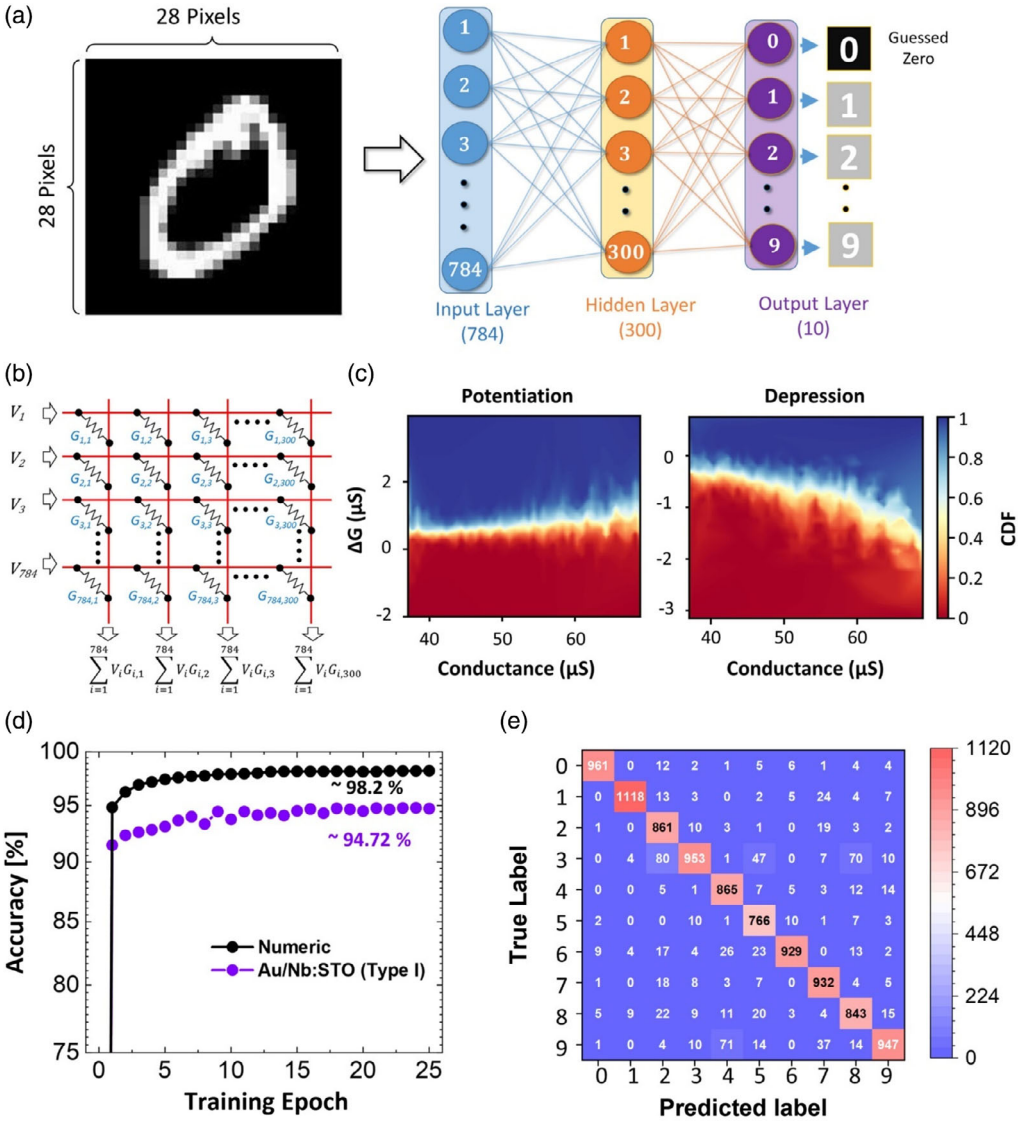


Figure 6. a) Input image (28 × 28 pixel) for digit 0 and an illustration of a neural network crossbar simulator with 784 input layers, 300 hidden layers, and 10 output layers. b) Schematic of a memristor crossbar array used for simulating neural network. c) Conductance variation (ΔG) versus G plots for potentiation and depression with respect to type I training sequence of the Au/Nb:STO device. d) Recognition accuracy of the simulated crossbar array based on type I training sequence compared with the ideal numeric model. e) Confusion matrix of the 25th epoch.

computing applications with room for further improvements such as smaller device size, larger device array, and CMOS integration. The studied phenomenology in Au/Nb:STO devices also opens the possibility of studying experimental applications of memristive-induced tunneling mechanisms, with applications to gradient descent.[60,61]

3. Conclusion

In summary, the RS properties of the Au/Nb:STO IT memristive devices have been explored for artificial synaptic functions and neuromorphic applications. The Au/Nb:STO devices exhibited interface-controlled RS behavior with a large analog memory window, which was controlled by the modulation of the Schottky barrier owing to charge trapping and detrapping at the interface. Multiple biological synaptic functions such as EPSC, PPF, LTP/LTD, and STDP were successfully emulated based on the voltage-dependent analog RS characteristics of the Au/Nb:STO devices. Furthermore, the memristive devices demonstrated low device-to-device, cell-to-cell, and cycle-to-cycle variability while maintaining high endurance, retention, and potentiation/depression stability. The performance of these Au/Nb:STO-based synapses in a neural network was simulated using the CrossSim, and it achieved a high recognition accuracy of ≈94.72% (94.71%) for 28 × 28 (8 × 8) pixel handwritten MNIST digits. Furthermore, the correlation between nonlinearity of potentiation/depression curves and recognition accuracy was explored. This work demonstrates that interface-controlled memristive devices with analog and homogeneous RS can be

© 2023 The Authors. Advanced Intelligent Systems published by Wiley-VCH GmbH

Table 1. Comparison of performance parameters of interface-type memristive devices-based artificial synapse.

Device structure	On/Off ratio	Endurance (cycles)	Retention [s]	Accuracy [%]	Image type	References
$Au/TiO_x/AlO_\sigma/Al$	10^3	–	10^4	–	–	[62]
$Ag/SiN_x/a\text{-}Si$	20	500	3×10^3	91.3	28×28	[63]
$Ta/TaO_x/TiO_2/Ti$	10^2	10^{12}	10^6	–	–	[64]
$Ni/Ta_2O_5/Si$	10^3	10^3	10^4	86.3	28×28	[65]
$Mo/TiO_x/TiN$	10^2	–	–	90	28×28	[59]
$Pt/TiO_x/TiN$	20	–	–	84.2	23×23	[66]
Au/PV-SFO/BM-SFO/SRO	25	10^7	–	88.8	28×28	[32]
$Pt/TaO_x/HfO_2/TiN$	10^2	300	10^4	80.8	28×28	[67]
$TiN/TaO_x/HfO_x/TiN$	50	>500	>3000	–	–	[68]
$Ni/HfO_x/AlO_y/Si$	20	–	–	90.6	28×28	[69]
$TiN/TaO_2/Pt$	5	1000	$>10^4$	93.25	28×28	[70]
Au/Nb:STO/Au	10^5	$>10^4$	$>3 \times 10^4$	94.72 94.71	28×28 This work 8×8	

used to develop highly reliable synaptic devices for neuromorphic computing.

4. Experimental Section

Device Fabrication and Characterization: Nb:STO substrates (1.4 wt% of Nb, 0.5 mm thick, single-side polished) purchased from CrysTech (GmbH, Germany) were used to fabricate memristive devices. Circular Au disks (cells) and bar with the thickness of 100 nm were deposited using e-beam evaporation through predesigned metal mask at 140 °C on these Nb:STO substrates. Au disk (serving as top electrode) was about 0.07 mm^2 whereas the size of the Au bar (serving as the bottom electrode) was about 10 mm^2. The contact between Nb:STO/Au bar was Ohmic. The schematic illustration of the Au/Nb:STO/Au memristive device is shown in Figure 1a. Electrical measurements were performed with Agilent E4980A LCR and Keithley 2450 source measure units (SMUs). The SMUs could precisely measure *I–V* under direct current (DC) voltage sweep and pulsed voltage mode. Voltage amplitude, pulse duration, and pulse frequency were precisely tuned to achieve various synaptic responses from the device. All electrical measurements were carried out in ambient condition (relative humility ≈20%) with the bias applied on the top Au disks and with the Au bar grounded as displayed in Figure 1a.

Neural Network Simulation: The neural network was constructed with three fully connected layers: input, hidden, and output layers, each layer with 784, 300, and 10 neurons, respectively. MNIST database was used to train and test the neural network, which consists of 60 000 training images (28×28 pixels) and 10 000 testing images. The MNIST database has been widely used in training and testing artificial neural networks and represents handwritten digits from 0 to 9. The conductance characteristics of the Au/Nb:STO devices based on different training pulse schemes were linearly mapped to embody the synaptic weights of the neural network. Therefore, the nonlinearity and asymmetry of the LTP and LTD determined the performance of neural network simulation.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

The work at Los Alamos National Laboratory was supported by the NNSA's Laboratory Directed Research and Development Program, and was performed, in part, at the CINT, an Office of Science User Facility operated for the U.S. Department of Energy Office of Science. Los Alamos National Laboratory, an affirmative action equal opportunity employer, is managed by Triad National Security, LLC for the U.S. Department of Energy's NNSA, under contract 89233218CNA000001. F.C. and M.D.S. were supported by LDRD grant 20230627ER. A.S. acknowledges the support from the NNSA's Advanced Simulation and Computing Beyond Moore's Law Program at Los Alamos National Laboratory. The work at University at Buffalo was partially supported by the U.S. National Science Foundation under award number ECCS-1902623. Q.X.J. also acknowledges the CINT User Program. H.W. acknowledge the support from the US National Science Foundation for work at Purdue University (ECCS-1902644 and DMR-1809520). J.L.M-D. thanks the EPSRC for grant EP/T012218/1 and the Royal Academy of Engineering, grant CIET 1819 24.

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available in the supplementary material of this article.

Keywords

analog resistive switching, artificial synapse, interface-controlled memristive devices, neuromorphic computing

Received: January 17, 2023
Revised: March 23, 2023
Published online:

[1] M. A. Zidan, J. P. Strachan, W. D. Lu, *Nat. Electron.* **2018**, *1*, 22.
[2] M. A. Zidan, Y. Jeong, J. Lee, B. Chen, S. Huang, M. J. Kushner, W. D. Lu, *Nat. Electron.* **2018**, *1*, 411.
[3] K. Roy, A. Jaiswal, P. Panda, *Nature* **2019**, *575*, 607.
[4] J. M. A. K. Jain, K. M. Mohiuddin, *Computer* **1996**, *29*, 31.
[5] G. E. MOORE, *Proc. IEEE* **1998**, *86*, 82.
[6] A. Razavieh, P. Zeitzoff, E. J. Nowak, *IEEE Trans. Nanotechnol.* **2019**, *18*, 999.
[7] H. Amrouch, J.-J. Chen, K. Roy, Y. Xie, I. Chakraborty, W. Huangfu, L. Liang, F. Tu, C. Wang, M. Yayla, in *2021 IEEE/ACM Int. Conf. Computer Aided Design (ICCAD)*, IEEE, Piscataway, NJ **2021**, p. 1.
[8] Q. Xia, J. J. Yang, *Nat. Mater.* **2019**, *18*, 309.
[9] Q. Wang, G. Niu, S. Roy, Y. Wang, Y. Zhang, H. Wu, S. Zhai, W. Bai, P. Shi, S. Song, Z. Song, Y.-H. Xie, Z.-G. Ye, C. Wenger, X. Meng, W. Ren, *J. Mater. Chem. C* **2019**, *7*, 12682.
[10] Y. Zhang, Z. Wang, J. Zhu, Y. Yang, M. Rao, W. Song, Y. Zhuo, X. Zhang, M. Cui, L. Shen, R. Huang, J. Joshua Yang, *Appl. Phys. Rev.* **2020**, *7*, 011308.
[11] C. Lammie, M. Rahimi Azghadi, D. Ielmini, *Semicond. Sci. Technol.* **2021**, *36*, 065003.
[12] J. D. Sweatt, *J. Neurochem.* **2016**, *139*, 179.
[13] E. P. H. Lynn, E. Dobrunz, C. F. Stevens, *Proc. Natl. Acad. Sci.* **1997**, *94*, 14843.

© 2023 The Authors. Advanced Intelligent Systems published by Wiley-VCH GmbH

[14] D. E. Feldman, *Neuron* **2012**, *75*, 556.
[15] W. Banerjee, Q. Liu, H. Lv, S. Long, M. Liu, *Nanoscale* **2017**, *9*, 14442.
[16] C. H. Huang, H. Chang, T. Y. Yang, Y. C. Wang, Y. L. Chueh, K. Nomura, *ACS Appl. Mater. Interfaces* **2021**, *13*, 52822.
[17] H. Sun, Z. Luo, L. Zhao, C. Liu, C. Ma, Y. Lin, G. Gao, Z. Chen, Z. Bao, X. Jin, Y. Yin, X. Li, *ACS Appl. Electron. Mater.* **2020**, *2*, 1081.
[18] J.-H. Ryu, B. Kim, F. Hussain, C. Mahata, M. Ismail, Y. Kim, S. Kim, *Appl. Surf. Sci.* **2021**, *544*, 148796.
[19] A. Prakash, H. Hwang, *Phys. Sci. Rev.* **2016**, *1*, 20160010.
[20] Z. Wang, H. Wu, G. W. Burr, C. S. Hwang, K. L. Wang, Q. Xia, J. J. Yang, *Nat. Rev. Mater.* **2020**, *5*, 173.
[21] Y. Park, M.-K. Kim, J.-S. Lee, *J. Mater. Chem. C* **2020**, *8*, 9163.
[22] E. Carlos, R. Branquinho, R. Martins, A. Kiazadeh, E. Fortunato, *Adv. Mater.* **2021**, *33*, e2004328.
[23] A. Chen, W. Zhang, L. R. Dedon, D. Chen, F. Khatkhatay, J. L. MacManus-Driscoll, H. Wang, D. Yarotski, J. Chen, X. Gao, L. W. Martin, A. Roelofs, Q. Jia, *Adv. Funct. Mater.* **2020**, *30*, 2000664.
[24] P. Roy, S. Kunwar, D. Zhang, D. Chen, Z. Corey, B. X. Rutherford, H. Wang, J. L. MacManus-Driscoll, Q. Jia, A. Chen, *Adv. Electron. Mater.* **2022**, *8*, 2101392.
[25] F. Caravelli, E. Iacocca, G.-W. Chern, C. Nisoli, C. I. L. de Araujo, *Commun. Phys.* **2022**, *5*, 166.
[26] H. L. Park, M. H. Kim, M. H. Kim, S. H. Lee, *Nanoscale* **2020**, *12*, 22502.
[27] S.-O. Park, S. H. Choi, S. Seo, S. Choi, *Sci. Adv.* **2021**, *8*, eabj7866.
[28] W. Sun, B. Gao, M. Chi, Q. Xia, J. J. Yang, H. Qian, H. Wu, *Nat. Commun.* **2019**, *10*, 3453.
[29] F. Wan, Q. Wang, T. Harumoto, T. Gao, K. Ando, Y. Nakamura, J. Shi, *Adv. Funct. Mater.* **2020**, *30*, 2007101.
[30] V. R. Nallagatla, J. Jo, S. K. Acharya, M. Kim, C. U. Jung, *Sci. Rep.* **2019**, *9*, 1188.
[31] T. Tuma, A. Pantazi, M. Le Gallo, A. Sebastian, E. Eleftheriou, *Nat. Nanotechnol.* **2016**, *11*, 693.
[32] J. Rao, Z. Fan, L. Hong, S. Cheng, Q. Huang, J. Zhao, X. Xiang, E. J. Guo, H. Guo, Z. Hou, Y. Chen, X. Lu, G. Zhou, X. Gao, J. M. Liu, *Mater. Today Phys.* **2021**, *18*, 100392.
[33] A. K. Singh, U. Kar, M. D. Redell, T.-C. Wu, W.-H. Peng, B. Das, S. Kumar, W.-C. Lee, W.-L. Lee, *npj Quantum Mater.* **2020**, *5*, 45.
[34] S. Kunwar, C. B. Somodi, R. A. Lalk, B. X. Rutherford, Z. Corey, P. Roy, D. Zhang, M. Hellenbrand, M. Xiao, J. L. MacManus-Driscoll, Q. Jia, H. Wang, J. Yang, W. Nie, A. Chen, *Adv. Electron. Mater.* **2022**, *9*, 2200816.
[35] E. Mikheev, B. D. Hoskins, D. B. Strukov, S. Stemmer, *Nat. Commun.* **2014**, *5*, 3990.
[36] E. M. Bourim, Y. Kim, D.-W. Kim, *ECS J. Solid State Sci. Technol.* **2014**, *3*, N95.
[37] Z. Fan, H. Fan, L. Yang, P. Li, Z. Lu, G. Tian, Z. Huang, Z. Li, J. Yao, Q. Luo, C. Chen, D. Chen, Z. Yan, M. Zeng, X. Lu, X. Gao, J.-M. Liu, *J. Mater. Chem. C* **2017**, *5*, 7317.
[38] J. Li, G. Yang, Y. Wu, W. Zhang, C. Jia, *Phys. Status Solidi A* **2018**, *215*, 1700912.
[39] G. Li, Z. Yang, X. Zhang, G. Li, X. Sun, W. Zhang, *Phys. Status Solidi A* **2019**, *216*, 1900125.
[40] Y. S. Chen, B. Chen, B. Gao, L. F. Liu, X. Y. Liu, J. F. Kang, *J. Appl. Phys.* **2013**, *113*, 164507.
[41] M. Akbari, M.-K. Kim, D. Kim, J.-S. Lee, *RSC Adv.* **2017**, *7*, 16704.
[42] J. M. Rafí, M. B. Gonzalez, O. Beldarrain, F. Campabadal, M. Zabala, *IEEE Trans. Device Mater. Reliab.* **2014**, *14*, 769.
[43] N. Ilyas, D. Li, C. Li, X. Jiang, Y. Jiang, W. Li, *Nanoscale Res. Lett.* **2020**, *15*, 30.
[44] B. L. Pai-Yu Chen, I.-T. Wang, T.-H. Hou, J. Ye, S. Vrudhula, J.-S. Seo, Y. Cao, S. Yu, presented at *Int. Conf. Computer-Aided Design (ICCAD)*, Austin, TX, USA **2015**.
[45] C. He, J. Tang, D. S. Shang, J. Tang, Y. Xi, S. Wang, N. Li, Q. Zhang, J. K. Lu, Z. Wei, Q. Wang, C. Shen, J. Li, S. Shen, J. Shen, R. Yang, D. Shi, H. Wu, S. Wang, G. Zhang, *ACS Appl. Mater. Interfaces* **2020**, *12*, 11945.
[46] S. Qin, F. Wang, Y. Liu, Q. Wan, X. Wang, Y. Xu, Y. Shi, X. Wang, R. Zhang, *2D Mater.* **2017**, *4*, 035022.
[47] X. Yan, Y. Pei, H. Chen, J. Zhao, Z. Zhou, H. Wang, L. Zhang, J. Wang, X. Li, C. Qin, G. Wang, Z. Xiao, Q. Zhao, K. Wang, H. Li, D. Ren, Q. Liu, H. Zhou, J. Chen, P. Zhou, *Adv. Mater.* **2019**, *31*, e1805284.
[48] R. S. Zucker, W. G. Regehr, *Annu. Rev. Physiol.* **2002**, *64*, 355.
[49] S. G. Hu, Y. Liu, T. P. Chen, Z. Liu, Q. Yu, L. J. Deng, Y. Yin, S. Hosaka, *Appl. Phys. Lett.* **2013**, *102*, 183510.
[50] P. Gkoupidenis, D. A. Koutsouras, G. G. Malliaras, *Nat. Commun.* **2017**, *8*, 15448.
[51] X. Yan, L. Zhang, H. Chen, X. Li, J. Wang, Q. Liu, C. Lu, J. Chen, H. Wu, P. Zhou, *Adv. Funct. Mater.* **2018**, *28*, 1803728.
[52] X. Deng, S. Q. Wang, Y. X. Liu, N. Zhong, Y. H. He, H. Peng, P. H. Xiang, C. G. Duan, *Adv. Funct. Mater.* **2021**, *31*, 2101099.
[53] K. Portner, M. Schmuck, P. Lehmann, C. Weilenmann, C. Haffner, P. Ma, J. Leuthold, M. Luisier, A. Emboras, *ACS Nano* **2021**, *15*, 14776.
[54] J.-H. Ryu, C. Mahata, S. Kim, *J. Alloys Compd.* **2021**, *850*, 156675.
[55] S. J. P. S. Agarwal, R. K. Schiek, I. Richter, A. H. Hsia, D. R. Hughart, R. B. Jacobs-Gedrim, C. D. James, M. J. Marinella, https://cross-sim.sandia.gov/ (accessed: May 2022).
[56] C. Li, D. Belkin, Y. Li, P. Yan, M. Hu, N. Ge, H. Jiang, E. Montgomery, P. Lin, Z. Wang, W. Song, J. P. Strachan, M. Barnell, Q. Wu, R. S. Williams, J. J. Yang, Q. Xia, *Nat. Commun.* **2018**, *9*, 2385.
[57] B. C. Jang, S. Kim, S. Y. Yang, J. Park, J. H. Cha, J. Oh, J. Choi, S. G. Im, V. P. Dravid, S. Y. Choi, *Nano Lett.* **2019**, *19*, 839.
[58] V. R. Nallagatla, J. Kim, K. Lee, S. C. Chae, C. S. Hwang, C. U. Jung, *ACS Appl. Mater. Interfaces* **2020**, *12*, 41740.
[59] J. Park, C. Lee, M. Kwak, S. A. Chekol, S. Lim, M. Kim, J. Woo, H. Hwang, D. Lee, *Nanotechnology* **2019**, *30*, 305202.
[60] F. Caravelli, F. C. Sheldon, F. L. Traversa, *Sci. Adv.* **2021**, *7*, eabh1542.
[61] F. Caravelli, F. L. Traversa, M. Di Ventra, *Phys. Rev. E* **2017**, *95*, 022140.
[62] S. Cho, J. Jung, S. Kim, J. J. Pak, *Semicond. Sci. Technol.* **2020**, *35*, 085006.
[63] K. Kim, S. Park, S. M. Hu, J. Song, W. Lim, Y. Jeong, J. Kim, S. Lee, J. Y. Kwak, J. Park, J. K. Park, B.-K. Ju, D. S. Jeong, I. Kim, *NPG Asia Mater.* **2020**, *12*, 77.
[64] Y. F. Wang, Y. C. Lin, I. T. Wang, T. P. Lin, T. H. Hou, *Sci. Rep.* **2015**, *5*, 10150.
[65] J.-H. Ryu, F. Hussain, C. Mahata, M. Ismail, Y. Abbas, M.-H. Kim, C. Choi, B.-G. Park, S. Kim, *Appl. Surf. Sci.* **2020**, *529*, 147167.
[66] J. Park, M. Kwak, K. Moon, J. Woo, D. Lee, H. Hwang, *IEEE Electron Device Lett.* **2016**, *37*, 1559.
[67] H. Ryu, S. Kim, *Nanomaterials* **2020**, *10*, 1550.
[68] W. Wu, H. Wu, B. Gao, N. Deng, S. Yu, H. Qian, *IEEE Electron Device Lett.* **2017**, *38*, 1019.
[69] S. Kim, J. Chen, Y. C. Chen, M. H. Kim, H. Kim, M. W. Kwon, S. Hwang, M. Ismail, Y. Li, X. S. Miao, Y. F. Chang, B. G. Park, *Nanoscale* **2018**, *11*, 237.
[70] M. Kim, M. A. Rehman, D. Lee, Y. Wang, D. H. Lim, M. F. Khan, H. Choi, Q. Y. Shao, J. Suh, H. S. Lee, H. H. Park, *ACS Appl. Mater. Interfaces* **2022**, *14*, 44561.

© 2023 The Authors. Advanced Intelligent Systems published by Wiley-VCH GmbH