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Power Loss Characterization and Modeling for GaN-Based Hard-Switching Half-Bridges Considering Dynamic On-State Resistance

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***Abstract*— Gallium Nitride enhancement-mode high electron mobility transistors (GaN E-HEMTs) can achieve high frequency and high efficiency due to its excellent switching performance compared with conventional Si transistors. Nevertheless, GaN HEMTs exhibit a more pronounced dynamic on-state resistance $R_{DS(on)}$ than silicon transistors. The variation of $R_{DS(on)}$ is caused by both the static $R_{DS(on)}$ due to junction temperature rise and the dynamic $R_{DS(on)}$ due to the electron trapping. Without a careful decoupling analysis, it is difficult to calculate and model the dynamic $R_{DS(on)}$ portion. This paper introduces a comprehensive approach of dynamic $R_{DS(on)}$ evaluation, comprising four techniques: 1) a clamping circuit for both the hard-switching (HS) device and synchronous rectification (SR) device; 2) a junction temperature monitoring technique; 3) control of both the pulse test and soak time; 4) continuous operation of device under test. Based on the dynamic $R_{DS(on)}$ test results, a new model of the $R_{DS(on)}$ variation is developed where two coefficients: k_{Tj} and k_{dR} are defined to model the contribution of the heating effect and the impact of the trapping effect, respectively. The $R_{DS(on)}$ model is validated by the comparison between the calculated and measured junction temperatures of a 650 V/30 A GaN-based half-bridge. Furthermore, a detailed loss breakdown analysis is conducted for the GaN-based hard-switching half-bridge. Results show that the switching losses, E_{on} and E_{off} are the dominant loss factors with high switching frequency. At last, the possible efficiency improvements are also discussed in detail.**

***Index Terms*— GaN HEMT, half-bridge, dynamic on-state resistance, hard-switching, power loss modeling, switching loss.**

I. Introduction

Gallium Nitride enhancement-mode high electron mobility transistors (GaN E-HEMTs) have significant advantages over conventional Si MOSFETs [1-2], such as the zero reverse recovery loss, low capacitive C_{oss} loss, excellent transconductance to reduce the rise/falling time during switching transitions, and good paralleling capability, etc. [3-5]. These advantages make GaN HEMTs promising candidates for converters demanding high switching frequency, high conversion efficiency, and high power density.

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Current research has demonstrated the advantages of GaN E-HEMTs in various applications, such as electric vehicles (EVs), consumer electronics, data centers, and renewable energy applications [6-8]. In particular, it is a trend that future EVs will adopt GaN HEMTs to achieve higher power density, lower weight, and higher efficiency. As a result, the vehicle running mileage can be increased [9].

Fig. 1 shows a typical diagram of the power electronics converters in EVs [9-10]. The AC/DC stage is an onboard charger, which can be implemented with either a two-stage AC/DC converter consisting of an AC/DC Boost PFC and a second-stage DC/DC converter, or a single-stage AC/DC converter [11-14]. For the propulsion subsystem, a three-phase traction inverter is needed to provide a DC/AC energy conversion for the traction motor [15]. A DC/DC Boost converter can be applied in between the onboard charger and traction inverter to step up the voltage for the traction system and also to provide a controllable DC input voltage for the traction inverter. Another isolated DC/DC converter is needed to convert energy from high voltage to low voltage for the low-voltage (LV) electronic loads. This converter is also known as the auxiliary power module (APM) [16-19].

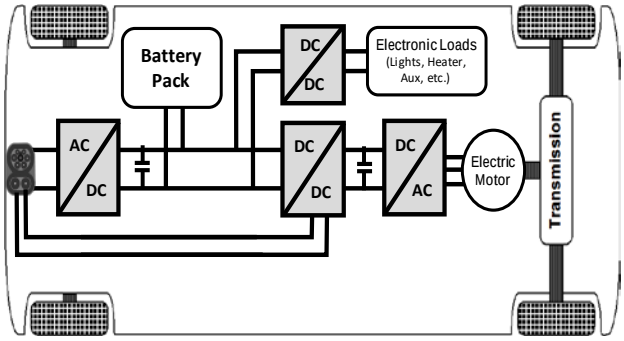

Fig. 1: Typical diagram of power electronics converters in electrified vehicles.

From the switching mode aspect, these converters can be classified into hard-switching and soft-switching converters. The AC/DC PFC, DC/DC Boost converter, and DC/AC inverter usually operate in the hard-switching mode. Typically, their power stages are based on the basic half-bridge unit, as shown in Fig. 2. For a half-bridge unit, one device is operating in the hard-switching (HS) mode, whereas the other will be in the synchronous rectification (SR) mode. Typically, the isolated DC/DC converter in Fig. 1 can run in the soft-switching mode.

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However, zero-voltage-switching (ZVS) can be lost under the light-load mode, due to the insufficient inductive energy to charge/discharge the parasitic capacitance C_{oss} in the power devices, like phase-shift full bridge (PSFB) converter. In this case, the hard-switching power loss characteristics also need to be considered. With GaN E-HEMTs used in these hard-switching half-bridge stages, the power conversion efficiency and power density can be significantly improved compared with Silicon counterparts.

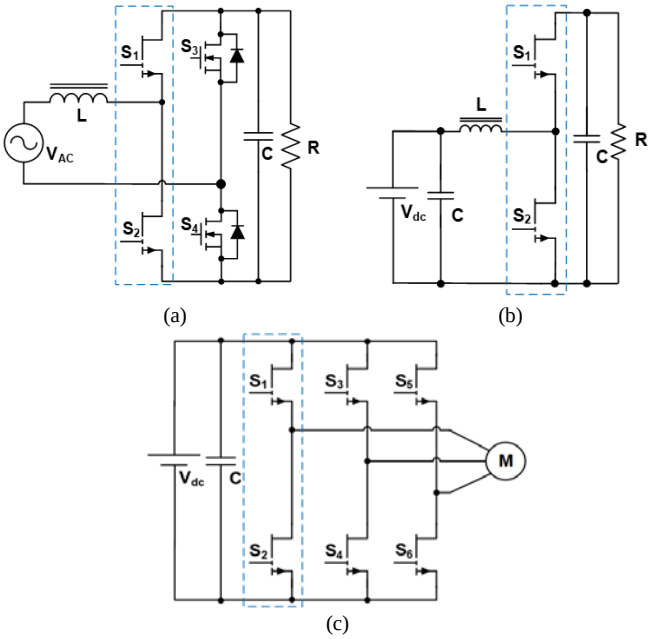

Fig. 2: Hard-switching half-bridge-based converters employing GaN E-HEMTs, (a) Totem-pole PFC, (b) DC/DC Boost converter, (c) three-phase traction inverter

Nevertheless, an accurate power loss calculation is necessary in order to evaluate the efficiency improvement and to re-design heatsinks for the weight/volume/cost optimization of GaN-based converters. For Si MOSFETs, the reverse recovery loss is relatively complicated to calculate and model, as it is dependent on the variables like operating voltage, load current, conduction time, *di/dt*, etc. GaN E-HEMTs do not have reverse recovery loss, which makes the switching loss calculation more straightforward. However, research from both academia and industry reveals that the on-state drain-source resistance ($R_{DS(on)}$) of GaN E-HEMTs changes under different operation conditions, which complicates the conduction loss estimation. Therefore, characterizing $R_{DS(on)}$ on GaN devices has been attracting increasing attention [20-33].

Researchers have shown that $R_{DS(on)}$ depends on various parameters, e.g., the operating voltage, junction temperature, duty cycle, switching frequency, load current, gate resistance, switching modulation, and GaN semiconductor production process [20], [22-30]. As a result, the $R_{DS(on)}$ variation becomes complicated, which makes the accurate power loss calculation challenging. To estimate the power loss, the prevailing power loss models use behavior-based models including the piece-wise linear, analytical, and numerical models [4], [5], [35-40]. These techniques, however, are time-consuming and have not yet considered the dynamic $R_{DS(on)}$ variation. Hence, it is necessary to characterize and model the $R_{DS(on)}$ variation such that the dynamic $R_{DS(on)}$ can be incorporated into the above power loss models.

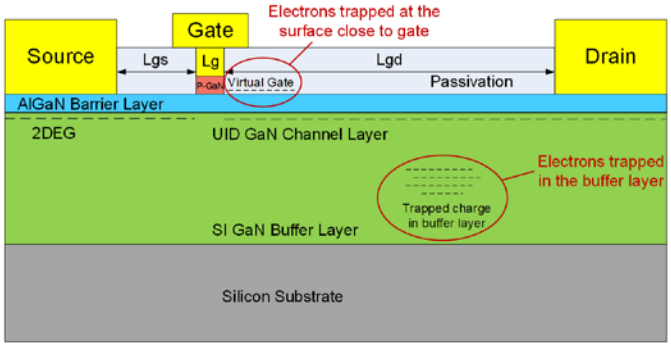

Fig. 3: Lateral GaN HEMT device structure with trapped electrons.

Physically, the variation of $R_{DS(on)}$ is mainly due to two aspects: the heating effect and the charge trapping effect of electrons. The rising junction temperature decreases the electron mobility and hence increases the static $R_{DS(on)}$. The mechanism of charge trapping effect of electrons is shown in Fig. 3. The electrons can be trapped at the surface close to the gate, and are also trapped in the buffer layer. The charge trapping effect results in a decrease of the two-dimensional electron gas (2DEG) density, and therefore, causes the dynamic $R_{DS(on)}$ to increase [20-21]. At different operating conditions, e.g., different operating voltages, duty cycles, switching frequencies, and load currents, both the heating and charge trapping effects can be induced, causing an increased $R_{DS(on)}$. However, many studies don't separate the two effects when testing and characterizing dynamic $R_{DS(on)}$ of GaN devices.

Another critical issue of current $R_{DS(on)}$ characterization techniques is that the practical operation condition has not been fully considered. For instance, refs. [23] and [26] apply a relatively long ($\geq$ 1s) or random soak time (i.e., the electron trapping time) in the $R_{DS(on)}$ characterization; thus, they claim that a long soak time can increase the dynamic $R_{DS(on)}$. However, the actual soak time is less than 100 µs because the switching frequency is higher than 10 kHz in most GaN E-HEMT based systems. In [20] and [29], authors propose to apply continuous tests rather than double pulse tests such that the soak time is more practical. However, the junction temperature is not monitored and thus, it is relatively hard to decouple the $R_{DS(on)}$variation due to the heating from the $R_{DS(on)}$ variation from the trapping effect. Because the heating effect depends on the thermal design (such as the heatsink design and the ambient temperature), the systems with different heatsinks can result in different dynamic $R_{DS(on)}$, and it is hard to repeat the exact results in [20], [29].

In this paper, the modified double pulse test (DPT) with soak time control and continuous test are both discussed. The junction temperature control decouples the $R_{DS(on)}$ into three portions, which are the static $R_{DS(on)}$ at 25 °C, the increased static $R_{DS(on)}$ due to heating effect, and the increased dynamic $R_{DS(on)}$ due to trapping effect. Then, an accurate conduction loss

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model is proposed by introducing two scaling coefficients, k_{Tj} and k_{dR}, which represent the contributions of the heating effect and trapping effects, respectively. The proposed model can accurately predict the loss evaluation for GaN-based hard-switching half-bridge applications under different operating conditions. Finally, the power loss tests at different junction temperatures are provided to evaluate the percentage of each loss generated by GaN HEMTs. The results reveal that the switching loss and deadtime loss dominate the total power loss, and the power loss due to the dynamic $R_{DS(on)}$ from the trapping effect is insignificant especially at high switching frequencies (e.g., > 20 kHz). In addition, with the detailed loss breakdown analysis, the further efficiency improvement for the GaN-based half-bridge is also discussed in detail.

The paper is organized as follows: Section II presents the power loss overview in GaN-based hard switching half-bridge. The switching loss, conduction loss, and deadtime loss for GaN HEMT are illustrated. Section III proposes a comprehensive test set-up for the $R_{DS(on)}$ characterization. The test set-up includes the on-state voltage measurement and clamping circuit design, the junction temperature monitoring, and the test methods discussion. Section IV proposes the power loss modeling for GaN HEMTs, where the modeling of switching loss E_{on}/E_{off} and decoupling analysis of $R_{DS(on)}$ are given in detail. Section V uses experiments to verify that the proposed power loss model is accurate under different operating conditions. The power loss distribution is also discussed to reveal the effect of dynamic $R_{DS(on)}$ on system loss. Finally, conclusions are drawn in Section VI.

II. Power Loss Overview in GaN-Based Hard-Switching Half-Bridges

The accumulated energy loss trajectories for the HS device and the SR device of a GaN-based hard-switching half-bridge are shown in Fig. 4 (a) and (b), respectively. The loss trajectories apply to all the system topologies that contain the GaN-based hard-switching half-bridge. It is clear that the SR device does not obtain the switching loss. However, two deadtime losses have occurred on this device.

The total accumulative energy loss E_{loss} of a device over a switching cycle is obtained by

$$E_{loss\_HS} = E_{on} + E_{cond} + E_{off} \tag{1}$$

$$E_{loss\_SR} = E_{deadtime1} + E_{cond} + E_{deadtime2} \tag{2}$$

where E_{on} and E_{off} represent the switching-on and switching-off energy losses, respectively; E_{cond} is the conduction loss; $E_{deadtime1}$ and $E_{deadtime2}$ denote the deadtime losses before turn-on and after turn-off, respectively.

A. Switching losses E_{on} and E_{off}

The switching energy losses E_{on} and E_{off} of GaN HEMTs have been studied thoroughly. Basically, the E_{on} consists of the I/V overlapping loss in the switching-on transition and the capacitive energy loss E_{qoss} from the opposite device in the half-bridge; E_{off} is composed of the I/V overlapping loss in the switching-off transition and the capacitive energy loss E_{oss}. The capacitive energy losses E_{oss} and E_{qoss} haven been studied in [4]. It is found that E_{oss} and E_{qoss} are functions of the drain-source voltage and output capacitance, and are independent of the junction temperature and the drain-source current. The equations for the E_{oss} and E_{qoss} are given as,

$$E_{oss} = \int_0^{V_{dc}} V_{ds} \cdot C_{oss(V_{ds})} dV_{ds} \tag{3}$$

$$E_{qoss} = \int_0^{V_{dc}} (V_{dc} - V_{ds}) \cdot C_{oss(V_{ds})} dV_{ds} \tag{4}$$

where V_{dc} is the applied DC-link voltage and C_{oss} is the output parasitic capacitance of the applied GaN HEMT device.

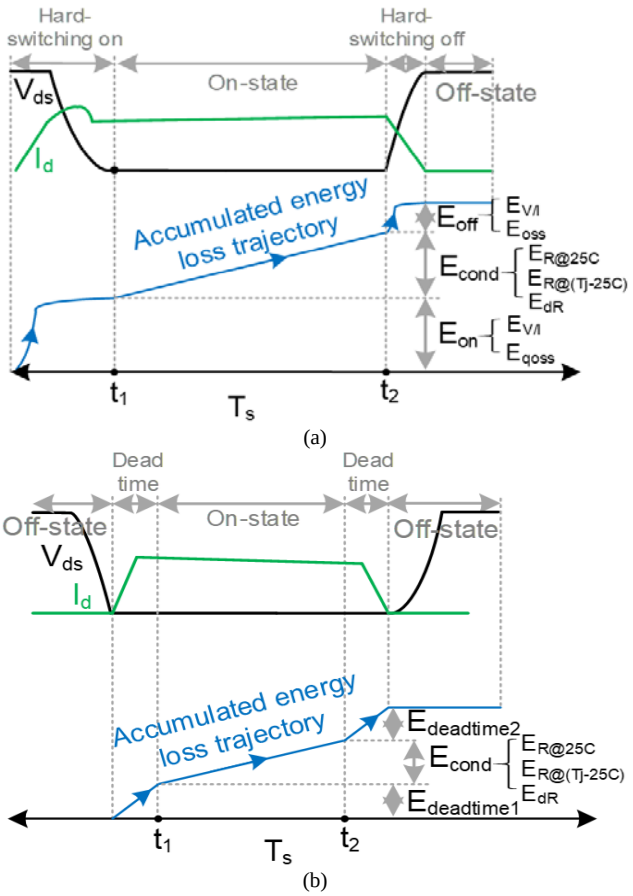

Fig. 4: Voltage and current waveforms and accumulative energy loss trajectories of a GaN-based half bridge over one switching cycle. (a) HS device, (b) SR device.

It should be noted that there is a difference between the measured E_{on}/E_{off} externally outside the device package and the intrinsic E_{on}/E_{off} inside device 2DEG; it is about the self-discharging capacitance loss E_{oss}. The loss E_{oss} can not be measured directly during the turn-on transition since the output capacitor C_{oss} is discharged through the internal 2DEG. Meanwhile, the same amount of loss E_{oss} will occur during the turn-off transition, as the capacitor self-charging current will flow to the outside of the device package and thus this amount of loss will be measured. But this amount of loss does not belong to turn-off loss, as the gate voltage is already below its

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threshold voltage and the 2DEG of that device is turned off. The E_{on}/E_{off} loss distribution for both measured and intrinsic can be shown in Fig. 5. In fact, this difference between measured and intrinsic losses does not affect the overall loss in hard-switching half-bridge. However, for soft-switching ZVS turn-on, as the capacitances C_{oss} for both high-side and low-side devices are resonant with power inductor, the capacitive loss E_{oss}/E_{qoss} are both zero. Therefore, for ZVS applications, only the $E_{V/I}$ loss in the E_{off} exists as the overall switching loss.

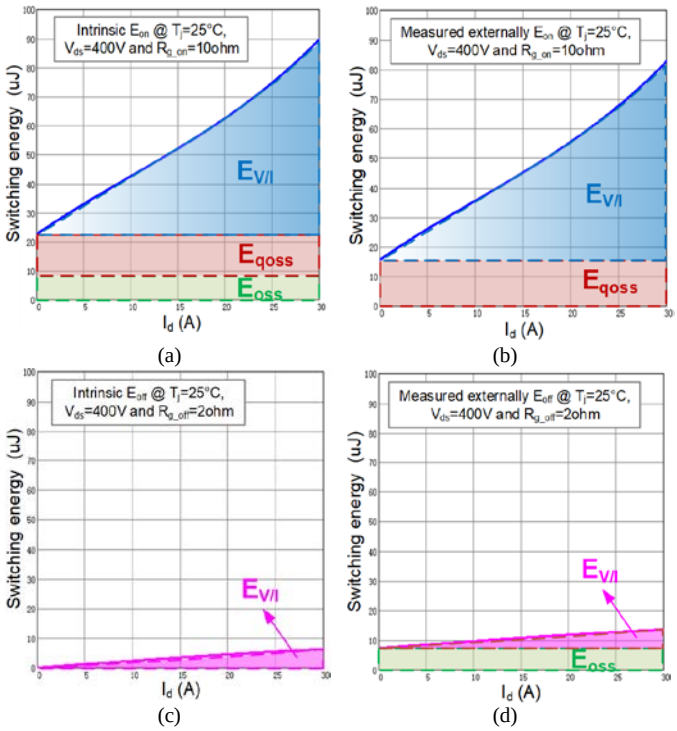

Fig. 5: Switching loss distribution. (a) intrinsic E_{on}, (b) measured E_{on}, (c) intrinsic E_{off}, (d) measured E_{off}.

B. Deadtime loss

GaN HEMTs do not have body diode inside and thus they have no reverse recovery period or corresponding power loss. This significantly improves both the switching speed and switching loss. Meanwhile, GaN HEMTs are still capable of conducting current reversely through the same channel when its gate is off. This is because that the 2DEG of GaN E-HEMT is bidirectional.

With a +6V voltage applied to the gate, the I-V curves are symmetrical in the first and third quadrants, as shown in Fig. 6. That is, with a positive or reverse current flow, the on-state voltage is the same. Moreover, under the third quadrant, a negative V_{ds} can still turn the device on in reverse, with the drain now behaving as source and the source as drain. In other words, when the V_{gd} voltage is higher than the threshold voltage V_{th}, the device will be turned on reversely. The V_{gd} voltage can be obtained as,

$$V_{gd} = V_{gs} - V_{ds} \tag{5}$$

This behavior makes GaN E-HEMT similar to a diode under third quadrant when the gate is off. But the voltage drop is typically higher than the diode's. Due to the relatively low threshold voltage of GaN E-HEMTs, it is also typically recommended to use a negative gate voltage V_{gs_off} for the off-state in order to prevent accidental turn-on. This negative gate voltage is added to the voltage drop across the channel resistance, leading to relatively higher power loss.

Therefore, synchronous rectification is preferred for GaN E-HEMTs during reverse conduction thus this high voltage drop loss only happens in the deadtime. This voltage drop during the deadtime can be obtained as,

$$V_{deadtime} = V_{th} + |V_{gs\_off}| + V_{ds(on)} \tag{6}$$

where V_{th} is the threshold voltage, V_{gs_off} is the turn-off gate voltage, and $V_{ds(on)}$ represents the on-state drain-to-source voltage.

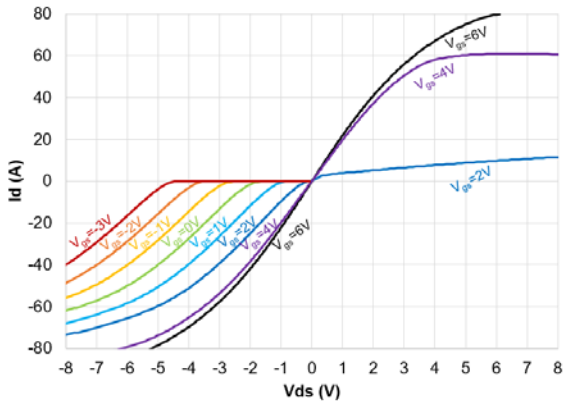

Fig. 6: Measured I-V curves of GS66508T GaN E-HEMT.

C. Conduction losses

Conventionally, the on-state resistance $R_{DS(on)}$ of Si MOSFETs can be divided into two parts, the static $R_{DS(on)}$ at 25 °C and the increased static $R_{DS(on)}$ from heating effect. However, for GaN devices, the dynamic $R_{DS(on)}$ caused by the electron-trapping effect also needs to be taken into account. Therefore, the total conduction energy loss E_{cond} of GaN E-HEMTs is composed of three portions, i.e.,

$$E_{cond} = E_{R@25°C} + E_{R@(Tj-25°C)} + E_{dR} \tag{7}$$

where $E_{R@25°C}$ is the energy loss contributed by the static $R_{DS(on)}$ at 25 °C; $E_{R@(Tj-25°C)}$ is the energy loss due to the increased static $R_{DS(on)}$ from the heating effect, and E_{dR} is the energy loss caused by the increased dynamic $R_{DS(on)}$ from the trapping effect.

It is important to decouple the $R_{DS(on)}$ into three portions such that their corresponding energy losses can be calculated accordingly. This decoupling method also helps with the loss calculation. As in a continuous operation, the self-heating from the device needs to be considered. It affects the final overall losses and final junction temperature. Several iterations are needed to make the loss calculation reaches thermal steady-state. If the loss term from the trapping effect is included in the thermal effect, this will make the iterations more complicated. In this paper, the normalized increase of $R_{DS(on)}$ due to the heating effect and trapping effect are defined as k_{Tj} and k_{dR} and thus, the equations for each conduction loss energy can be

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obtained as,

$$E_{R@25C} = \int_{t1}^{t2} \left(i_{d(t)}^2 \cdot R_{DSon(25℃)}\right) dt \quad (8)$$

$$E_{R@(Tj-25C)} = \int_{t1}^{t2} \left(i_{d(t)}^2 \cdot R_{DSon(25℃)} \cdot k_{Tj}\right) dt \quad (9)$$

$$E_{dR} = \int_{t1}^{t2} \left(i_{d(t)}^2 \cdot R_{DSon(25℃)} \cdot k_{dr}\right) dt \quad (10)$$

where t_1 and t_2 represent the beginning and end instants of the conduction time duration, respectively; k_{Tj} and k_{dR} are the normalized increases of $R_{DS(on)}$ due to the heating effect and trapping effect, respectively. The detailed $R_{DS(on)}$ measurement and its decoupling analysis will be explained in the next two sections.

III. Measurement and Characterization of $R_{DS(ON)}$ for GaN HEMTs

In this section, the detailed dynamic $R_{DS(on)}$ measurement will be discussed. The two most critical measurements, i.e., the on-state voltage and junction temperature of the device under test (DUT), will be introduced first. Then, two test setups will be presented, which are the DPT with soak time control and the continuous system test.

A. On-state voltage measurement and clamping circuit

One of the most critical parts of the dynamic $R_{DS(on)}$ measurement is the design of the clamping circuit. As the operating voltage for high-voltage GaN HEMTs is usually around hundreds of volts (typically around 400 V). For a conventional 8-bit oscilloscope, usually, 100 V/div is applied to measure the V_{ds} voltage. This brings the challenge to the on-state V_{ds} voltage measurement accuracy. Therefore, a clamping circuit is applied to clamp and block the high off-state V_{ds} voltage and only measure the low on-state V_{ds} voltage. Therefore, the low voltage measurement resolution will be improved and the results will be more accurate. Many clamping circuits are proposed and applied in [22-29].

In this paper, for the $R_{DS(on)}$ measurement on the HS device, the developed clamping circuit shown in Fig. 7 (a) is similar to that in [28], due to its fast switching performance, good dynamic response, and reliable operation. In this clamping circuit, D_1 is a high-voltage SiC diode with relatively small parasitic capacitance. It blocks the high voltage during the off-state and conducts during the on-state of the DUT. In order to attenuate the voltage spike on the clamping circuit, a Zener diode Z_1 is needed and thus the measured voltage is not overridden on the oscilloscope and a higher measurement resolution can be achieved. However, Zener diodes usually have relatively poor reverse recovery performance. During the switching-on transient, due to the fast-switching performance of GaN HEMTs, a relatively high *dv/dt* will be introduced. The current can flow into the Zener diode Z_1 and its reverse recovery will impact the measured voltage $v_{DS(m)}$. Therefore, a low-voltage Schottky diode D_2 is applied to provide a path for the current during the *dv/dt*.

For the SR device, a reverse current flow through the DUT and a negative on-state voltage are obtained. Therefore, the clamping circuit in Fig. 7 (a) can not be applied to measure the negative on-state voltage. The reason is that the diode D_2 will attempt to clamp the negative voltage to zero. Therefore, the clamping circuit is modified to Fig. 7 (b). The diode D_2 is removed and in order to prevent the voltage overshoot and undershoot, the back-to-back Zener diodes Z_1/Z_2 are applied.

Meanwhile, R_1 and R_2 form a voltage divider on the supplied voltage V_{cc1}. Therefore, during the off-state of the DUT, the clamped voltage will be

$$V_{clamp} = \frac{R_2}{R_1 + R_2} \cdot V_{cc1} \quad (11)$$

where V_{cc1} is the supplied voltage to the clamping circuit.

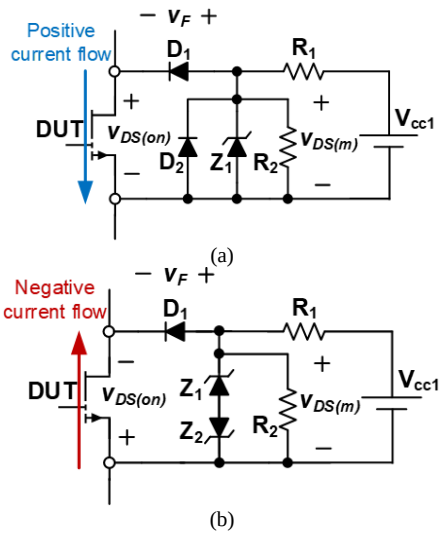

Fig. 7: Schematic of the on-state resistance measurement circuit (clamping circuit), (a) for HS device, (b) for SR device.

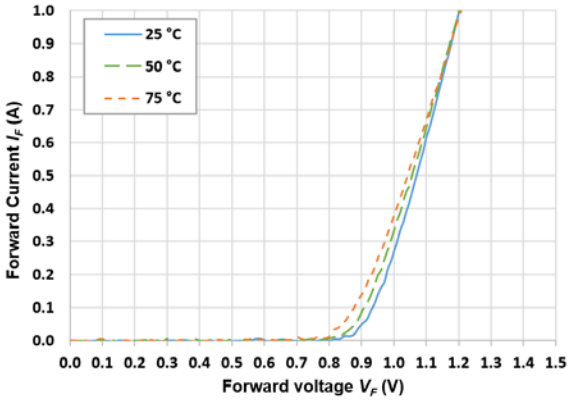

Fig. 8: Forward characteristics of the applied SiC diode (C3D02065E).

The Zener diode breakdown voltage can be chosen based on the voltage value above. In addition, in order to limit the heating effect on the resistance value variations on the R_1 and R_2, the R_1 and R_2 are chosen with a relatively low temperature coefficient. During the on-state, the on-state voltage of the DUT can be calculated as

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$$v_{DS(on)} = v_{DS(m)} - v_F \quad (12)$$

where v_F is the forward voltage drop on the SiC diode D_1. It should be noted that v_F is not a constant value but is dependent on its forward current i_{D1} and also the temperature. The forward characteristics of the SiC diode used in the clamping circuit are shown in Fig. 8.

The forward current i_{D1} can be obtained by the equation below

$$i_{D1} = \frac{v_{cc1} - v_{DS(m)}}{R_1} - \frac{v_{DS(m)}}{R_2} \quad (13)$$

In fact, the current flowing through SiC diode D_1 is relatively small. Therefore, the self-heating from D_1 is not significant. For the sake of accurate voltage measurement, it is necessary to place the SiC diode close to the DUT, where the temperature is relatively high. On the other hand, in order to mitigate the temperature's impact on the SiC diode, it is desired to have the SiC diode installed away from the heat source and DUT. In this paper, the clamping circuit is implemented with a daughter board and installed upon the mother board. A small heatsink is also applied on the SiC diode and its temperature is monitored by a thermal camera. The temperature on the heatsink is also monitored in the steady-state to compensate for the forward voltage difference caused by the temperature increase.

B. *Junction temperature monitoring*

Junction temperature monitoring is another critical part of the dynamic $R_{DS(on)}$ measurement. As shown in Fig. 9 (a), the structure of a top-cool GaN HEMT, on which a heat source or a heat sink can be attached. The thermal interface material (TIM) is applied in-between to provide electrical isolation. Inside the GaN E-HEMT, there are four major layers. Among them, the copper base of the GaN HEMT is close to the heat source or heat sink. And the actual GaN layer is very close to the PCB. Two holes are drilled in the PCB for the temperature measurement by using a thermal camera. The thermal camera applied in this paper is FLIR E75. The detailed junction-to-case thermal model for GaN HEMT can be found in [41-42]. Basically, the model is a four-level RC Cauer thermal model, as shown in Fig. 10. For GS66508T, the parameters for the junction-to-case thermal model is also given in Table I. The simulation results of the relationship between the monitored package temperature and the actual junction temperature are shown in Fig. 9 (b). It is clear that the temperature difference is relatively small. This is important, as then for the total measured $R_{DS(on)}$ value, its heating and trapping effects can be separated and therefore, an accurate dynamic $R_{DS(on)}$ value can be obtained.

TABLE I
RC CAUER THERMAL MODEL PARAMETERS FOR GS66508T

	R_θ (°C/W)	C_θ (W·s/°C)
#1	0.015	8.0×10^{-5}
#2	0.23	7.4×10^{-4}
#3	0.24	6.5×10^{-3}
#4	0.015	2.0×10^{-3}

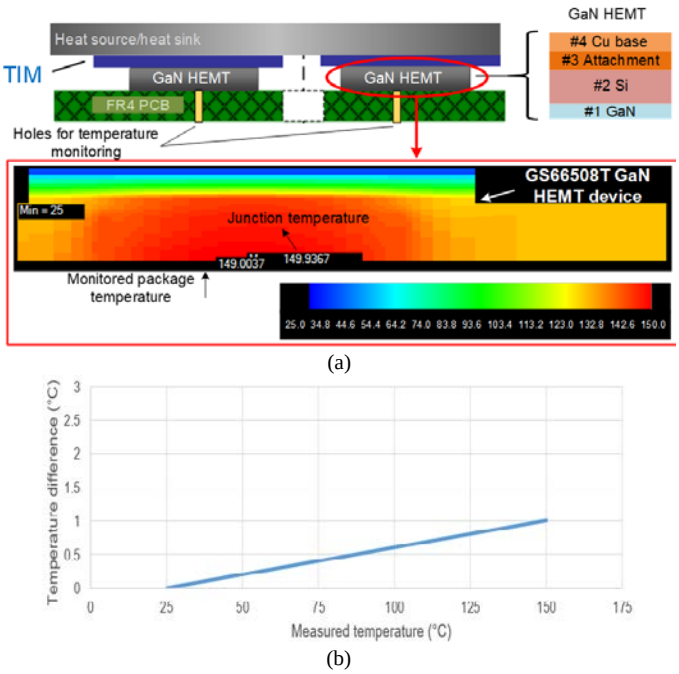

Fig. 9. Junction temperature monitoring with holes drilled in PCB and the simulated temperature difference between the junction and the package of GS66508T GaN E-HEMT. (a) The simulated temperature contour. (b) The simulated temperature difference between the junction and the package.

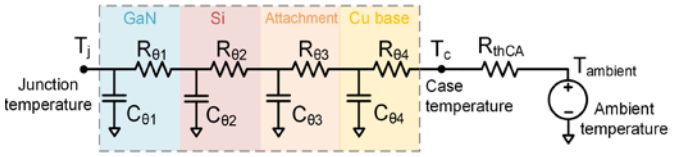

Fig. 10. 4-level RC Cauer thermal model for GaN HEMT.

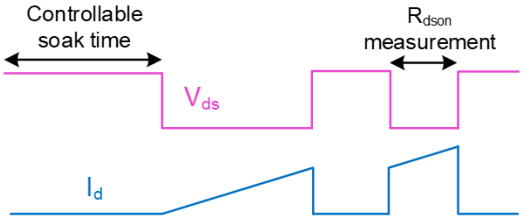

Fig. 11: Soak time control diagram.

C. *Test circuit discussion*

As power electronics engineers get used to applying double pulse tests (DPTs) to measure the switching energy loss E_{on}/E_{off}, the first attempt on the dynamic $R_{DS(on)}$ measurement is also based on the same test bench. However, conventional DPT does not support the soak time control. The soak time represents the time duration after the high voltage is on while before triggering the DPT, as illustrated in Fig. 11.

The switching loss E_{on}/E_{off} does not change with the soak time. Therefore, it is not necessary to apply the soak time control in the E_{on}/E_{off} measurement. However, the trapping effect is dependent on the soak time. The longer the device is soaked or stressed, the higher the trapping effect will be.

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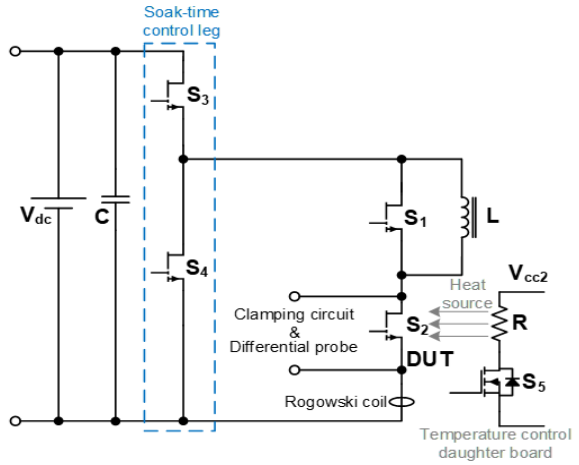


Fig. 12: Schematic of a double-pulse test with soak time and junction temperature control.

The soak time control can be achieved by an additional half bridge leg S3/S4 as shown in Fig. 12. In this test setup, two GS66516B GaN HEMTs are applied for switches S3 and S4. And here S1, S2 and inductor L form a traditional DPT. The GS66508T is applied for S1 and S2. Fig. 13 shows the on/off sequence of the four switches S1-S4. At the beginning of the sequence, only switch S4 is turned on, and then the high voltage is applied to the dc link. There is no voltage across device S2 until S4 is turned off. After the deadtime, S3 is turned on, and after that, the device starts to handle the voltage stress and then later the DPT can be triggered.

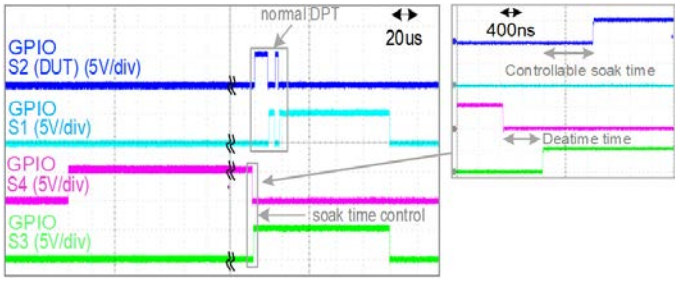
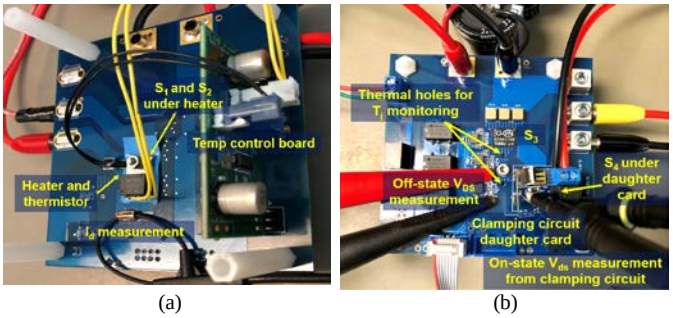


Fig. 13: The switch on/off sequence of S_1-S_4 for the pulse test with soak time control.

During the DPT, the junction temperature is controlled by using a temperature control board. The temperature control board consists of a heating resistor, an NTC thermistor, and a power switch. Close-loop temperature control is also achieved by using the NTC thermistor to sense the temperature and a controller to control the PWM to the power switch.

The pulse test setup from the top view and bottom view is shown in Fig. 14. In Fig. 14 (a), the S_1/S_2 half-bridge is under the heater and thermistor. The Rogowski coil for the drain current measurement is close to the DUT. In Fig. 14 (b), the S_3/S_4 half-bridge is on the top side of the PCB board for the soak time control. The clamping circuit is installed upon the switch S_4, the location of which is also close to the DUT S_2 on the back side. Two through holes are placed for the junction temperature monitoring.



(a) (b)

Fig. 14: Pulsed test setup (a) bottom view, (b) top view.

Fig. 15 shows the tested dynamic $R_{DS(on)}$ results with soak time control. The different colors indicate different soak times. It can be seen that the dynamic $R_{DS(on)}$ is dependent on the soak time. As this paper focuses on the hard-switching half-bridge system loss and its distribution, the continuous test can be more meaningful and might be more practical in a real-world scenario.

For a Buck converter, the low-side device operates under SR, whereas, for a Boost converter, the low-side device is hard-switched. Therefore, the Buck converter can be used to extract the dynamic $R_{DS(on)}$ values for the SR device and the Boost converter can be used to extract the dynamic $R_{DS(on)}$ values for the HS device.

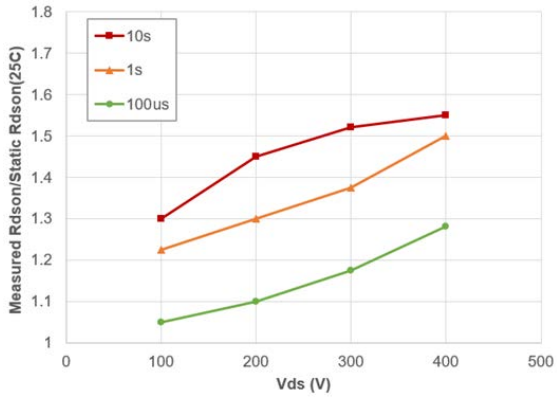


Fig. 15: Measured dynamic $R_{DS(on)}$ at different soak times and voltages.

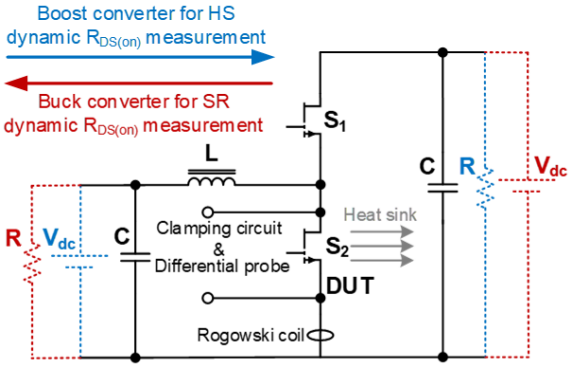


Fig. 16: Continuous mode test diagram for Buck or Boost converter.

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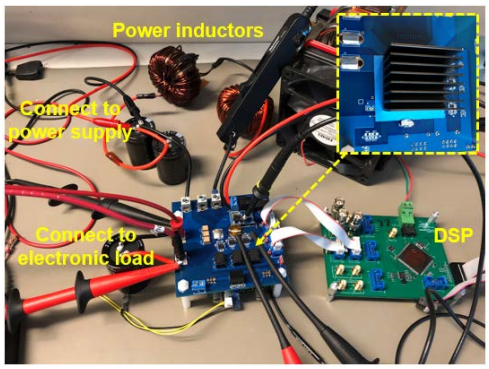

Fig. 17: Continuous mode test setup for dynamic $R_{DS(on)}$.

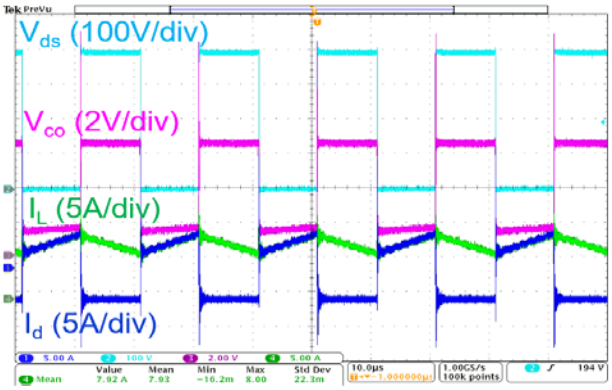

Fig. 18. Waveforms of Continuous test for dynamic $R_{DS(on)}$ measurement.

The diagram and setup of the Boost converter tests are shown in Fig. 16 and 17, respectively. The operating waveforms of the Boost converter are shown in Fig. 18. It can be observed that the precision of 2 V/div can be achieved for the on-state voltage measurement without overdriving the oscilloscope.

IV. Power Loss Modeling of GaN-Based Half-Bridges

A. Modeling of Switching Energy Loss E_{on}/E_{off}

An E_{on}/E_{off} scaling model has been developed in [35], where the E_{on}/E_{off} can be scaled from a normal operating condition to different operating voltage V_{ds}, gate resistance R_g, and junction temperature T_j.

For GaN E-HEMTs, E_{on} is temperature dependent because the transconductance g_m is decreased with the increase of T_j. The transfer characteristics of GS66508T with different T_j at V_{ds}=9 V is shown in Fig. 19.

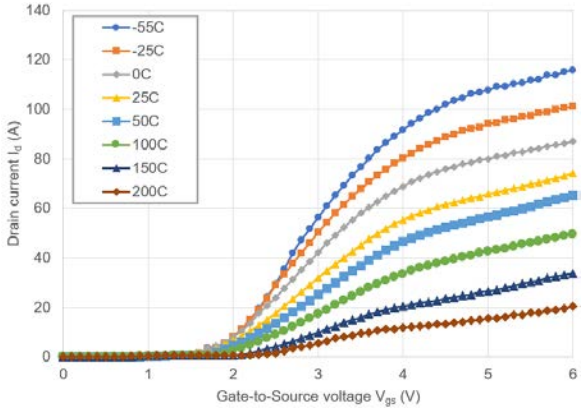

Fig. 19. Transfer characteristics at V_{ds}=9V of GS66508T.

An average transconductance g_m as a function of T_j for GS66508T can be obtained,

$$g_{m(Tj)} = 0.0011T_j^2 - 0.317T_j + 31.14 \quad (14)$$

Therefore, E_{on} can be scaled to different temperatures with the equation below

$$E_{on(Tj2)} = \left(E_{on(Tj1)} - E_{qoss}\right) \cdot \sqrt{\frac{g_{m(Tj1)}}{g_{m(Tj2)}}} + E_{qoss} \quad (15)$$

Fig. 20 shows a comparison between the modeled and measured E_{on} and E_{off} of a GS66508T GaN HEMT at 400 V and different junction temperatures. As can be seen, E_{on} increases with the T_j increasing, but E_{off} is relatively constant with temperature. And the model can predict the temperature-dependent E_{on} well.

Meanwhile, both $E_{V/I}$ and capacitance loss E_{oss}/E_{qoss} are dependent on V_{ds}. The relation between E_{oss}/E_{qoss} and V_{ds} can be found in Fig. 21. This is based on equations (3) and (4). The reason for the difference between E_{oss} and E_{qoss} is that the E_{oss} energy loss is the capacitance loss from the C_{oss} of the device itself, while E_{qoss} energy loss is the capacitance loss from the C_{oss} of the opposite device [4]. The equivalent CV curves for E_{oss}/E_{qoss} can be obtained, as shown in Fig. 22. As a result, the E_{qoss} loss is higher than E_{oss}, due to the high nonlinearity of C_{oss} of semiconductor power devices over the drain-source voltage.

The operating voltage and voltage falling/rising time affect the $E_{V/I}$ loss for both turn-on and turn-off. The voltage falling/rising time scaling can be obtained as,

$$\frac{T_{v1}}{T_{v2}} = \frac{V_{ds1} \cdot C_{rss\_tr1}}{V_{ds2} \cdot C_{rss\_tr2}} \quad (16)$$

where C_{rss_tr} is the time-related reverse transfer capacitance C_{rss} at the corresponding operating voltage level.

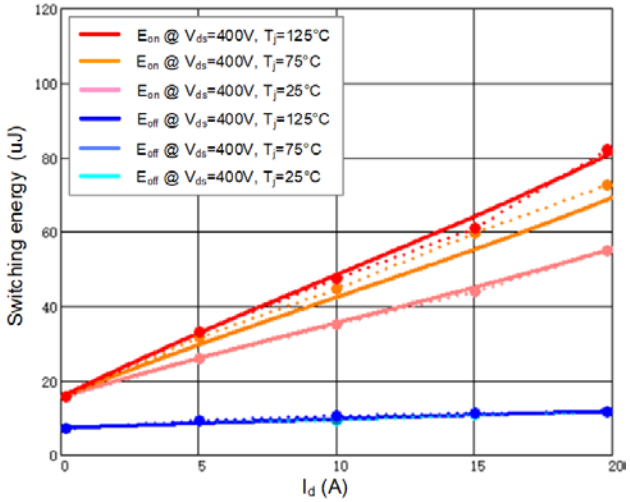

Fig. 20. Comparison between the modeled and measured E_{on} and E_{off} at V_{ds}=400 V with T_j variations (calculated results in solid lines and measurements in dashed lines).

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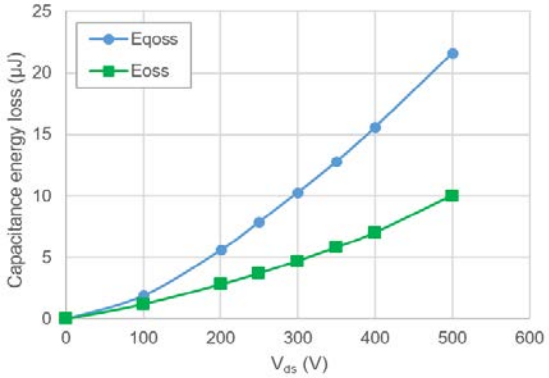

Fig. 21. Calculated E_{oss} and E_{qoss} of GS66508T versus the V_{ds}.

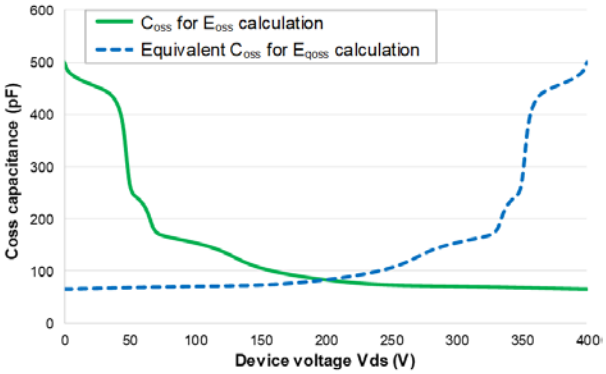

Fig. 22. Equivalent CV curves for capacitance loss E_{oss}/E_{qoss}.

As the voltage and capacitance charge Q is proportional to the V/I overlapping loss energy $E_{V/I}$, the desired $E_{V/I(yV)}$ at voltage y can be scaled from the known energy loss $E_{V/I(xV)}$ at voltage x,

$$\frac{E_{V/I(yV)}}{E_{V/I(xV)}} = \frac{V_{ds(y)} \cdot Q_{(yV)}}{V_{ds(x)} \cdot Q_{(xV)}} \tag{17}$$

Finally, the V_{ds} scaling equations for E_{on} and E_{off} can be obtained in (18) and (19), respectively, where $E_{on/off(xV)}$ is the known energy loss at voltage x and $E_{on/off(yV)}$ is the scaled total E_{on}/E_{off} energy loss at voltage y.

In addition, the definition of Q_{gs_sw} is also given as below,

$$Q_{gs\_sw} = Q_{gs} \cdot \left(\frac{V_{plat} - V_{th}}{V_{plat}} \right) \tag{20}$$

where V_{plat} is plateau voltage and Q_{gs} is the gate-to-source charge.

Fig. 23 shows the curves of the modeled and measured E_{on} and E_{off} of GS66508T at 25 °C and different operating voltages. It can be seen that both E_{on}/E_{off} can be scaled and modeled to other V_{ds} voltages pretty well.

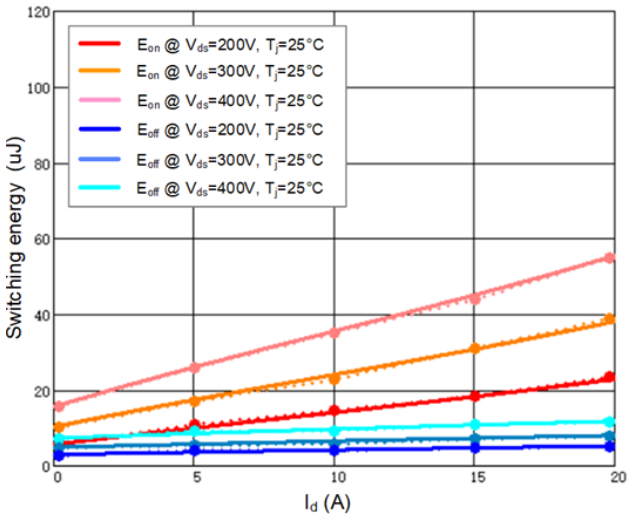

Fig. 23. Comparison between modeled and measured E_{on} and E_{off} at T_j=25°C with V_{ds} variations (calculated results in solid lines and measurement results in dashed lines).

B. *Decoupling Analysis and Modeling of $R_{DS(on)}$*

Before the dynamic $R_{DS(on)}$ tests, all the GaN HEMTs are characterized with static tests, and the dependence of the static $R_{DS(on)}$ on the junction temperature is shown in Fig. 24. The factor k_{Tj} is defined as the normalized increase of $R_{DS(on)}$ due to the heating effect:

$$k_{Tj} = \frac{R_{DSon(Tj)}}{R_{DSon(25°C)}} - 1 \tag{21}$$

From Fig. 24, it can be seen that the k_{Tj} at 75°C and 125°C are 0.49 and 1.12, respectively. Over the considered junction temperature range [0 °C, 150 °C], the factor k_{Tj} can be fitted as a function of T_j, i.e.,

$$k_{Tj}(T_j) = 3.39 \times 10^{-7} \times T_j^3 - 3.19 \times 10^{-5} \times T_j^2 + 9.55 \times 10^{-3} \times T_j - 0.21 \tag{22}$$

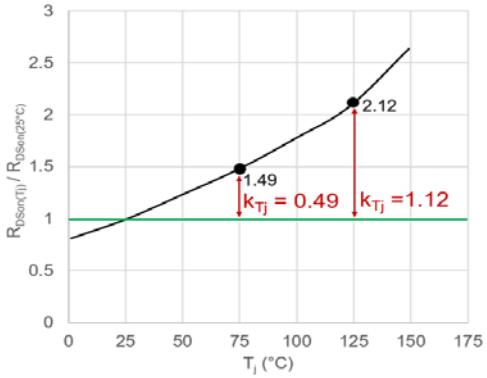

Fig. 24. Dependence and characterization of the static $R_{DS(on)}$ of GaN HEMTs on the junction temperature T_j.

$$E_{on(yV)} = \left(E_{on(xV)} - E_{qoss(xV)}\right) \cdot \frac{V_{ds(y)} \cdot \left(V_{ds(y)} \cdot C_{rss\_tr(yV)} + Q_{gs\_sw}\right)}{V_{ds(x)} \cdot \left(V_{ds(x)} \cdot C_{rss\_tr(xV)} + Q_{gs\_sw}\right)} + E_{qoss(yV)} \tag{18}$$

$$E_{off(yV)} = \left(E_{off(xV)} - E_{oss(xV)}\right) \cdot \frac{V_{ds(y)} \cdot \left(V_{ds(y)} \cdot C_{rss\_tr(yV)} + Q_{gs\_sw}\right)}{V_{ds(x)} \cdot \left(V_{ds(x)} \cdot C_{rss\_tr(xV)} + Q_{gs\_sw}\right)} + E_{oss(yV)} \tag{19}$$

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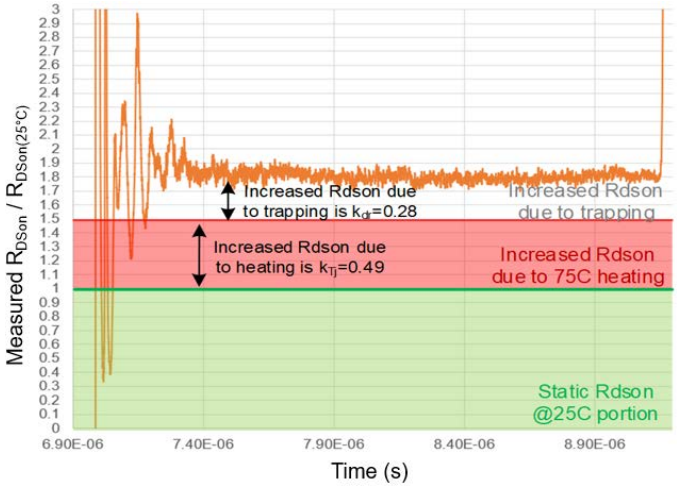

Fig. 25. $R_{DS(on)}$ quantitative analysis at V_{ds}=400 V and T_j=75 °C

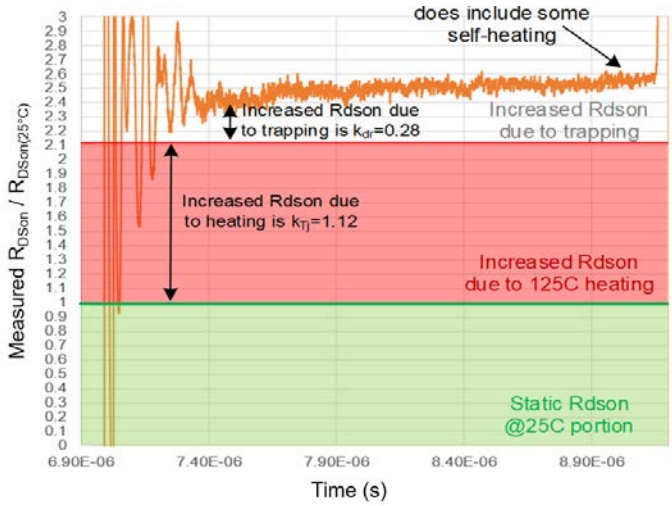

Fig. 26. $R_{DS(on)}$ quantitative analysis at V_{ds}=400 V and T_j=125 °C.

By knowing the T_j and the total measured $R_{DS(on)}$, an $R_{DS(on)}$ decoupling analysis can be conducted. Two examples are shown in Fig. 25 and Fig. 26. As the T_j is known, the measured $R_{DS(on)}$ can be decoupled into three portions: the green portion is the static $R_{DS(on)}$ at 25 °C which is equal to 1; the red portion is the increased $R_{DS(on)}$ from heating effect, which is also the k_{Tj} value; the rest can be considered as the increased $R_{DS(on)}$ due to trapping effect and is defined as k_{dR} factor.

These two cases share the same operating conditions except for the junction temperature. As can be seen from Figs. 25 and 26, the k_{dR} factor stays almost the same in both cases. However, at T_j = 125 °C, the measured $R_{DS(on)}$ rises with time, and this can be explained as self-heating. As the junction temperature is high (125 °C) in Fig. 26, the hard-switching turn-on loss and conduction loss generated during this pulse test can be relatively high. These losses will cause extra junction temperature increase and thus, it is easier for the device to be self-heated. Therefore, as a short conclusion for the decoupling analysis, the k_{dR} factor is relatively temperature independent in the range from 25 °C to 125 °C, which is applicable to most applications.

More tests under different T_j and V_{ds} have been conducted and both the k_{Tj} and k_{dR} factors are summarized in Fig. 27.

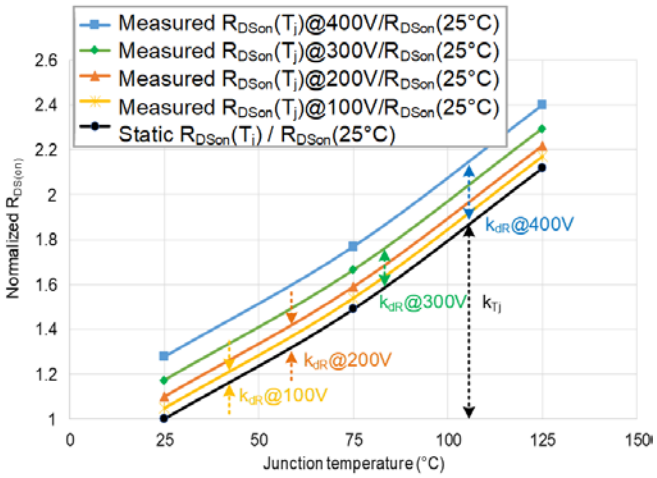

Fig. 27: Dependence and characterization of the static $R_{DS(on)}$ of GaN HEMTs on the junction temperature T_j.

V. Experimental Verification and Loss Distribution Discussion

A. Experimental Verification

Continuous tests are performed at different loads and switching frequencies to verify the proposed power loss model. The test setup is shown in Fig. 17. During the Boost converter test, the input and output voltages are kept constant which are 200 V and 400 V, respectively. However, for the Buck converter test, the input and output are swapped. The system cooling method is forced air convection. The applied V_{gs} voltage is +6/-3V for turn-on and turn-off and external gate resistance is 10 Ω and 2 Ω for turn-on and turn-off, respectively. The applied deadtime in the DSP between the high-side and low-side devices is 120 ns. The junction-to-ambient thermal resistance is 8.7 °C/W, and the ambient temperature is 25 °C.

In order to prevent overheating on the current shunt, a Rogowski coil is applied to measure the drain current for the DUT for the continuous test. Due to the limitation on the bandwidth of the Rogowski coil, the E_{on} and E_{off} switching losses cannot be measured simultaneously due to delay of current rising or falling transition. Therefore, the E_{on} and E_{off} modeling method can be used to scale the switching energy as a post-process for continuous operation tests by taking the settled value of current from the Rogowski coil which is independent to its bandwidth. The on-state resistance and device package temperature can be measured in real time to conduct the the $R_{DS(on)}$ decoupling analysis in real time. As a result, all power losses are measured and modeled. The power loss modeling and measurement procedure is shown in Fig. 28.

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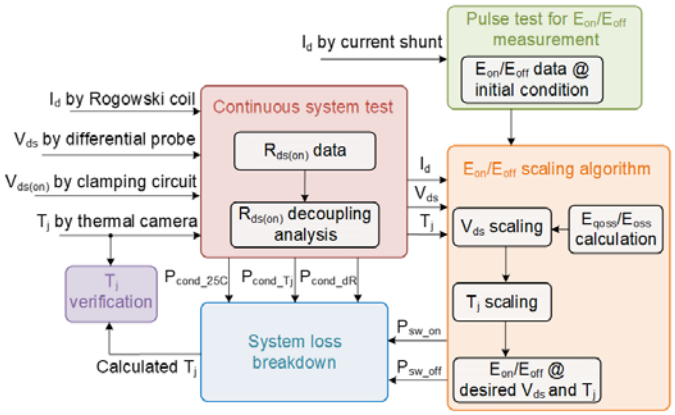

Fig. 28: Procedure of power loss modeling and measurement.

Fig. 29 shows the power loss breakdown of the hard-switching half-bridge system at different loads and switching frequencies. It is seen from Fig. 29 that with the increase of power load, the junction temperature is increased, and the dynamic $R_{DS(on)}$ loss becomes less significant than the heating effect. In fact, the dynamic $R_{DS(on)}$ related power loss always represents a small portion of the total system power loss. Instead, it is the switching loss that has the most effect on the system power loss at switching frequencies over 20 kHz.

In fact, in order to validate the proposed power loss model, the junction temperature can be calculated and compared with the measured temperature from the thermal camera. The calculated T_j can be obtained by,

$$T_j = R_{th(ja)} \cdot E_{loss} \cdot f_{sw} + T_{amb} \quad (23)$$

where $R_{th(ja)}$ is the thermal resistance from junction to ambient and T_{amb} is the ambient temperature.

The comparison between the measured and modeled junction temperatures of the HS and SR GaN E-HEMTs at different switching frequencies are shown in Fig. 30. It is clear that the model can predict the junction temperature of the device well. The maximum temperature error is 2.1 °C.

The half-bridge efficiency with/without dynamic $R_{DS(on)}$ can be compared and plotted in Fig. 31. It can be seen that the efficiency impact is in the range from 0.03% to 0.08%. On average, the dynamic $R_{DS(on)}$ contribute about 0.05% efficiency drop to this hard-switching half-bridge. Since this paper focuses on the power loss characterization and modeling of GaN-based hard-switching half-bridges, the losses of other components, e.g., the power inductor and capacitor, are not considered for converter systems.

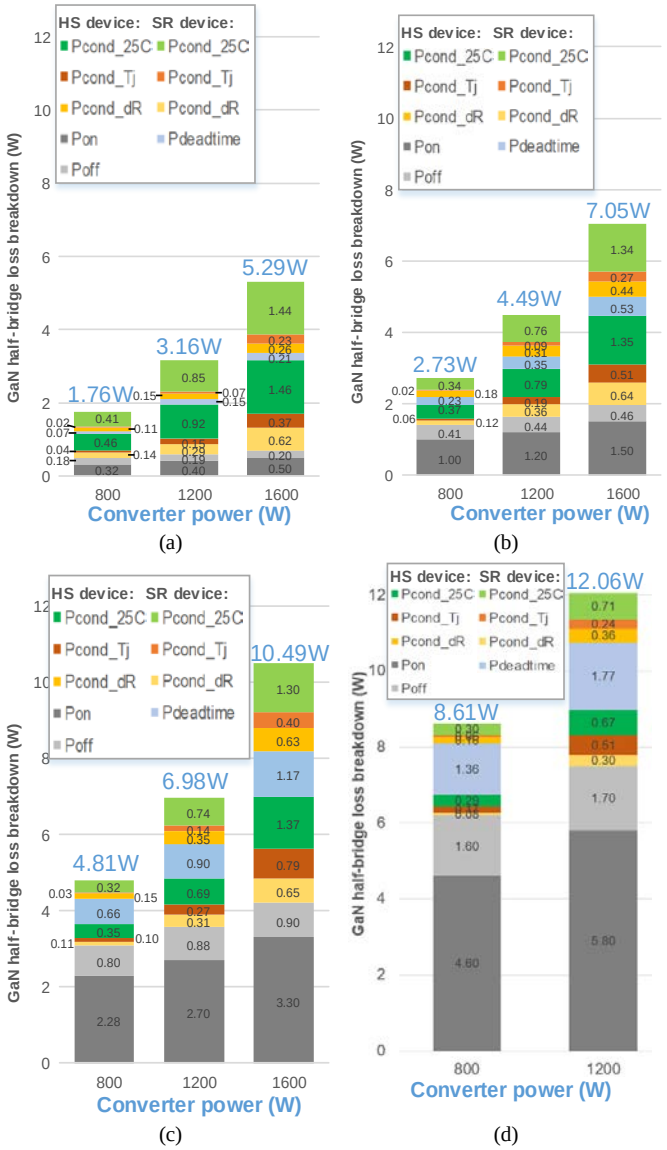

Fig. 29: Power loss breakdown of hard-switching GaN E-HEMTs under different loads and switching frequencies (a) f_{sw}=20 kHz, (b) f_{sw}=50 kHz, (c) f_{sw}=100 kHz, (d) f_{sw}=200 kHz.

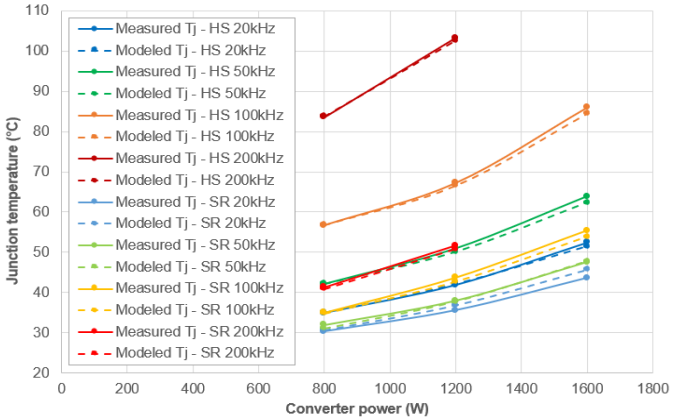

Fig. 30: Comparison of the measured and calculated junction temperatures.

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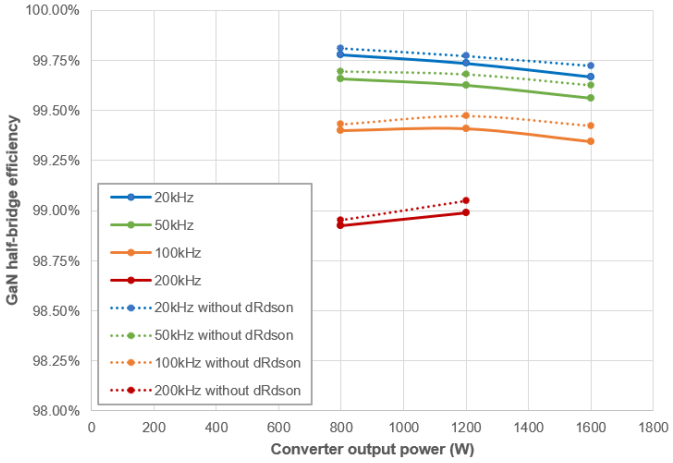

Fig. 31: Efficiency comparison of the GaN E-HEMT half-bridge with and without considering dynamic $R_{DS(on)}$. It is noted that the power losses of the inductor and capacitor are not taken into account.

B. Discussion on Loss Distribution and Efficiency Improvement

The detailed loss breakdown is relatively useful for engineers and researchers, if the target is to further improve the GaN-based half-bridge system efficiency. For example, it is quite clear that the dominant losses under high-frequency hard-switching are switching loss E_{on}/E_{off} and deadtime loss.

In switching loss, the I/V overlapping loss $E_{V/I}$ in E_{off} is relatively small, due to the fast switching-off speed of GaN. Typically, a small value of $R_{g(off)}$ is required to provide a low impedance path for the Miller current, such that most Miller current is dumped into the driver, instead of flowing into the gate of the device. While the $E_{V/I}$ in E_{on} is relatively bigger and it is more gate-resistance dependent. In this paper, the applied $R_{g(on)}$ is 10 Ω. By reducing the $R_{g(on)}$, the $E_{V/I}$ can be reduced further. The other loss part in E_{on}/E_{off} is capacitance loss E_{qoss}/E_{oss}, which is dependent on the parasitic capacitance. The overall parasitic capacitance in the circuit includes the C_{oss} from switching devices, the parasitic capacitance from power inductor and PCB [4]. Therefore, a good PCB layout with minimized parasitic capacitance in the circuit can help reduce this loss.

On deadtime loss, it is important to reduce the length of deadtime. As this paper's target is to present the loss breakdown in a typical operating scenario, the half-bridge efficiency is not fully optimized. The applied deadtime in this test setup is 120 ns. The deadtime can be reduced further if the primary target is to maximize the system efficiency. For the hard-switching converter, the deadtime can be reduced further in the range from 50 ns to 100 ns, while for the soft-switching converter, it is dependent on the desired ZVS range [43]. The deadtime loss is also dependent on the turn-off gate voltage V_{gs}. For the negative turn-off gate voltage, there is a trade-off between the efficiency optimization and converter switching safe operation. As the negative gate drive voltage is applied to prevent the switching device from incorrect triggering and therefore shoot-through, while it does increase the deadtime loss. Therefore, for low-power applications or soft-switching converter, where limited noise is in the circuit, a zero-voltage turn-off gate voltage is feasible. For high-power applications, a negative gate drive voltage is necessary, while it is still possible to reduce the voltage amplitude.

In addition, thermal resistance also plays a critical role in the system losses. As both the switching loss E_{on} and the conduction loss from heating effect increase with temperature increasing. So, with a bigger thermal resistance, the power loss from the self-heating effect is increased. In this paper, the top-cooled device is applied as it is easier to measure the package temperature and therefore junction temperature. The thermal resistance from junction-to-ambient, in this case, is 7.8 °C/W. The thermal resistance can be reduced further by applying a bigger heat sink for the top-cooled device or applying an insulated metal substrate (IMS)-based solution for the bottom-cooled device [44].

VI. Conclusions

In this paper, the test setup and measurements on the dynamic $R_{DS(on)}$ of GaN E-HEMTs have been discussed. Specifically, the clamping circuit design for the on-state voltage measurement on both the HS and SR devices and the junction temperature measurement are presented. Two different test setups, i.e., the DPT-based pulse test with soak time control and the continuous Boost/Buck converter system test, have been conducted. Then, an $R_{DS(on)}$ model for GaN E-HEMTs has been proposed to decouple the trapping and heat effects. Taking into account the dynamic $R_{DS(on)}$, an analytical power loss model is proposed to calculate the power loss of GaN-based half-bridges. Also, a comprehensive power loss breakdown analysis is performed to investigate the percentage of each type of loss in the whole half-bridge system. Finally, the calculation and measurement results of junction temperature are compared to validate the proposed dynamic $R_{DS(on)}$ and power loss models.

Following conclusions are drawn:

- For the studied GaN E-HEMT GS66508T, its dynamic $R_{DS(on)}$ increases monotonically with higher off-state voltages and longer soak time. Therefore, conventional DPT without soak time control can lead to inaccurate measurement and continuous test with junction temperature monitoring is preferred in measuring the dynamic $R_{DS(on)}$.
- The increase of $R_{DS(on)}$ is caused by both the heating and trapping effects which are separately quantified. Two functions, k_{Tj} for the heating effect and k_{dR} for the trapping effect have been introduced to calculate the dynamic $R_{DS(on)}$.
- With the temperature increases, the $R_{DS(on)}$ loss caused by the heating effect can become more significant than that by the trapping effect. From the perspective of the half-bridge system power loss, the dynamic $R_{DS(on)}$ related power loss is insignificant, particularly at high switching frequencies (> 20 kHz). Interestingly, it is found that it is the switching losses E_{on} /E_{off} and the deadtime loss are more dominant in the total power loss of high-frequency GaN-based hard-switching half-bridge. Finally, further efficiency improvement on this half-bridge is also discussed in detail.

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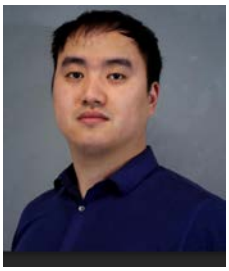

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