

# Robust Large-Port-Count Hybrid Switches with Relaxed Control Tolerances

Q. Cheng, A. Wonfor, R. V. Penty, I. H. White

Centre for Photonic Systems, University of Cambridge, 9 JJ Thomson Avenue, Cambridge, CB3 0FA, United Kingdom

Author e-mail address: [qc223@cam.ac.uk](mailto:qc223@cam.ac.uk)

**Abstract:** The control tolerances of large-port-count optical switches with up to 128×128 ports using the MZI-SOA hybrid design are investigated. The first quantitative analysis is presented showing tolerant control requirements of the hybrid switch design.

**OCIS codes:** (130.4815) Optical switching devices; (130.6622) Subsystem integration and techniques

## 1. Introduction

The ever-continuing growth in data traffic is causing increased demands on network switching capacity, and has led to renewed interest into high-bandwidth, high-speed, but low-energy optical switches [1]. Recent advances in photonic integration technology have scaled the connectivity of a monolithic circuit to tens of connections for future optical packet switching applications [2, 3]. However, building larger port-count high-speed integrated switches imposes stricter requirements on switch design, fabrication and control. We have proposed a scalable integration-compliant optical switch using a novel hybrid MZI-SOA approach [1] and the feasibility of building a 128×128 port-count hybrid switch has been demonstrated [4]. Large-port-count optical switching circuits, however, pose a challenge to their control accuracy, as variations compromise the device optical signal-to-noise ratio (OSNR). Relaxed control requirements are preferable as they allow the switching circuit to operate blind within tolerances.

In this work, we therefore investigate the control tolerances of hybrid switches with up to 128×128 ports. The first quantitative analysis is presented using physical layer simulations fitted using experimental data. This analysis indicates that the hybrid design also enables relaxed control requirements for large-port-count optical switch fabrics.

## 2. Hybrid Switch Design

This work focuses on the hybrid switch which places short SOAs at the outputs of an MZI in a dilated structure as shown in Fig. 1(a). The short SOAs are switched in tandem with the MZIs to pass the wanted signals and strongly absorb the first order leakage signals. Hence, this design enables suppressed crosstalk and gain to overcome excess loss, both of which are essential for large-port-count switches. An N×N port count hybrid switch can be built from identical switch modules, connected via shuffle networks [Fig. 1(b)]. The worst aggregate crosstalk ratio (in dB) of such a switch is estimated by [1]:

$$C = 2X + 20\log_{10}(2\log_2 N - 1) - 23 \quad (1)$$

where  $X$  is the crosstalk ratio of a single MZI cell and  $N$  is the port number. In practice, however, uneven coupler split ratio and excess electro-absorption loss within the phase-shift section of the MZI in a hybrid switch both introduce an intensity imbalance in its two parallel arms which translates into crosstalk. Moreover, the fabrication variability and design constraints further limit the reliably achievable crosstalk for a large matrix integrated device. Currently the reliably attainable crosstalk ratio of a single MZI cell within large-scale photonic integrated circuits lies at -15dB [5]. However, the dilated hybrid design provides increased immunity to performance degradation caused by component variability, achieving crosstalk better than -40dB [4].

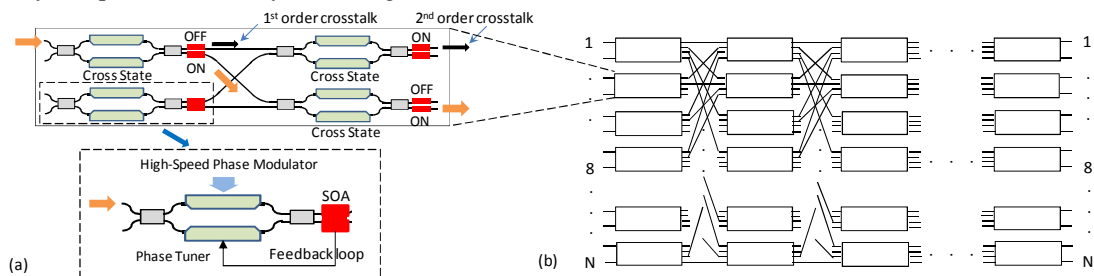


Fig. 1 (a) Schematic of operating principle of the hybrid switch building block. (b) Schematic of the scalable hybrid switch.

## 3. Switch Control Tolerances

As indicated by the bottom figure in Fig. 1(a), the upper phase-shifter of the MZI element acts as a high-speed phase modulator for dynamic switching while the lower one serves as a phase tuner to minimize the phase and electro-

absorption loss difference between the two parallel arms. A feedback loop can be set up, using the integrated SOAs as power detectors, to search the optimum operating points for the phase tuners during a self-learning process. Device control tolerances of the switching voltages to the high-speed phase modulators ( $\Delta V_\pi$ ) and of the bias currents to the short SOAs ( $\Delta I$ ) can thus be determined by the allocated sub-system penalties. The investigation of the control tolerance is based on the worst case in which all signals entering the switch fabric have the same wavelength and the device is fully loaded. The induced crosstalk penalty,  $P$ , can be calculated by the expression [6]:

$$P = -5 \log_{10}(1 - 4q^2 10^{C/10}) \quad (2)$$

where  $C$  is the aggregate circuit crosstalk in dB, and  $q=5.9$  for an error rate of  $10^{-9}$ . Therefore, the required crosstalk-level of a hybrid switch building block for 1dB-penalty operation can be achieved and the switching voltage tolerance can be evaluated using the commercial VPI simulator with parameters fitted from experimental data [7]. Here it is assumed that the MZI elements have a crosstalk ratio of -15dB and that 170  $\mu\text{m}$ -long SOAs are integrated at their outputs. The  $\Delta V_\pi$  is studied for 10Gb/s operation using both single and 10 input wavelengths (with 100GHz spacing) in the C-band. The variation of  $V_\pi$  with wavelength compromises the extinction ratio of the MZI under multiple wavelength operation. The tolerance of the allowed control voltage as a function of port count is plotted in Fig. 2(a). It can be seen that the voltage tolerance decreases as the port count increases. However the 128 $\times$ 128 port size hybrid switch still achieves a  $\Delta V_\pi$  exceeding 0.7V for 10-wavelength operation.

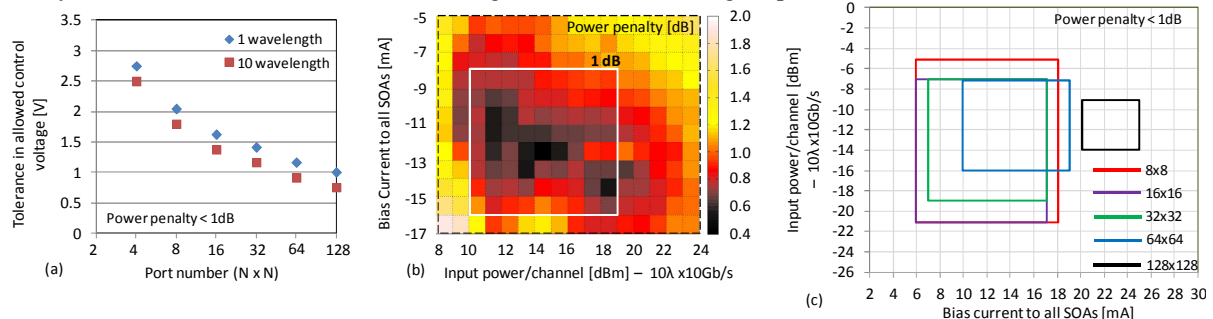


Fig. 2 (a) The tolerance of allowed control voltage as a function of port number. (b) Penalty map for 64 $\times$ 64 hybrid switch as a function of input power and bias current (key shows penalties in dB). (c) Input power and bias tolerance of hybrid switches with 8 $\times$ 8 to 128 $\times$ 128 port count.

The tolerance of bias current of the short SOAs also depends on the input optical powers. The  $\Delta I$  is determined for 10 $\lambda$  $\times$ 10Gb/s operation under worst case operation when all current sources are offset from optimum in the same sense. Figure 2(b) shows a detailed penalty map for a 64 $\times$ 64 port count hybrid switch as a function of both input power and bias variation [1]. The white rectangle outlines the  $\Delta I$  and input power dynamic range (IPDR) for a penalty less than 1dB. Figure 2 (c) summarizes similar data for 8 $\times$ 8, 16 $\times$ 16, 32 $\times$ 32, 64 $\times$ 64 and 128 $\times$ 128 port count hybrid switches. It shows that the  $\Delta I$  and IPDR are 12mA and 16dB respectively for an 8 $\times$ 8 hybrid switch, decreasing to 5mA and 5dB respectively when the port number increases to 128 $\times$ 128.

#### 4. Conclusions

Large-port-count high-speed integrated switches not only impose strict requirements on switch design and fabrication but also on control accuracy. This paper for the first time investigates the control tolerances for large-port-count optical switches using the hybrid switch approach. Quantitative analysis using physical layer simulations fitted with experimental data is presented. A 128 $\times$ 128 port count features a relaxed tolerance of 0.7V and 5mA on the voltage and bias current respectively for 10Gb/s  $\times$  10-wavelength operation with sub-system penalties less than 2dB. This demonstrates that the hybrid switch enables both very good scalability and control tolerance.

#### 5. Acknowledgment:

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