Desynchronizing Paralleled GaN HEMTs to Reduce Light-Load Switching Loss

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Abstract—Parallel connection of GaN high-electron-mobility transistors (HEMTs) is a more cost-effective or even an unavoidable solution to achieve higher current ratings. As the load decreases, however, the switching loss of paralleled HEMTs becomes dominant over the conduction loss, and the overall power conversion efficiency drops sharply. To reduce the light-load switching loss, this paper proposes a desynchronizable paralleling scheme. The midpoint (AC terminal) of each paralleled HEMT half bridge is connected with a commutation inductor, which thus, enables two operation modes: synchronous and asynchronous modes. The synchronous mode is activated at heavy loads to share the high current; the added commutation inductors lead to better current sharing than the direct parallel. When operating at light loads, however, the paralleled devices are desynchronized to generate a circulating current flowing through the commutation inductors. The circulating current enables the lagging HEMTs to achieve the zero-voltage switching (ZVS) and allows the leading ones to turn on at a current lower than the load, thereby significantly reducing the total switching loss. In addition, a thermal balancing scheme is proposed to alleviate the thermal stress imbalance between the desynchronized GaN HEMTs. The operating principle and design guidelines of the desynchronizable paralleling scheme are detailed. Finally, experimental results from multi-pulse and continuous tests of GaN HEMTs are provided to verify the advantages of the proposed paralleling scheme in reducing light-load switching loss and improving light-load efficiency.

Index Terms—Parallel of GaN HEMTs, desynchronized parallel, commutation inductors, switching loss, ZVS, light-load efficiency

I. INTRODUCTION

C ompared with Si counterparts, GaN enhancement-mode high-electron-mobility transistors (HEMTs) feature a higher switching speed and lower switching loss. Thus, it is easier for GaN-based power electronics converters to achieve high efficiency and high power density. Hence, GaN HEMTs have been applied to various industrial and consumer products such as photovoltaic (PV) converters [1], on-board electric vehicle (EV) chargers [2], motor drives [3], and portable chargers [4].

The on-state resistance $R_{ds,on}$ of GaN HEMTs has a strong dependency on the junction temperature $T_J$, e.g., the $R_{ds,on}$ of GS66508T is tripled when $T_J$ increases from 0 °C to 137 °C [5]. To reduce the conduction loss and maintain high efficiencies in high-current and high-temperature conditions, it is desired to adopt high-current-rating GaN HEMTs. To date, the maximum current rating of commercial 650-V GaN HEMTs is 60 A, i.e., GS66516T [6]. However, it is challenging to use unparalleled GS66516T devices (size: 9.0 mm × 7.6 mm × 0.54 mm) in high power applications (e.g., >10-kW motor drives) due to the caused high power loss and high thermal stress [7]. Furthermore, in many cases, the price of GaN HEMTs varies nonlinearly with the current rating; one high-current device can be much more expensive than multiple low-current counterparts, e.g., GS66516T×1 for $46.96, versus GS66508T×2 for $27.84 [8]. Therefore, parallel connection of power devices can be a cost-effective or even an unavoidable solution for power electronic converters [9]–[17].

When operating at light loads, however, the switching loss of the paralleled HEMTs dominates over the conduction loss, which deteriorates the light-load efficiency performance. Meanwhile, the light-load operation represents the dominant use in many operating environments, e.g., microprocessors [18], PV [19] and EVs [20]; reducing the light-load switching loss may contribute to a remarkable energy efficiency improvement [21], [22]. Accordingly, it is desired to develop a paralleling technique that is able to lower both the light-load switching loss and the heavy-load conduction loss.

The dynamic turn-on/off speed/timing mismatches among paralleled power semiconductor devices occur frequently due to the inevitable differences from the gate delay, threshold voltage $V_{gs,th}$, transconductance $g_f$, junction temperature $T_J$, gate resistance $R_g$, parasitic capacitance, and parasitic inductance [10]–[12], [15], [23]–[31]. Therefore, many paralleling techniques have been proposed to improve the current sharing performance among paralleled semiconductor power devices. Specifically, refs. [24]–[28] actively control the gate resistance or delay times of paralleled devices to balance the transient currents. However, these approaches need multiple high-bandwidth current sensors and analog feedback control which are difficult to fabricate and complicated to implement [14], [17], [30], [31]. Recently, the passive current balancing approaches [14], [17], [29]–[31] become popular due to their simplicity and robustness. In these works, inversely-coupled inductors are added to the paralleled SiC and GaN transistors; a high differential-mode impedance can be formed and it is able to alleviate the current imbalance among paralleled devices. However, these techniques cannot reduce the low-current switching loss that is dominant in the total light-load power losses of high-frequency power converters.

The multiphase interleaving of half-bridge (HB) legs (e.g., the synchronous buck converter and the intercell transformer for inverters) is able to reduce the output filter size and to enhance the dynamic response performance of converters [32]–[35]. To improve the light-load efficiency, multiple techniques, e.g., the pulse skipping, pulse frequency modulation, half-full-bridge switching, constant ON time, and phase shedding, have been proposed in the literature [21], [22], [34], [36]–[40].

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Among them, the most popular scheme for the multiphase interleaved systems is to adjust the operational phase number based on the load current condition [21], [32], [34], [40]. However, the multiphase interleaving requires relatively large (> several hundreds of μH) inductors, which are normally not desired in some inductive-load applications, e.g., motor drives, due to the added power loss, cost and volume [41], [42]. Recently, the triangular-current-mode (TCM) multiphase interleaving has attracted increasing research attention owing to its soft-switching characteristics for all switches [43]–[45]. This approach requires high-speed zero current detection (ZCD) and accurate timing for the zero-voltage switching (ZVS) realization, and therefore its implementation complexity is high [30], [46], [47].

To reduce the light-load switching loss of parallel-connected GaN HEMTs, this paper proposes a desynchronized control scheme for the first time. In the scenario of low load currents, the paralleled HB legs are desynchronized at their turn-on instants; thus, a small circulating current can be generated, whereas the asynchronous-mode thermal stress deviation between the leading and lagging GaN HEMTs, this paper proposes a desynchronized control scheme for the first time. In the scenario of low load currents, all the paralleled HEMTs are driven synchronously to share the high current and to reduce the total power loss; the small commutation inductors added to the midpoints of paralleled HB legs lead to better transient current sharing performance than the direct parallel.

The remainder of this paper is organized as follows: the switching loss characteristics of paralleled GaN HEMTs and the derivation of the proposed desynchronizable parallelizing structure are presented in Section II. Section III details the operating principles of the proposed parallelizing technique in both the synchronous and asynchronous modes before Section IV presents design guidelines and a thermal balancing scheme. After that, the experimental results of multi-pulse and continuous tests are provided in Section V for proposal verification. Finally, conclusions are drawn in Section VI.

II. DERIVATION OF PROPOSED DESYNCHRONIZABLE PARALLELIZING STRUCTURE

A. Switching Loss Breakdown of GaN HEMTs

Typical hard-switching (HS) waveforms of a GaN HEMT are shown in Fig. 1(a) and (b), and the measured switching losses of paralleled GaN HEMTs (GS66508T×1, GS66508T×2, and GS66516T×1) are shown in Fig. 1(c). As can be seen, both the turn-on and turn-off energy losses \( E_{on} \) and \( E_{off} \) are composed of two portions, i.e., the current-independent capacitive losses \( E_{qoss} \) and \( E_{oss} \), and the current-dependent losses \( E_{on,VI} \) and \( E_{off,VI} \) [43].

The energy loss \( E_{oss} \) of \( N \) paralleled GaN HEMTs is introduced by the self-discharging current of their output capacitance, whereas \( E_{qoss} \) is caused by the capacitive charging current from the opposite switching devices [48]–[50]. The two types of losses \( E_{oss} \) and \( E_{qoss} \) can be obtained as

\[
E_{oss}(V_{ds},N) = \int_{0}^{V_{dc}} v_{ds} NC_{oss}(v_{ds}) dv_{ds} \quad (1)
\]

\[
E_{qoss}(V_{dc},N) = \int_{0}^{V_{dc}} (V_{dc} - v_{ds}) NC_{oss}(v_{ds}) dv_{ds} = V_{dc} N Q_{oss}(V_{dc}) - \int_{0}^{V_{dc}} v_{ds} NC_{oss}(v_{ds}) dv_{ds} = V_{dc} N Q_{oss}(V_{dc}) - E_{oss}(V_{dc},N) \quad (2)
\]
where $V_{dc}$ is the dc bus voltage, $C_{oss(v_{ds})}$ denotes the $v_{ds}$-dependent output capacitance of a GaN HEMT, and $Q_{oss(V_{ds})}$ is the charge stored in one output capacitor at $v_{ds} = V_{dc}$. The output capacitance $C_{oss}$ of a GaN HEMT nonlinearly decreases with respect to the increase of $v_{ds}$; as a result, $E_{goss}$ is larger than $E_{oss}$ at the same $V_{dc}$. It is seen from (1) and (2) that both $E_{goss}$ and $E_{oss}$ are independent of the switching current and junction temperature; instead, these two capacitive losses are directly proportional to the number of GaN HEMTs in parallel, $N$, and the dc bus voltage $V_{dc}$, as indicated in (1c). However, for the losses $E_{on,V1}$ and $E_{off,V1}$, they are determined by the switching current, junction current, and gate resistance [49].

From Fig. (1c), it is also seen that the losses $E_{on,V1}$ and $E_{off,V1}$ are dominant at high load currents. As the load current decreases, the fixed capacitive losses $E_{oss}$ and $E_{goss}$ then make up a higher proportion in the total switching loss. In particular, at medium and low load currents, $E_{off}$ is mainly determined by $E_{oss}$ due to the small $E_{off,V1}$. This is because the two-dimensional electron gas (2DEG) conducting channel of a GaN HEMT can be fast cut off before the voltage of the nonlinear output capacitance, i.e., $v_{ds}$, rises significantly [52].

### B. Derivation of Desynchronizable Parallelling Structure

As seen from Fig. (1c) and (d), at high currents, more GaN HEMTs in parallel (i.e., a larger $N$) leads to lower switching and conduction losses; at low currents, however, it results in a higher switching loss that dominates the total light-load power loss. In order to reduce the power loss in the whole load range, it is desired to flexibly adjust the effective number of HEMTs in parallel based on the load current. It seems sensible to separately drive the paralleled HEMTs in Fig. (2a) and to keep some legs off at light loads. However, this method actually causes much higher switching losses than a single device or more in parallel because the effective output capacitance of the paralleled HEMTs remains but the active HEMTs have to turn on and turn off at the full load current.

By adding small commutation inductors, i.e., $L_1$, $L_2$, ..., $L_N$, to the midpoints of the paralleled GaN HEMT half bridges, we can obtain a desynchronizable parallelling structure, as shown in Fig. (2b). It enables both the synchronous and asynchronous operations for the paralleled HBs. Typically, the output filter inductance $L_o$ is significantly larger than the commutation inductance, i.e., $L_o \gg L_1 = L_2 = ... = L_N$, but still, the commutation inductors can act as part of $L_o$.

It should be noted that GaN enhancement mode HEMTs do not have an intrinsic body diode, and the added body diodes in Fig. (2) are used to facilitate the commutation analysis below.

### III. OPERATING PRINCIPLES OF PROPOSED DESYNCHRONIZABLE PARALLELLING STRUCTURE

#### A. Synchronous Mode

When the load current is high, it is desired to synchronously switch the paralleled HEMTs such that the conduction and switching losses can be reduced, as indicated in Fig. (1c).

The operating waveforms of the desynchronizable parallelling structure in the synchronous mode are shown in Fig. (3).

The $N$ low-side switches $S_{Ln}, n = 1, 2, ..., N$, (the DUTs), are turned on at $1/N$ of the load current $I_{L_o}$, which is similar to the conventional parallelling structure without commutation inductors. However, the addition of commutation inductors leads to better transient current sharing characteristics than the conventional structure, as illustrated below.

The equivalent circuit of the proposed parallelling structure (cf. Fig. (2b)) is shown in Fig. (3). Considering an ideal switching process, i.e., both the turn-on and turn-off times are equal to 0, we can obtain that the midpoint voltages $v_{og}(n = 1, 2, ..., N)$ is equal to either 0 or $V_{dc}$.

The commutation inductor currents, $i_{L1}, i_{L2}, ..., i_{LN}$, can be decoupled into the common-mode current $i_{CM}$ and the differential-mode currents $i_{DM1}, i_{DM2}, ..., i_{DMN}$. By definition, the common-mode and differential-mode currents can be obtained as

\[
i_{CM} = \frac{1}{N} \sum_{n=1}^{N} i_{Ln} = \frac{I_{L_o}}{N} \tag{3}
\]

\[
\left\{
\begin{aligned}
  i_{DM1} &= i_{L1} - i_{CM} \\
  i_{DM2} &= i_{L2} - i_{CM} \\
  &... \\
  i_{DMN} &= i_{LN} - i_{CM}
\end{aligned}
\right. \tag{4}
\]

It is seen from (4) that the real current difference among the commutation inductors is equal to the difference of their differential-mode currents. If all the paralleled GaN HEMT HBs are exactly the same and also they are synchronized, then $i_{DM1} = i_{DM2} = ... = i_{DMN} = 0$, and $i_{L1} = i_{L2} = ... = i_{LN} = \frac{I_{L_o}}{N}$, which implies that current sharing can be achieved for the commutation inductors and the paralleled GaN HEMT HBs.

In practice, however, the dynamic turn-on/-off speed/timing mismatch of paralleled GaN HEMTs is inevitable due to the differences from the gate delay, threshold voltage $V_{gs,th}$, transconductance $g_{fs}$, junction temperature $T_j$, gate resistance $R_g$, parasitic capacitance, and parasitic inductance [10]. As a result, the voltages of HB midpoints ($v_{1}, v_{2}, ..., v_{N}$) and those across the commutation inductors ($v_{O1}, v_{O2}, ..., v_{NO}$) are misaligned with each other.

In the first step, it is assumed that $n_{td} (1 \leq n_{td} \leq N - 1)$ of the $N$ paralleled HBs are leading the remaining $N - n_{td}$ ones by a time delay of $\Delta \tau$. In this case, the midpoint voltages and the unbalanced inductor currents are shown in Fig. (3b).
The generated differential-mode currents flowing through each leading leg and each lagging leg can be obtained as

\[
\begin{align*}
I_{DM,ld} &= \frac{V_{dc}}{L_c} \Delta \tau (N - n_{ld}) \\
I_{DM,lg} &= \frac{V_{dc}}{L_c} \Delta \tau n_{ld}
\end{align*}
\]  

Thus, the maximum current difference between the leading and lagging legs is obtained as

\[
\Delta I_{L,max} = |I_{DM,ld} - I_{DM,lg}| = \frac{V_{dc} \Delta \tau}{L_c}
\]  

In a general case, the time delays of the \(N\) paralleled GaN HBs may differ with each other, as shown in Fig. 5(c). The maximum current difference is between the earliest leg and the latest leg, i.e., between \(i_{L1}\) and \(i_{LN}\) in Fig. 5(c).

According to [5], the generated current difference between \(i_{Ln}\) and \(i_{Ln+1}\) for \((n = 1, 2, \ldots, N - 1)\) within the interval \([\tau_n, \tau_{n+1}]\), i.e., \(\Delta I_L, \Delta \tau_n\), can be obtained as

\[
\Delta I_L, \Delta \tau_n = \frac{V_{dc} \Delta \tau_n}{L_c}
\]  

The maximum inductor current imbalance \(\Delta I_{L,max}\) can be obtained by

\[
\Delta I_{L,max} = \sum_{n=1}^{N-1} \Delta I_L, \Delta \tau_n = \frac{V_{dc} \Delta \tau}{L_c}
\]  

As can be seen, the maximum inductor current imbalance is independent of \(N\) and \(N_{ld}\), but is determined by the maximum time delay among the \(N\) parallel GaN HEMT legs and the commutation inductance \(L_c\).

The analysis above is based on the assumption that the rise and fall time of the midpoint voltages, \(t_r\), equals 0. In practice, however, \(t_r > 0\). Neglecting and considering the rise and fall time \(t_r\), the voltage and current waveforms of two commutation inductors \(L_m\) and \(L_n\) for \((n = 1, 2, \ldots, N - 1)\) are shown in Fig. 6. The voltage \(v_{nm}\) represents the difference between two random midpoint voltages \(v_n\) and \(v_m\), i.e., \(v_{nm} = v_n - v_m\). \(\Delta I_{L,m,n}\) and \(\Delta I_{L,m,n}\) denote the current variations of \(i_{Ln}\) and \(i_{Lm}\) caused by \(v_{nm}\), i.e.,

\[
-\Delta i_{L,m,n} = \int_{t_0}^{t_f} v_{nm}(t) dt = \frac{1}{2 L_c} A_{vnm}
\]  

where \(A_{vnm}\) represents the volt-second product of \(v_{nm}\) during \([t_0, t_f]\), i.e., the shaded areas in Fig. 6. Regardless of the shape of the rise and fall edge of midpoint voltage, the shaded areas in Fig. 6(a), (b) and (c) can be always obtained as \(A_{vnm} = \int_{t_0}^{t_f} v_{nm}(t) dt = \frac{1}{2 L_c} A_{vnm}\). Thus, \(\Delta i_{L,m,n}\) can be expressed as \(-\Delta i_{L,m,n} = \frac{V_{dc} \Delta \tau}{2 L_c}\). That is, the resulting current difference between \(L_m\) and \(L_n\), \(\Delta I_{L,\tau_n} = |\Delta i_{L,m,n} - \Delta i_{L,m,n}| = \frac{V_{dc} \Delta \tau}{2 L_c}\), is independent of the rise (fall) time and shape of midpoint voltages. Therefore, the analyses above \((t_r = 0)\) also hold true in practical scenarios where \(t_r > 0\).

Compared with the direct parallel where \(L_1, L_2, \ldots, L_N\) represent parasitic inductances and have small values (e.g., < a few tens of nH), the proposed paralleling structure with added commutation inductors is capable of alleviating the current imbalance among the paralleled GaN HEMT HB legs.
B. Asynchronous Mode

As the load decreases, fewer effective GaN HEMTs in parallel lead to lower switching losses, as shown in Fig. 7(c). Hence, it is preferable for the proposed desynchronizable paralleling structure to operate in an asynchronous mode. In this asynchronous mode, \( n_{id} \) legs are leading the remaining \( n_{ig} \) \( (n_{ig} = N - n_{id}) \) ones at their turn-on instants, as shown in Fig. 7(a). Meanwhile, the \( n_{id} \) leading legs are synchronously gated, and so are the \( n_{ig} \) lagging legs. The theoretical midpoint voltages of these HBs are shown in Fig. 5(b). However, it should be noted that in this proposed asynchronous mode, the time delay is much longer than the inevitable small delay in the synchronous mode.

To simplify the analysis in the asynchronous mode, the \( n_{id} \) leading legs and their corresponding commutation inductors are lumped into a single leading leg \( S_{Ha} \& S_{La} \) with a single commutation inductor \( L_a \). Likewise, the \( n_{ig} \) lagging legs and their corresponding commutation inductors can be lumped into \( S_{Hb} \& S_{Lb} + L_a \). The equivalent circuit of Fig. 7(a) is shown in Fig. 7(b). It is noted that the equivalent output capacitances of \( S_{Ha} \& S_{La} \) and \( S_{Hb} \& S_{Lb} \) are \( n_{ig} C_{oss} \) and \( n_{ig} C_{oss} \), respectively; the inductances of \( L_a \) and \( L_b \) are \( L_e/n_{id} \) and \( L_e/n_{ig} \), respectively. Thus, the equivalent differential-mode inductance between the two lumped legs is

\[
L_{DM} = L_a + L_b = n_{id} + n_{ig} L_e \quad (10)
\]

The typical operating waveforms of the proposed paralleling structure in the asynchronous mode are shown in Fig. 8. Depending on the polarity of the leading indutor current at \( t_0 \) i.e., \( I_{La,t_0} = I_{La,t_0} - I_{lb,t_0} \), \( I_{La,t_0} = I_{La,t_0} - I_{lb,t_0} \), two operating cases can be identified in the asynchronous mode: Case I \( (I_{La,t_0} = I_{La,t_0} - I_{lb,t_0} \geq 0 \), see Fig. 8(a)) and Case II \( (I_{La,t_0} = I_{La,t_0} - I_{lb,t_0} < 0 \), see Fig. 8(b)).

1) Case I \( I_{La,t_0} = I_{La,t_0} - I_{lb,t_0} \geq 0 \)

Considering the parasitic output capacitance of HEMTs, we can identify ten operation stages for one switching cycle \([t_0, t_1]\), as shown in Figs. 8(a) and 9(a).

Stage 1 \([t_0, t_1]\) (see Figs. 8(a) and 9(a)): The high-side switches \( S_{Ha} \) and \( S_{Hb} \) have been reversely conducting before \( t_0 \). At \( t_0 \), \( S_{Ha} \) and \( S_{Hb} \) are turned off, and thus, their body diodes begin conducting.

Stage 2 \([t_1, t_2]\) (see Figs. 8(a) and 9(c)): After the deadtime \( t_d \), the low-side switch of the leading HB leg, i.e., \( S_{La} \), is applied with a turn-on signal. When its gate-source voltage \( V_{gs, lb} \) rises to the threshold voltage \( V_{gs, bh} \), the channel of \( S_{La} \) begins to conduct, operating as a voltage-controlled current source. The drain current \( i_{ds, SLa} \) rises (as shaded in Fig. 8(a)) corresponding to the charge stored in \( C_{oss, SLa} \), i.e., \( n_{ig} C_{oss} = \int_0^{t_3} V_{oss, SLa}(V_{ds})dV_{ds} = n_{ig} V_{ds}^2 C_{oss}(v_{ds})dV_{ds} \). In this stage, the output capacitor of \( S_{La} \), i.e., \( C_{oss, SLa} \), is self discharging via its 2DEG, leading to a decreasing \( V_{ds, SLa} \) and an energy loss \( n_{ig} E_{oss} \), as indicated by the light blue dashed line in Fig. 9(d). It should be noted that the energy loss \( n_{ig} E_{oss} \) is stored during last turn-off event and is included in the measured turn-off energy loss.

Stage 4 \([t_3, t_4]\) (see Figs. 8(a) and 9(e)): At \( t_3 \), \( C_{oss, SHa} \) and \( C_{oss, SLa} \) are fully charged to \( V_{dc} \) and discharged to 0, respectively, which means that \( S_{La} \) is fully turned on and \( S_{Ha} \) is fully turned off. Then, the negative midpoint voltage \( v_{ab} = -V_{dc} \) drives the circulating current \( i_{lb} \) to decrease. That is, during the interval of \([t_3, t_4]\), the energy stored in the commutation inductor \( L_b \) is delivered to the dc source \( V_{dc} \). The decrease of \( i_{lb} \) follows

\[
i_{lb}(t) = i_{lb}(t_3) - \frac{V_{dc}}{L_{DM}}(t - t_3)
\]

\[
i_{lb}(t) = i_{lb}(t_3) - \frac{n_{id} n_{ig} V_{dc}}{n_{ig} V_{dc} + n_{id} V_{ds}}(t - t_3)
\]

\[
i_{lb}(t) = i_{lb}(t_3) - \frac{n_{id} n_{ig} V_{dc}}{n_{ig} V_{dc} + n_{id} V_{ds}}(t - t_3)
\]

where \( I_{lb, pk} \) represents the peak value of the circulating current \( i_{lb} \). From (11), we can obtain the time between \( t_3 \) and \( t_4 \) as

\[
\Delta t_{LB} = t_4 - t_3 \approx \frac{I_{lb, pk}(n_{id} + n_{ig}) L_e}{n_{id} V_{dc}}
\]

It is also noted that during the interval \([t_1, t_4]\), the circulating current \( i_{lb} \) remains freewheeling through \( S_{Hb} \), and thus, the states of the lagging-leg switches \( S_{Hb} - \overline{S_{Lb}} \) keep unchanged.

Stage 5 \([t_4, t_5]\) (see Figs. 8(a) and 9(f)): The circulating current \( i_{lb} \) falls to 0 at \( t_4 \), after which the output capacitors

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This page contains technical content related to power electronics, specifically focusing on desynchronizable paralleling structures in GaN HEMTs for asynchronous operation. The content covers the analysis of different operation stages, including the charging and discharging of output capacitors, the calculation of energy loss, and the behavior of circulating current. It also includes diagrams and equations to illustrate these processes. The text is rich with mathematical expressions and diagrams that are essential for understanding the asynchronous mode of operation. The document is part of a larger study on power electronics, focusing on the optimization of power conversion efficiency through the use of GaN HEMTs in high-frequency switching applications.
\[ L_{DM} \left[ \left( i_{LB}(t_5) \right) \right]^2 = \frac{(n_{id} + n_{ig}) L_c}{n_{id} n_{ig}} \frac{i_{cir.pk}^2}{2} = n_{ig} V_{dc} Q_{oss} \] (13)

where the peak value of the circulating current \( i_{LB} \), i.e., \( I_{cir.pk} \), can be obtained as

\[ I_{cir.pk} = -i_{LB}(t_5) = \sqrt{\frac{2 n_{id} n_{ig}^2 V_{dc} Q_{oss}}{(n_{id} + n_{ig}) L_c}} \] (14)

The output capacitance of a GaN HEMT is strongly dependent on its drain-source voltage. Due to this dependency, the shape of \( i_{LB} \) is almost trapezoidal during \([t_4, t_5]\). In [33], [53], the highly nonlinear output capacitance \( C_{oss} \) is further idealized, i.e., \( C_{oss} \) is assumed as extremely large at low voltages and extremely small at high voltages; thus, a \( Q_{oss}\)-based time model is proposed for power MOSFETs and HEMTs [43], [53]. According to this model, the total accumulated charge of \( i_{LB} \) over \([t_4, t_5]\) is \( 2 n_{ig} Q_{oss} \), and the trapezoidal current \( i_{LB} \) reaches it vertex when the accumulated charge equals \( n_{ig} Q_{oss} \). Thus, we can obtain the time between \( t_4 \) and \( t_5 \), i.e.,

\[ \Delta t_{45} = t_5 - t_4 = \frac{2 n_{ig} Q_{oss}}{I_{cir.pk}} + \frac{n_{ig} Q_{oss}}{I_{cir.pk}} = \frac{3 n_{ig} Q_{oss}}{I_{cir.pk}} \] (15)

**Stage 6** \([t_5, t_6]\) (see Figs. 8(a) and 8(f)): After \( t_5 \), the body diode of \( S_{LB} \) begins conducting the circulating current \( i_{LB} \).

Subsequently, applying a turn-on gate signal to \( S_{LB} \) enable it to achieve the ZVS-on, thereby minimizing its switching loss. During the interval \([t_5, t_6]\), both the load current \( I_{Lo} \) and the small circulating current \( i_{LB} \) are flowing through \( S_{La} \).

**Stage 7** \([t_6, t_7]\) (see Figs. 8(a) and 9(h)): At \( t_6 \), the turn-off gate signals of the low-side switches \( S_{La} \& S_{LB} \) are applied. \( S_{La} \) is then switched off at \( t_7 \). During this interval, \( C_{oss,SLa} \) is charged to \( V_{dc} \) and thus stores energy of \( E_{oss} \). However, it should be noted that this energy of \( E_{oss} \) is not dissipated until next turn-on interval \([t_2, t_3]\) (see the light blue dashed line in Fig. 9(d)). During the whole interval \([t_6, t_7]\), the body diode of \( S_{LB} \) conducts the negative circulating current \( i_{LB} \) and therefore, \( S_{LB} \) has not truly turned off.

**Stage 8** \([t_7, t_8]\) (see Figs. 8(a) and 9(i)): The output capacitors \( C_{oss,SLa} \) and \( C_{oss,SLb} \) are respectively fully charged and discharged at \( t_7 \), after which the body diode of \( S_{La} \) begins to conduct. Therefore, \( S_{La} \) is able to achieve the ZVS-on if the turn-on signal is applied subsequently. Meanwhile, the differential voltage \( V_{gb} \) is equal to \( V_{dc} \), causing the circulating current \( i_{LB} \) to linearly increase as

\[ i_{LB}(t) = i_{LB}(t_7) + \frac{V_{dc}}{n_{id}} \frac{t - t_7}{t_8 - t_7} \]

From (16), we can obtain the time between \( t_7 \) and \( t_8 \) as

\[ \Delta t_{78} = t_8 - t_7 = \frac{i_{LB}(t_7) (n_{id} + n_{ig}) L_c}{V_{dc}} \frac{t_8 - t_7}{n_{id} n_{ig}} \]

(17)

**Stage 9** \([t_8, t_9]\) (see Figs. 8(a) and 9(j)): At \( t_8 \), the circulating current \( i_{LB} \) reaches 0, and thus, the output capacitors \( C_{oss,HLb} \) and \( C_{oss,HLb} \) begin transfer charge through the commutation inductors \( L_a \) and \( L_b \) under the excitation of \( V_{dc} \) setting at \( t_9 \) with \( C_{oss,SLb} \) charged to \( V_{dc} \) and \( C_{oss,SLa} \) discharged to 0. Assuming there is no resistive energy loss during \([t_4, t_5]\), then according to the law of conservation of energy, we have

\[ C_{oss,SLb} \, C_{oss,SLb} \] begin to transfer charge through the commutation inductors \( L_a \& L_b \) under the excitation of \( V_{dc} \) setting at \( t_5 \) with \( C_{oss,SLb} \) charged to \( V_{dc} \) and \( C_{oss,SLa} \) discharged to 0. Assuming there is no resistive energy loss during \([t_4, t_5]\),
From (18), we have
\[ I_{\text{load}} = I_{\text{pk}} \]
with the interval \([t_4, t_5]\), neglecting the resistive energy loss during \([t_5, t_6]\) yields
\[
\frac{L_{\text{DM}}[(t_{\text{LB}}(t_9))]^2}{2} = \frac{(n_{\text{ld}} + n_{\text{ig}})L_c I_{\text{pk}}^2}{n_{\text{ld}}n_{\text{ig}}} = \frac{I_{\text{pk}}}{n_{\text{ld}}n_{\text{ig}}} V_{\text{dc}, \text{oss}}
\]
From (18), we have
\[
i_{\text{LB}}(t_9) = -i_{\text{LB}}(t_5) = I_{\text{pk}} = \sqrt{\frac{2n_{\text{ld}}n_{\text{ig}}^2 V_{\text{dc}, \text{oss}}}{(n_{\text{ld}} + n_{\text{ig}})L_c}}
\]
As with the interval \([t_4, t_5]\), the time between \(t_8\) and \(t_9\) can be derived as
\[
\Delta t_{\text{LB}} = t_9 - t_8 = \frac{2n_{\text{ld}}Q_{\text{oss}}}{I_{\text{pk}} \text{pk}} + \frac{n_{\text{ig}}Q_{\text{oss}}}{I_{\text{pk}} \text{pk}} = \frac{3n_{\text{ld}}Q_{\text{oss}}}{I_{\text{pk}} \text{pk}}
\]
From (12), (15), (17) and (20), we have \(\Delta t_{\text{FS}} = \Delta t_{34}\) and \(\Delta t_{\text{LB}} = \Delta t_{45}\).

Stage 10 \([t_9, t_{10}]\) (see Figs. 8(a) and 9(k)): After \(t_9\), the body diode of \(S_{\text{HSb}}\) conducts, and thus, \(S_{\text{HSb}}\) is able to achieve ZVS-on by being applied with a turn-on gate signal. During the interval \([t_9, t_{10}]\), the drain-source current of \(S_{\text{HSa}}\) is lower than the load current, i.e., \(-i_{\text{ds}, S_{\text{HSa}}} = I_{\text{La}} - I_{\text{LB}}\). A brief summary of the asynchronous operation in Case I can be drawn, as follows:

- The leading lower switch \(S_{\text{La}}\) is hard switched-on at a current lower than the load current, i.e., \(I_{\text{La}, t_0} = I_{\text{Lo}} - I_{\text{cir, pk}} > 0\);
- The lagging lower switch \(S_{\text{Lb}}\) is able to achieve the ZVS-on, and thus its switching loss can be eliminated compared with the synchronous operation.

2) Case II: \(I_{\text{La}, t_0} = I_{\text{Lo}} - I_{\text{cir, pk}} < 0\)
As the load current \(I_{\text{Lo}}\) further decreases, the leading inductor current at \(t_0\), \(I_{\text{La}, t_0}\), will become negative, i.e., \(I_{\text{La}, t_0} = I_{\text{Lo}} - I_{\text{cir, pk}} < 0\). This case is termed as Case II in which the operating process of the proposed paralleling structure is the same as that in Case I except for intervals \([t_9, t_{10}]\) and \([t_0, t_1]\), as shown in Figs. 8(b), 9(b) and 9(l).
As with Case I, due to the delay between the leading and lagging legs and the commutation inductors $L_a$ and $L_b$, a circulating current $i_{lb}$ with a peak value of $I_{cir.pk}$ can be also generated in Case II. Thus, the lagging switches are able to achieve the ZVS-on, leading to minimized switching losses. For the turn-on of the leading switch $S_{La}$, the operating principle in Case II is different from that in Case I, as illustrated below.

Before $t_0$, the lagging upper switch $S_{Ha}$ is reversely conducting due to the positive circulating current $i_{lb}$. For the leading inductor current $i_{La}$, however, it is negative, i.e., $i_{La} = I_{Lo} - i_{lb} < 0$, which means that a positive current $-i_{lb}$ is flowing through the leading upper switch $S_{Ha}$ during $[t_9, t_{10}]$, as shown in Fig. 9(a). At $t_0$, turn-off gate signals are applied to cut off the channels of $S_{Ha}$ and $S_{Ho}$. Thus, the body diode of $S_{Ho}$ is conducting during $[t_0, t_1]$. For the leading upper switch $S_{Ha}$, however, its channel current is diverted to the output capacitors $C_{oss,Ha}$ and $C_{oss,La}$, as shown in Fig. 9(b). That is, the two output capacitors $C_{oss,Ha}$ and $C_{oss,La}$ begin transferring charge through the commutation inductors $L_a$ and $L_b$. under the excitation of $V_{dc}$. During this interval $[t_0, t_1]$ in Case II, the inductor currents $i_{La}$ and $i_{lb}$ decrease in magnitude; the drain-source voltages of the leading leg switches $v_{ds,SLa}$ and $v_{ds,SHA}$ rises and decreases, respectively. This interval terminates at $t_1$ when $i_{La}$ reaches 0, i.e., $i_{La}(t_1) = I_{Lo} - i_{lb}(t_1) = 0$.

If $v_{ds,SHA}$ increases to $V_{dc}$ and $v_{ds,SLa}$ decreases to 0 at $t_1$, then the leading lower switch $S_{La}$ is able to achieve the ZVS-on. If $v_{ds,SLa}$ decreases but not to 0 when $i_{La}$ reaches 0, then $S_{La}$ is only able to achieve the incomplete zero-voltage switching (iZVS) ON.

Assuming $v_{ds,SLa}$ decreases to 0 at $t_1$ when $i_{La}$ reaches 0, then according to the law of conservation of energy, we have

$$V_{dc}n_i Q_{oss} = \frac{1}{2} L_{DM} (I_{Lo} - I_{cir.pk})^2$$

(21)

Substituting (14) into (21) yields the critical load current below which the leading lower switch $S_{La}$ can achieve the
ZVS-on, i.e.,

\[
I_{Lo,cri} = I_{cir, pk} - \sqrt{\frac{2V_{ds}n_{ig}Q_{oss}}{L_{DM}}} \\
= \sqrt{\frac{2n_{ig}^2V_{ds}Q_{oss}}{(n_{ig}+n_{ld})L_{c}}} - \sqrt{\frac{2n_{ld}^2V_{ds}Q_{oss}}{(n_{ld}+n_{ig})L_{c}}} \\
= (\sqrt{m_{ig}} - \sqrt{m_{ld}}) \sqrt{\frac{2n_{ig}n_{ld}V_{ds}Q_{oss}}{(n_{ig}+n_{ld})L_{c}}} \tag{22}
\]

Based on (22), we can conclude:

- In the scenario of \( n_{ig} < n_{ld} \), the critical load current \( I_{Lo,cri} \) is always positive, indicating the critical load current \( I_{Lo,cri} \) is always positive. It implies that switch \( S_{La} \) is able to achieve the ZVS-on when the load current satisfies \( 0 \leq I_{Lo} \leq I_{Lo,cri} \), and achieve the ZVS-on [54] when \( I_{Lo,cri} < I_{Lo} < I_{cir, pk} \).
- In Case II, \( n_{ig} > n_{ld} \), then \( I_{Lo,cri} < 0 \). It means that switch \( S_{La} \) is not able to achieve the ZVS-on when \( 0 \leq I_{Lo} < I_{cir, pk} \).

In Case II, the load durations \( \Delta t_{f5}, \Delta t_{f8}, \) and \( \Delta t_{s9} \) still follow (15), (17), and (20), respectively. For \( \Delta t_{s4} \), however, it has different expressions in both cases. In Case II, \( \Delta t_{s4} \) becomes load-current-dependent and it follows

\[
\Delta t_{s4} = I_{Lo} \frac{(n_{id} + n_{lg}) L_c}{V_{dc} n_{id} n_{lg}} \tag{23}
\]

In both Case I and Case II, the peak circulating current \( I_{cir, pk} \) can be expressed by (23). Fig. 11 shows the curves of the peak circulating current \( I_{cir, pk} \) with respect to the commutation inductance \( L_c \) at different numbers of parallelled devices \( N \) and different numbers of lagging devices \( n_{lg} \). As can be seen from (14) and Fig. 11, the peak circulating current \( I_{cir, pk} \) is independent of the load current \( I_{Lo} \). Instead, it is determined by the commutation inductance \( L_c \), the number of devices in parallel \( N \), and the number of lagging devices \( n_{lg} \). The more devices in parallel and the more lagging devices, the higher the peak circulating current. Moreover, it is seen that \( I_{cir, pk} \) decreases with the increase of \( L_c \); thus, the region of operating in Case II \((I_{Lo} < I_{cir, pk})\) becomes smaller.

C. Comparison Between Synchronous and Asynchronous Modes

1) Soft-switching

As analyzed in Section III, when the load current \( I_{Lo} \) is positive, all the high-side switches \( S_{Hi} \) can achieve the ZVS-on in both the synchronous and asynchronous modes. For the low-side switches, i.e., the DUTs, they can be turned on under soft or hard conditions depending on the operation modes and cases, as summarized in Table I. Specifically, in the synchronous mode, all the DUTs are hard switched; in the asynchronous mode, the leading DUT \( S_{La} \) is turned on under HS and ZVS in Case I and Case II, respectively. By contrast, the lagging DUT \( S_{Ld} \) always achieves the ZVS in the asynchronous mode. Compared with the synchronous operation, the asynchronous mode leads to a reduced number of hard-switched GaN HEMTs, and therefore, it enables to decrease the switching loss.

It is noted that when the direction of the load current is reversed, i.e., \( I_{Lo} < 0 \), the soft-switching conditions of \( S_{Ha} \& S_{Hb} \) and \( S_{Ld} \& S_{Lb} \) will be swapped.

2) dv/dt of Common-Mode Voltage \( v_O \)

As mentioned in Section II-B, the commutation inductance \( L_c \) is negligible compared with the output filter inductance \( L_o \), i.e., \( L_c \ll L_o \), the output (common-mode) voltage of the \( N \) paralleled HBs (see Figs. 2[b], 3, and 7) is the average of the \( N \) midpoint voltages, i.e.,

\[
v_O = \frac{1}{N} \sum_{n=1}^{N} v_n \tag{24}
\]

The waveforms of \( v_O \) in the synchronous and asynchronous modes are shown in Figs. 3 and 8, respectively. In the synchronous mode, the common-mode voltage \( v_O \) is identical to the drain-source voltage of the low-side switches. The high-side switches achieve the ZVS-on, leading to a slow rise time \( (t_4, t_5) \) for \( v_{ds, SLn} \). Therefore, the maximum \( dv/dt \) of \( v_O \) in the synchronous mode is determined by the hard-switching-on of the low-side switches, i.e., during \([t_2, t_3]\) in Fig. 3.

In the asynchronous mode, the common-mode voltage \( v_O \) is the average of \( v_{ds, SLa} \) and \( v_{ds, SLb} \) which, however, are not in phase with each other. As a result, the edges of \( v_O \) are expanded to three or four intervals, i.e., \([t_2, t_3]\), \([t_4, t_5]\), and \([t_6, t_7]\) in Case II, \([t_3, t_4]\) and \([t_5, t_6]\) for the rising edge, and \([t_7, t_8]\), \([t_8, t_9]\) and \([t_8, t_9]\) for the falling edge, as shown in Fig. 8. The maximum \( dv/dt \) of \( v_O \) in this mode is determined by the hard-switching interval \([t_2, t_3]\) during which the leading low-side switch \( S_{La} \) is being hard turned on, but the lagging low-side switch \( S_{Lb} \) is kept off. Thus, the \( dv/dt \) of \( v_O \) during \([t_2, t_3]\) is halved compared with the synchronous mode. During other switching intervals, i.e., \([t_0, t_1]\) (Case II), \([t_4, t_5]\), \([t_6, t_7]\) and \([t_8, t_9]\), it still holds true that only one of the two lumped HBs (see Figs. 7[b], 8) is being turn-on under ZVS. Hence, the \( dv/dt \) of \( v_O \) in these switching intervals can be significantly reduced, leading to alleviated electromagnetic interference (EMI).

3) RMS Current and Peak-to-Peak Magnetic Flux Density of Commutation Inductors

i) Root-Mean-Square (RMS) Current:

The RMS currents of commutation inductors in the synchronous and asynchronous modes are obtained and shown in Table I.

ii) Peak-to-Peak Magnetic Flux Density \( \Delta B \):

When operating in the asynchronous mode, the current ripple of commutation inductors can be approximated as \( 2I_{cir, pk} \), as shown in Fig. 8. The resulting peak-to-peak magnetic flux density of commutation inductors can be obtained as
\[ \Delta B = L_c \frac{2I_{\text{cir.pk}}}{n_t A_c} \]  
(25)

where \( n_t \) and \( A_c \) represent the number of turns and the effective cross-sectional area of a commutation inductor, respectively.

Substituting (14) to (25) yields

\[ \Delta B = 2 \sqrt{\frac{\mu_r \mu_0}{V_e}} \sqrt{\frac{2n_{tud} n^2_g V_{dc} Q_{\text{loss}}}{n_{ld} + n_{lg}}} \]  
(26)

where the constant \( \mu_0 \) is the permeability of free space, \( \mu_r \) represents the relative permeability of the used magnetic core material, and \( V_e \) denotes the effective magnetic core volume of a commutation inductor. It is seen that the flux density swing \( \Delta B \) is proportional to the square root of the relative permeability \( \mu_r \). According to Steinmetz’s equation, the magnetic core loss is positively related to \( \Delta B \). Therefore, from the perspective of core loss reduction, low-permeability core materials should be used and/or air gaps should be inserted.

When operating in the synchronous mode, the current ripple of commutation inductors is determined by the load current, i.e., \( \Delta I_{L_c} = I_{L_c}/N_c \), which is relatively small. Therefore, the magnetic flux density fluctuation \( \Delta B \) is also low, leading to low core loss. Nevertheless, the synchronous mode is activated when the load current is high, and this means that the commutator inductors need to withstand a DC current of \( I_{L_c}/N_c \). To avoid magnetic saturation in the synchronous mode, it is also desired to use low-permeability core material or insert an air gap.

It is noted that the commutation inductors can be inversely-coupled to increase the differential-mode inductance, decrease the common-mode inductance, and lower the core loss in the synchronous mode.

IV. Design Guidelines and Thermal Balancing Scheme of Proposed Parallelizing Structure

A. Design Guidelines

1) Number of GaN HEMT HB Legs in Parallel \( N \)

As aforementioned, the synchronous and asynchronous modes are selected at heavy and light loads, respectively. The number of paralleled GaN HEMTs, \( N \), should be determined based on the maximum power loss and highest junction temperature of devices at the rated full power in the synchronous mode.

2) Commutation Inductors

i) Commutation Inductance \( L_c \):

In the synchronous mode, the commutation inductors \( L_1, L_2, ..., L_N \) (see Fig. 2(b)) are able to help the parallel devices achieve better dynamic current sharing under parameter mismatches of HEMTs. The maximum inductor or HEMT current imbalance \( \Delta I_{L_c,\text{max}} \) is a function of the DC voltage \( V_{dc} \), the maximum gating time delay \( \tau \) and the commutation inductance \( L_c \). The higher the commutation inductance, the smaller the current imbalance. When operating in the asynchronous mode, a higher \( L_c \) results in a lower circulating current peak \( I_{cir.pk} \) (see (14) and Fig. 11), which is beneficial to the conduction loss reduction.

On the other hand, a higher commutation inductance results in higher inductor volume. Therefore, a trade-off among dynamic current sharing, conduction loss and inductor size should be made when selecting \( L_c \).

ii) Bandwidth Requirement:

Bandwidth 1 \( BW_{L_c,1} \): Neglecting the short turn-on times of GaN HEMTs, the maximum rise and fall times of the commutation inductor currents are equal to the time delays \( t_{dl,L} \) and \( t_{dt,H} \) which depend on multiple parameters, as shown in Fig. 12. When the commutation inductance \( L_c \geq 1 \mu H \), the rise and fall times of \( t_{la} \) and \( t_{lb} \) are above 50 ns which correspond to a bandwidth of \( BW_{L_c,1} = \frac{1}{t_{la}} = 7 \) MHz [58]. This means that in order to implement the proposed asynchronous operation, the commutation inductors need to maintain the desired inductance \( L_c \) at 7 MHz or above.

Bandwidth 2 \( BW_{L_c,2} \): As mentioned in Section III-A, the commutation inductors are used also to alleviate the current imbalance between the paralleled HBs in the synchronous mode. The current mismatch is caused by the differential-mode voltage \( v_{ab} = v_a - v_b \) whose bandwidth is not higher than that of \( v_{ab} \) (i.e., \( v_{ds,SLa} \) or \( v_{rb} \), i.e., \( v_{ds,SLb} \)). Therefore, the rise or fall times of \( v_{ds,SLa} \) and \( v_{ds,SLb} \) can be used to calculate the maximum bandwidth of the commutation inductors required to alleviate current imbalance in (9). Assume that the rise time of drain-source voltage of a 650-V GaN HEMT with a 400-V dc bus voltage is 10 ns, then the corresponding bandwidth \( BW_{L_c,2} = \frac{0.35}{10 ns} = 35 \) MHz.

If the maximum delay between the midpoint voltages is 5 ns, and the allowed maximum current imbalance is 1 A, then based on (9), the required commutation inductance at 35 MHz is

\[ L_c @ 35 \text{MHz} = \frac{400 \text{ V} \times 5 \text{ ns}}{1 \text{ A}} = 2 \mu H \]  
(27)

Therefore, the commutation inductors are required to maintain an inductance of \( L_c \) (e.g., 3.3 \( \mu H \)) at \( BW_{L_c,1} \), and also have an inductance over \( L_c @ 35 \text{MHz} = 2 \mu H \) at \( BW_{L_c,2} \).

iii) Core Material Selection:

As discussed above, the required maximum bandwidth of commutation inductors is determined by \( BW_{L_c,2} \) which can be as high as 35 MHz for paralleling the GS66508T GaN HEMTs. To have a desired inductance at 35 MHz, the relative permeability of used magnetic cores should be high (e.g., > 50 [31]) so that the inductor size can be reduced.

In the meanwhile, it is seen from Figs. 3 and 8 that the commutation inductors are excited at the switching frequency \( f_s \); then core loss is generated at \( f_s \) as well. Therefore, the selected core material should also feature low core loss at the switching frequency \( f_s \). If the switching frequency \( f_s \geq 50 \) kHz, then high-frequency Mn-Zn Ferrite materials can be selected due to their low cost and low power loss density over other materials, e.g., iron powder, nanocrystalline, and amorphous [59].

3) Time Delays \( t_{dl,L} \& t_{dt,H} \) in Asynchronous Mode

As seen in Fig. 8 in the asynchronous mode, the turn-on instants of the legging leg switches \( S_{Hb,K} \& S_{Lb} \) are delayed by \( t_{dl,L} \& t_{dt,H} \) with respect to the leading leg \( S_{H,L} \& S_{L}. \) Based on the analysis in Section III-B, we can obtain the time delays

\[ t_{dl,L} = \ldots \]  
(28)

\[ t_{dt,H} = \ldots \]  
(29)

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Switching frequency dependent

High due to large inductance

Not needed

Needed

Needed

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\[ t_{dl,L} = t_{sw,L} + \Delta t_{34} + \Delta t_{45} \]

\[ = t_{sw,L} + \begin{cases} 5 \frac{N Q_{swLc}}{2(N-n_{lg})V_{dc}}, & \text{Case I} \\ 3 \frac{N Q_{swLc}}{2(N-n_{lg})V_{dc}} + \frac{t_{swZVSH}N_{f}}{n_{lg}(N-n_{lg})V_{dc}}, & \text{Case II} \end{cases} \]

\[ t_{dl,H} = \Delta t_{78} + \Delta t_{89} = -\frac{t_{sw,h}}{2} + 5 \sqrt{\frac{N Q_{swLc}}{2(N-n_{lg})V_{dc}}} \]

where the switching times of \( S_{La} \) and \( S_{Hf} \), i.e., \( t_{sw,L} \) and \( t_{sw,H} \), depend on many factors, e.g., the gate resistance, turn-on current, number of HEMTs turned on \( n_{lg} \). Nevertheless, the turn-on time of a 650-V GS66508/16 GaN HEMT is normally less than 10-20 ns [5], [50], [51], [60] which is short compared to the other times \( \Delta t_{34}, \Delta t_{45}, \Delta t_{78}, \Delta t_{89} \). Therefore, in practice, a conservative fixed value, e.g., 20 ns, can be assigned to \( t_{sw,L} \) and \( t_{sw,H} \).

Fig. 12 shows the calculated theoretical time delays \( t_{dl,L} \) and \( t_{dl,H} \) with respect to multiple parameters, i.e., the load current \( I_{Lo} \), the commutation inductance \( L_{c} \), the number of devices in parallel \( N \), and the number of lagging devices \( n_{lg} \). As one can see, both time delays \( t_{dl,L} \) and \( t_{dl,H} \) are affected by the three parameters \( L_{c}, N \), and \( n_{lg} \). For the load current \( I_{Lo} \), however, it has different impacts on the time delays \( t_{dl,L} \) and \( t_{dl,H} \) in Case I and Case II of the asynchronous mode. Specifically, in Case I, the load current \( I_{Lo} \) has no impact on both time delays \( t_{dl,L} \) and \( t_{dl,H} \). In Case II, \( I_{Lo} \) still does not affect \( t_{dl,H} \), but influences \( t_{dl,L} \); the time delay \( t_{dl,L} \) linearly falls with the decrease of \( I_{Lo} \).

The proposed desynchronizable control scheme can be applied to any converter topologies consisting of multiple paralleled HBs. The implementation diagram is shown in Fig. 13(a). In addition to the main control and modulation blocks of a specific converter, this desynchronizable paralleling scheme also requires blocks to select the operation mode and to determine the time delays based on the dc-bus voltage \( V_{dc} \) and the load current \( I_{Lo} \). Specifically, the efficiency performance of the converter should be evaluated or tested in the synchronous and asynchronous modes, leading to a lookup table (LUT) for selecting an efficiency optimal mode. Then, (28) and (29) can be used to calculate or look up the time delays for the lagging low-side and high-side switches, respectively. Furthermore, the leading and lagging legs do not share the same thermal stress because they have different power losses. The lagging lower...
HEMT achieves the ZVS-on and conducts the small circulating current, whereas the leading counterpart is hard-switched and meanwhile, has a higher RMS current. Therefore, the leading device suffers from a severer thermal stress. In order to achieve a balanced thermal stress between the leading and lagging DUTs, an alternating delay scheme is proposed for the paralleled structure operating in the asynchronous mode, as shown in Fig. [13](a) and (b). One of the two legs $S_{1a}$&$S_{1b}$ and $S_{2a}$&$S_{2b}$ lags the other alternately. Thus, both legs generate the same power loss and are able to share the same junction temperature under the premise of having the identical thermal resistance.

C. Comparison With CCM/TCM Multiphase Interleaving

A comparison between the proposed desynchronizable paralleling scheme and the continuous-conduction-mode (CCM)/TCM multiphase interleaving techniques is shown in Table II. In the multiphase interleaving techniques, the phase shift is equal to $\frac{2\pi}{N_f}$ which is switching frequency dependent, and is much larger than the small delay (e.g., 98 ns in Fig. [12]) required by the proposed paralleling scheme. Therefore, both the CCM and TCM multiphase interleaving techniques need high inductance in order to limit the circulating current among phases. The large inductance significantly increases the difficulty for the inductors to be integrated with power switches in modules. By contrast, the small inductance in the proposed scheme has a low impact on the output filter, which implies that this scheme is of higher generality, and the commutation inductors can be potentially integrated in a power module.

Steady-state current imbalance among the multiphase inductors is inevitable due to small mismatches in the timing of switching signals, differing switching characteristics of semiconductor devices, and unequal inductor impedances [35], [47], [61]. Therefore, current balancing schemes are required in the CCM and TCM multiphase interleaved converters [35], [45], [62]. Although all the switches can achieve the ZVS in TCM converters, they have to suffer from high RMS currents, high conduction loss and high magnetic loss at high currents. Therefore, this technique is seldom used in applications over 50 kW. Another issue with the TCM multiphase interleaving is its high implementation complexity owing to the requirements of high-speed zero current detection (ZCD) circuit and accurate timing for ZVS [30], [46], [47]. By comparison, it is relatively easier for the CCM multiphase interleaving and the proposed desynchronizable paralleling scheme to be implemented.

When operating at light loads, phase-shedding can be applied to CCM multiphase interleaved converters [21]; some phases are shut down, and thus, only part of the switches are hard-switched at the load current, leading to reduced switching loss. By contrast, the proposed asynchronous control scheme enables the remaining switches to turn on at a current lower than the load or even to achieve the iZVS; therefore, the switching loss can be further reduced with the proposed asynchronous control, as shown in Fig. [17].

V. EXPERIMENTAL VALIDATION

To verify the advantages of the proposed desynchronized paralleling scheme on the light-load switching loss reduction, multi-pulse tests and continuous Boost dc-dc operation of two parallel-connected GS66508T GaN HEMT HB legs (i.e., $N = 2$) are conducted.

A. Multi-Pulse Tests

A multi-pulse tester of two parallel-connected half bridges with GaN Systems™ GS66508T HEMTs. The test bench employs a high bandwidth oscilloscope (MSO64/Tektronix, 1 GHz) to process and display the measured data. High bandwidth current shunts (SDN-414-10/T&M Research, 2 GHz) are used to measure the drain-source currents by means of coaxial cables whereas the drain-source voltages are measured with high-voltage passive probes (PHV 1000/PMK, 400 MHz).
(DSP) control board. For high accuracy, a 1-GHz oscilloscope and 400-MHz deskewed voltage probes were used in tests along with 0.1-Ω coaxial current shunts, as shown in Table III.

The experimental waveforms of the two paralleled GaN HEMT HB legs with commutation inductors (see Fig. 7(b)) in the synchronous mode are shown in Fig. 15(a). Theoretically, the paralleled devices behave simultaneously. In practice, however, a 3.5-ns delay occurs at the turn-on instants of the HEMTs due to the aforementioned mismatches. With the help of the added commutation inductors, the turn-on current peaks and turn-on energy losses of the HEMTs are close with each other. From Fig. 15(a), it is seen that the peak current and turn-on energy loss differences are 0.7 A and 61.63 µJ = 52.11 µJ = 9.52 µJ, respectively. These differences represent small percentages of the load current and the total turn-on energy loss, i.e., 0.7 A = 2% and 61.63 µJ = 9.52 µJ = 8.36%, respectively. By contrast, in the case of direct parallel of GaN HEMTs (i.e., without the commutation inductors added), significant current imbalance (9.5 A/34 A = 19.1%) and turn-on energy loss difference (85.31–37.21)/85.31 = 39.3%) will occur, as shown in Fig. 15(b).

The experimental waveforms of the paralleled GaN HEMTs in the asynchronous mode at $V_{dc} = 400$ V are shown in Fig. 16. It is seen that $S_{La}$ is controlled to lag $S_{Lb}$ at their turn-on instants. As a result, a circulating current $i_{Lb}$ of 2.8-A peak value is generated in $L_{c}$. Given the number of paralleled GaN HEMTs $N$, the dc-link voltage $V_{dc}$, the commutation inductance $L_{c}$, and the $C_{oss}$ characteristics of GS66508T [5], we can obtain the theoretical peak circulating current based on (14), i.e.,

$$I_{cir,pk} = \frac{2n_{in}n_{out}V_{dc}Q_{oss}}{(n_{in}+n_{out})L_{c}} = \frac{2\times1.1\times400\times57\times10^{-5}}{(1+1)\times3.4\times10^{-6}} = 2.63 \text{ A}$$

The error between the measured and the calculated peak circulating current values, i.e., 2.8 A $- 2.63$ A = 0.17 A, is mainly caused by the parasitic capacitance of PCB and load inductor.

With the help of the circulating current $i_{Lb}$, the lagging switch $S_{Lb}$ is able to achieve the ZVS-on and ZVS-off, leading to minimized switching losses. For the leading switch $S_{La}$, in Case I (see Fig. 16(a)), it still turns on under the hard switching, but the switching current is equal to $i_{La} = I_{Lo} - i_{Lb}$ which is lower than the load current $I_{Lo}$. Hence, the total turn-on energy loss of $S_{La}$ & $S_{Lb}$ in the asynchronous mode is smaller than a single HEMT at the same load current $I_{Lo}$ (see Fig. 17).

When the load current $I_{Lo}$ is lower than the peak circulating current $I_{cir, pk}$, the operation of the desynchronized paralleled GaN HEMT legs enters Case II, as shown in Fig. 16(b). In addition to that the lagging switch $S_{Lb}$ achieves the ZVS-on and ZVS-off, the leading switch $S_{La}$ is able to achieve the incomplete ZVS [54], resulting in decreased switching losses. It is obtained from (22) that the critical load current $I_{Lo, cri} = 0$, which implies that the leading switch can achieve the complete ZVS when the load current $I_{Lo}$ decreases to 0.
Fig. 16(c) shows the experimental results at $I_{LO} = 0\, A$. As one can see, the drain-source voltage of the leading switch, i.e., $v_{ds,SLa}$, has decreased from 400 V to 20 V (5% of 400 V) when its gate-source voltage $v_{gs,SLa}$ rises, leading to negligible turn-on current bump and energy loss (see Fig. 17). The measured time delays $t_{dl,L}$ and $t_{dl,H}$ in the three operating scenarios in Fig. 16 are $t_{dl,L} = 131\, ns$ @ $I_{LO} = 13.5\, A$, $t_{dl,L} = 98\, ns$ @ $I_{LO} = 0.85\, A$, $t_{dl,L} = 82\, ns$ @ $I_{LO} = 0\, A$, $t_{dl,H} = 93\, ns$ @ $I_{LO} = 13.5\, A$, $t_{dl,H} = 91\, ns$ @ $I_{LO} = 0.85\, A$, and $t_{dl,H} = 94\, ns$ @ $I_{LO} = 0\, A$. The corresponding theoretical time delays in Fig. 12 are 128 ns, 99 ns, 85 ns, 98 ns, 98 ns, and 98 ns, respectively. The corresponding errors between the measured and calculated time delays are -3 ns (2.3%), 1 ns (1%), 3 ns (3.5%), 5 ns (5.1%), 7 ns (7.1%), 4 ns (4.1%), which are small. Therefore, the developed time delay models (28) and (29) are accurate.

The measured turn-on and turn-off energy losses of a single GaN HEMT and two paralleled HEMTs in the synchronous and asynchronous modes are shown Fig. 17(a). At high load currents, the synchronous operation of two parallel GaN HEMTs enables lower turn-on energy losses due to the reduced current stress on each HEMT. However, as the current decreases, the total turn-on energy loss in the asynchronous mode becomes smaller than that in the synchronous mode. When the load current is smaller than the peak circulating current 2.8 A, the asynchronous operation enables a more significant switching loss reduction than the synchronous operation because $S_{Lb}$ and $S_{La}$ achieve the ZVS and the incomplete ZVS, respectively.

Fig. 17(b) shows the total switching energy losses $E_{sw}$. It can be seen that the switching loss reduction brought by
the asynchronous operation becomes more pronounced as the load current \( I_L \) decreases. The experimental results agree well with the theoretical analysis in Section III.

**B. Continuous Boost DC-DC Operation**

The multi-pulse tester (see Figs. 7(b) and 14) can be reconfigured as a Boost converter, as shown in Fig. 18. The input Boost inductance \( L_{in} = 235 \, \mu \text{H} \) whereas the commutation inductance \( L_c = 3.3 \, \mu \text{H} = 1.45 \times 235 \, \mu \text{H} \) is much smaller. Fig. 19 shows the experimental waveforms of the Boost converter when applying the proposed thermal balancing scheme (see Fig. 13(b)) to the parallel-connected GaN HEMT HB legs. As can be seen, the two legs \( S_{Hb,1} \& S_{La,1} \) and \( S_{Hb,2} \& S_{La,2} \) are lagging with each other in an alternating manner. Seamless transitions can be achieved, and the transitions do not affect the output voltage \( V_o \).

As analyzed in Sections III-B and IV-B, the asynchronous operation leads to unbalanced power loss and thermal stress to the leading and lagging devices. Without applying the proposed thermal balancing scheme, the two parallel-connected GaN HEMT HB legs suffer different case temperatures in the asynchronous mode, i.e., 72.9 °C for the leading HEMT and 35.8 °C for the lagging HEMT, as shown in Fig. 20(a) and (b). By contrast, the case temperatures of the GaN HEMTs with the proposed alternating-delay scheme can be balanced to 58.4 °C and 58.8 °C, as shown in Fig. 20(c) and (d).

The measured efficiencies of the Boost dc-dc converter in...
Its efficiency is superior than that of two synchronous HBs when the load is lower than 750 W because the switching loss can be reduced. However, it is still lower than the proposed asynchronous mode where the lagging devices achieve the ZVS and the leading ones turn on at a lower current or achieve the iZVS, as compared in Section IV-C.

To further illustrate the advantages of the proposed asynchronous mode in light-load efficiency over the synchronous mode, the distributions of power losses in both modes are calculated and shown in Fig. 22. For the Boost converter operating in the synchronous mode, the switching losses account for the largest share of the total power loss from light to heavy loads. By contrast, with the proposed asynchronous mode, the switching losses can be significantly reduced, particularly at light loads. Compared with the synchronous mode, the asynchronous operation increases the conduction loss of switches and the loss of commutation inductors. However, the loss increase is not as remarkable as the switching loss reduction when the load is not heavy. Therefore, the total power loss can be lowered, particularly at light loads.

VI. CONCLUSIONS

A commutation-inductor-based desynchronizable parallelizing scheme is proposed for GaN HEMTs. The operating principle and design guidelines are detailed, and an alternating-delay thermal balancing scheme is proposed for the asynchronous operation. Multi-pulse and continuous Boost power conversion tests have been conducted to verify the feasibility and advantages of the proposal. The following conclusions can be drawn:

- Two operating modes, i.e., the synchronous and asynchronous modes, are enabled for the proposed parallelizing structure;
- In the synchronous mode, the proposed parallelization structure is able to achieve better current sharing performance than the conventional solution without commutation inductors;
- In the asynchronous mode, the lagging ones of the paralleled GaN HEMT HB legs are capable of achieving the ZVS and the leading ones turn on at a current lower than the load current, thereby remarkably reducing the switching loss.
- The switching loss reduction and efficiency improvement brought by the asynchronous operation become more pronounced as the load current decreases;
- The proposed alternating delay scheme enables to balance the thermal stress between the paralleled GaN HEMTs operating in the asynchronous mode.

APPENDIX

In the synchronous mode, the load current $I_{Lo}$ is shared by the $N$ commutation inductors. Neglecting the ripple of $I_{Lo}$, the equivalent RMS current of the commutation inductors is

$$I_{LC,rms,eq} = \frac{I_{Lo}}{\sqrt{N}} \quad (31)$$

In the asynchronous mode, the RMS currents of $i_{La}$ and $i_{Lb}$ can be expressed as

$$
\begin{align*}
I_{La,rms} &= \sqrt{(I_{Lo} - I_{cir, pk})^2 + 4DI_{Lo}I_{cir, pk} - \frac{sf_la I_{cir, pk}k_{La}}{\Delta L_c}} \\
I_{Lb,rms} &= I_{cir, pk}\sqrt{1 - \frac{sNf_la I_{cir, pk}k_{La}}{\Delta L_c}}
\end{align*}
$$

(32)
where $D$ represents the duty cycle of the low-side switches, and $f_s$ is the switching frequency. The equivalent RMS value of each commutation inductor can be derived as

$$I_{c,\text{rms},eq} = \sqrt{\frac{I_{L_a,\text{rms}}^2}{n_{td}} + \frac{I_{L_b,\text{rms}}^2}{n_{tg}}} \tag{33}$$

### References


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