A High-Frequency Pulsating DC Link for Electric Vehicle Drives with Reduced Losses

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Abstract—**This paper proposes a motor drive suitable for electric vehicles (EVs) with notably reduced losses as compared to conventional drives. The proposed drive feeds the dc-link with a dynamically reconfigurable battery formed by cascaded half-bridges containing battery units. The reconfigurable battery concurrently forms a modular multilevel dc-link able to synthesize variable dc-link voltages, which can adjust the dc link voltage to run a motor to operate at the optimum load point or even to contribute to modulation and greatly reduce the switching loss of the main inverter—in this case a standard two-level three-phase inverter. Up to $^2/_3$ switching actions are avoided in the main inverter, which can run at maximum duty cycle and fundamental-frequency commutation. The saved switching effort in the main inverter is shifted to the modular multilevel dc-link, but with much less loss due to the fractionized switching voltage and the use of field-effect transistors (FETs).**

At high drive speeds, the converter halves the total loss compared to a standard inverter only; at lower speeds and thus smaller modulation indices, the advantage is even more pronounced because of the dynamically lowered dc-link voltage. Other benefits include alleviated insulation stress for motor windings and direct battery balancing. The proposed motor drive is verified on a down-scaled setup with eight modules constituting the dc-link.

Keywords—*Electric vehicle, reconfigurable battery, smart dc battery, pulsating dc-link, shared modulation, converter losses.*

I. INTRODUCTION

Concerns about the environmental impact and future shortage of fossil fuels is driving the growths of electric vehicle (EV) fleets. Their drive trains almost exclusively use hard-wired battery packs and two-level three-phase inverters due to their simplicity, compactness, and ruggedness [1]–[5].

Fixed dc-link motor drives suffer several problems. First, the dc-link is at the maximum voltage at all times regardless of the actual demand, imposing maximum switching loss and insulation stress on the motor windings [2], [6], [7]. Second, the constant presence of high-voltage complicates assembly as occupational safety standards have to be implemented and involved personnel has to be high-voltage trained; furthermore, the permanent high voltage regularly confuses first responders at car crash sites with possibly delayed rescue [8]–[12]. The safety concerns are further aggravated by the recent trend toward higher battery voltages [5]. Third, the hard-wired battery concept suffers large variation of the output voltage due to load and state of charge (SoC). This spread can reach almost 50% of the rated voltage. In consequence, all loads have to operate at the entire voltage range. The consequence is a large compromise with respect to size, cost, and efficiency [13], [14]. Furthermore, hard-wired batteries suffer from their weakest link, but cell properties spread [15], [16]. Whereas charge differences due to varying capacitance and self-discharge can be managed by passive and active cell balancing, different power capabilities and heating due to varying internal resistances as well as different ageing cannot [17]. When the first cell is at its limits, the load or charging power has to be curtailed; when the first cell dies, the entire battery is dead. This issue aggravates with growing battery voltage and cells in a battery.

Some of the above problems can be solved by adjusting the dc-link voltage, e.g., regulating the dc-link voltage with respect to the speed. A dc/dc converter can, for instance, mitigate the large variation of battery voltage with SoC and the extreme mismatch between available and ideal voltage with respect to efficiency. Some vehicles, branded commercially as hybrid synergy drive by Toyota, implement a dc/dc converter between the hard-wired battery and the inverter to compensate the effect.

In such vehicles, the voltage of the dc link is controlled typically via boost, rarer a buck or buck-boost dc/dc stage between the battery pack and the three-phase inverter [6], [7], [14], [18]. At low speeds, the lowered dc-link voltage alleviates the switching loss in the inverter and notably improves the total efficiency. At higher operating speeds, however, the dc/dc stage is less beneficial to the frontend inverter but produces notice-
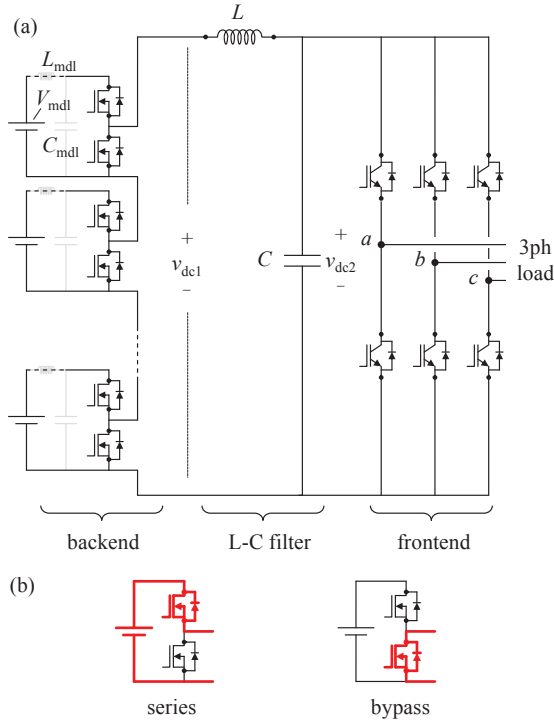
Fig. 2. (a) Proposed three-phase pulsating dc-link motor drive. A small L-C filter is implemented between dc-links v_{dc1} and v_{dc2}. Each module can incorporate an optional battery filter (L_{mdl} and C_{mdl}). (b) Switching states of the backend converter, where the battery filters are ignored.

Fig. 1. Equivalent space-vector diagram. Black arrows indicate progression in time.

able extra losses itself [2]. The dc/dc stage also requires large passive components, which impede efforts to reduce weight [19]–[21]. More importantly, the other problems of hard-wired battery packs, including safety and the limiting impact of the weakest cell, cannot be solved by the dc/dc stage.

This paper presents a modular multilevel implementation of the dc-link for EV motor drives. The batteries are individually interfaced by cascaded half-bridges (CHB), whereas the outputs are produced by a two-level three-phase inverter. The multilevel dc-link allows *1)* active battery management and flexible power distribution without external circuits, *2)* variational dc-link which inherits all advantages of the abovementioned two-stage motor drives, and most importantly *3)* arbitrary pulsating waveform at the dc-link without large passive components [22]. In particular, we produce a six-pulse rectified waveform at the dc-link to dynamically shape the modulation region and, consequently, to keep two phases in a fixed switching position. In equivalent terms, no zero-voltage vectors are required. The frontend inverter therefore spares $^2/_3$ switching actions compared to the conventional space-vector pulse-width modulation (SVPWM), or $^1/_2$ compared to the discontinuous pulse-width modulation (DPWM) [21], [23], [24]. The spared switching duty is relegated to the multilevel backend, but the latter incurs much less switching loss due to the fractionized switching voltage and the use of fast-switching field-effect transistors (FETs). The saved loss mostly owes to the now aggressively reduced switching loss of the insulated gate bipolar transistors (IGBTs) in the frontend inverter, which cannot easily benefit from more silicon in parallel; the reduced switch-
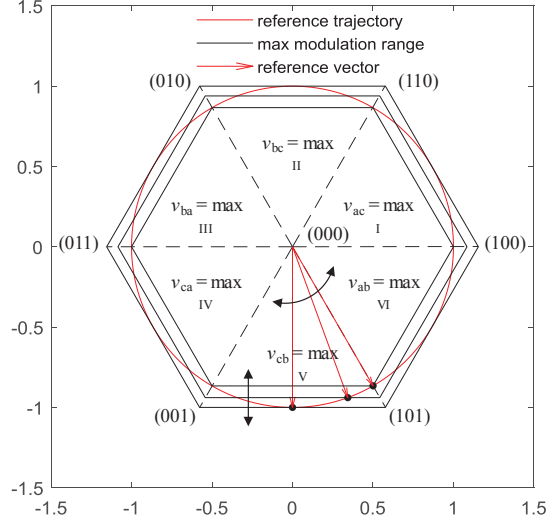
ing loss can be traded for better conduction loss in the IGBT selection. Furthermore, the output quality of the proposed converter remains good across all modulation ranges whereas SV-PWM and DPWM with fixed dc-link voltage inevitably suffer higher distortion at lower modulation indices.

The proposed topology is verified on a 2.7 kW setup with eight modules at the backend and a two-level three-phase IGBT module at the frontend.

II. TOPOLOGY AND OPERATING PRINCIPLE

A. Topology

Fig. 2 shows the proposed three-phase motor drive. It contains a modular multilevel converter as the backend, a three-phase two-level inverter as the frontend, and a small L-C filter in between. The adaptive dc battery in the backend generates the intermediate product v_{dc1}, which is further filtered by the L-C filter to produce v_{dc2} to form the rectified common-mode of the motor phases. Voltage v_{dc2} is shared with the frontend drive inverter. The L-C filter is tuned to decouple the switching transients between the frontend and the backend, and therefore can be small.

B. Operating Principle

Let us first ignore the backend and assume that v_{dc2} can be freely controlled. From the inverter's point of view, the optimal waveform for v_{dc2} is

$$v_{dc2} = \max\{v_a, v_b, v_c\} - \min\{v_a, v_b, v_c\}$$
$$= \max\{v_{ab}, v_{bc}, v_{ca}, -v_{ab}, -v_{bc}, -v_{ca}\} \quad (1)$$

where v_a, v_b, v_c are reference phase voltages. Equation (1) is optimal in the sense that there are always two inverter phases remain unswitched, regardless of the references. The low switching effort is a consequence of v_{dc2} tracking the maximum output voltage envelope per (1).

The reduction in the switching is clear when viewed in the space-vector diagram in Fig. 1. The circular reference trajecto-

ry is inferred from upper-level controls. The hexagons reflect the momentary modulation range (defined by v_{dc2}) and therefore have a variable size. Equation (1) sets v_{dc2} in such a way that the hexagon always coincides with the momentary reference vector (Fig. 1) and effectively eliminating the over-modulation region. Without the over-modulation region, the reference can be conveniently synthesized by the two adjacent active vectors without zero vectors, and only one phase leg switches at high frequency. Compared to the conventional SVPWM scheme, the elimination of the zero vector spares $^2/_3$ of switching. Precise evaluation of the overall loss depends on the load angle, output current, as well as the loss of the backend adaptive dc battery, which are detailed in Section IV. In short, the overall loss turns out lower because regulating v_{dc2} takes much less effort using the backend FETs than inserting zero-vectors with the frontend IGBTs. Furthermore, for power factors larger than 0.5, the frontend inverter never switches at current apexes. The reference signal per phase is

$$m_x = \frac{v_x - \min\{v_a, v_b, v_c\}}{\max\{v_a, v_b, v_c\} - \min\{v_a, v_b, v_c\}}, x = a, b, c. \quad (2)$$

III. MODULAR MULTILEVEL BACKEND CONVERTER

A. Modular Multilevel Backend Converter

In contrast to previous approaches with monolithic dc/dc stages and other separate units [7], [21], [23]–[26], we use a dynamically reconfigurable modular multilevel dc battery as the backend (Fig. 2). The dc battery is implemented with a cascaded structure where each module is rated at a fraction of the total voltage and incorporates a battery unit. As such, low-voltage high-current FETs can be used [27]. The adaptive dc battery's physical modularity is perfectly suited for this pulsating-dc-link EV drive, particularly because of *1)* flexible control over individual batteries to operate each battery at its ideal point with active energy as well as power balancing and thus extended mileage [28]–[30] and *2)* excellent output quality while causing negligible switching loss [31]–[35]. Importantly, we will show that the high-fidelity output allows a much smaller L-C filter and thus a rapid response.

Fig. 2(b) lists the switching states. The adaptive dc battery voltage v_{dc1} is determined by the number of series states

$$v_{dc1} = n_{series} V_{mdl}, \quad (3)$$

where V_{mdl} is the voltage of the battery subunits, n_{series} is the number of modules in series state.

B. Modulation

We use a phase-shifted carrier (PSC) scheme to modulate the adaptive dc battery. Specifically, the PSC scheme assigns a carrier C_k ($0 \le C_k \le 1$) to the k-th battery module. The switching state is determined by

$$\text{state}(k) = \begin{cases} \text{series}, & \text{if } m_{dc} \ge C_k, \\ \text{bypass}, & \text{if } m_{dc} < C_k, \end{cases}$$

$$m_{dc} = \frac{\max\{v_a, v_b, v_c\} - \min\{v_a, v_b, v_c\}}{N_{mdl} V_{mdl}}, \quad (4)$$

where N_{mdl} denotes the number of battery modules.

C. Balancing

For reconfigurable batteries based on CHB in general, battery balancing can be achieved without additional hardware or losses by superimposing small dc values $\Delta m_{x,k}$ to the modulation indices. As long as $\Sigma \Delta m_{x,k} = 0$, there is no influence on the external load. The differential load for the kth module of phase x is

$$\Delta p_{x,k} = \Delta m_{x,k} V_{mdl} i_x \quad (5)$$

where i_x is the current of phase x.

IV. ANALYSIS

This section compares the proposed motor drive with some alternatives. To show the advantage of the variational dc-link voltage, we compare the proposed solution with a conventional single-stage two-level three-phase inverter emphasizing on converter losses and total harmonic distortions (THDs). To demonstrate the benefit of the modular multilevel backend concept, in turn, we compare the CHB backend with a buck-type dc/dc converter from the state of the art with focus on switch utilization ratio (SUR) and quality of the dc-link waveform.

A. Switch Utilization Ratio

The CHB-based variable dc battery backend essentially operates as a multilevel step-down dc/dc converter. We compare its SUR with that of a buck converter according to

$$\text{SUR} = P_{load}/S, \quad S = \Sigma V_j I_j, \quad (6)$$

where S is the *total active switch stress*, defined as the sum of the products of the peak voltage V_j and rms current I_j seen by each switch. The SURs are shown Fig. 4 with various voltage conversion ratios. The SUR of the variable dc battery is advantageous in the high modulation region, which corresponds to approximately the range from 40 $^{km}/_h$ or 25 mph up in many vehicles with single-speed gearbox.

B. Voltage Ripple

We assume $N_{mdl} V_{mdl}$ at the input of the buck converter, matching the maximum voltage of the adaptive dc battery. With the same L-C filter, the two topologies produce the following voltage ripple at v_{dc2}:

$$\Delta v_{dc2}(\text{CHB}) = \frac{V_{mdl}(\lceil m_{dc} N_{mdl}\rceil - m_{dc} N_{mdl})(m_{dc} N_{mdl} - \lfloor m_{dc} N_{mdl}\rfloor)}{16 L C f_s^2 N_{mdl}^2},$$

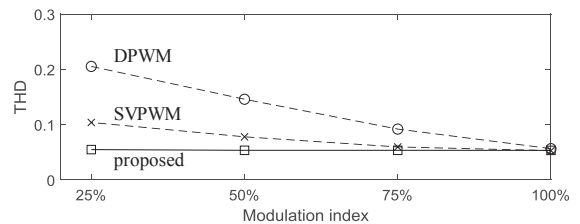$$\Delta v_{dc2}(\text{buck}) = \frac{N_{mdl} V_{mdl}(1 - m_{dc}) m_{dc}}{16 L C f_s^2}.$$

Fig. 3. THDs under series R-L passive load (1.75 Ω/200 μH). The modulation index refers to the utilization of the maximum dc-link voltage. See TABLE I for other settings. The carrier frequencies are identical across three cases.
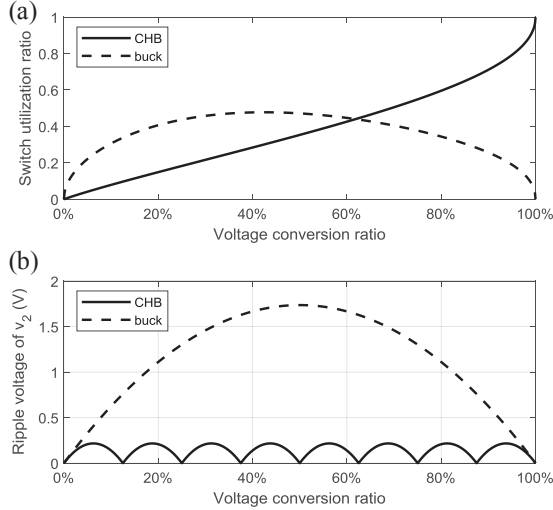
Fig. 4. (a) Switch utilization ratios (SUR). (b) Estimated ripple voltage of CHB and buck-dc/dc backend converters. $L = 30$ μH, $C = 60$ μF, $N_{mdl} = 8$, f_s(buck) = $N_{mdl} f_s$(CHB) = 40 kHz, and $V_{mdl} = 40$ V. The influence of the frontend inverter is ignored.

The numerical results are shown in Fig. 4(b) with the parameters of TABLE I. The effective switching frequencies of both topologies are matched. The adaptive dc battery produces much smaller voltage ripple because of the fractioned switching voltage. As such, the adaptive dc battery can use a much smaller L-C filter and/or switching frequency than that of a buck backend.

C. Loss Comparison

We compare the losses across three cases through SPICE simulations: the proposed modulated dc link, conventional inverter with SVPWM, and conventional inverter with discontinuous PWM (DPWM) [21], [23], [24]. In SVPWM, the transistors are constantly switching, whereas DPWM injects a special common-mode modulation reference, e.g.,

$$m_{com} \atop (DPWM) = \begin{cases} 1 - \max\left\{m_a, m_b, m_c\right\}, \\ \quad \text{if } \max\left\{m_a, m_b, m_c\right\} > -\min\left\{m_a, m_b, m_c\right\}; \\ \min\left\{m_a, m_b, m_c\right\} - 1, \\ \quad \text{if } \max\left\{m_a, m_b, m_c\right\} \leq -\min\left\{m_a, m_b, m_c\right\}. \end{cases}$$

so that $^1/_3$ of the switches remain untoggled. Even compared to DPWM, the proposed solution halves the switching actions.

The detailed simulation settings are listed in TABLE I. In the conventional setup, the dc link is fixed at 640 V and the main inverter is kept the same as that of the proposed system (FF300R12ME4, Infineon). Across all cases, we fix the peak output current to 200 A but vary the modulation index and the power factor. Low modulation indices emulate smaller back emf under low speeds, whereas the combination of higher modulation indices and low power factors (cos φ) reflect field-weakening under high speeds.

Fig. 5 details the converter losses. Despite the additional loss in the FETs, the proposed topology notably reduces the overall loss under all conditions thanks to the fewer switching actions in the frontend inverter. The relative ratio of the IGBT switching losses for the three evaluated cases is approximately

1:2:3 as predicted. The IGBTs' conduction losses are identical across all cases because of the controlled output current; the FET loss decreases at lower power factors due to the cancellation effect at the dc link.

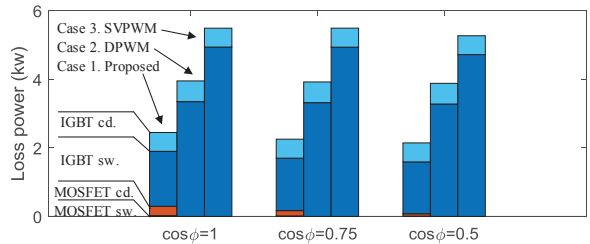We selected FF300R12ME4 (IGBT) and IPT007N06N (FET)

TABLE I
Simulation settings

Shared parameters		
Output power	P	100 kW ($m = 1$)
Output current		200 Apk
Output frequency	f	50 Hz
Frontend inverter		IGBT: 300 A/1200 V (FF300R12ME4[†], Infineon)
IGBT gate driver		+15 V /−5 V ideal, $r_g = 1.8$ Ω
Frontend inverter switching frequency	f_{inv}	10 kHz (i.e., 3.3 kHz per switch)
Case 1: Proposed modular multilevel dc-link motor drive		
Backend modules		40 V × 16
DC-link voltage	v_{dc2}	0–640 V adjustable
Module switch		FET: 0.75 mΩ, 300 A/60 V (IPT007N06N[‡], Infineon)
Module switching frequency	f_{mdl}	5 kHz (i.e., 90 kHz at v_{dc1})
FET gate driver		+15 V /−5 V ideal, $r_g = 1.8$ Ω
Frontend reference	m_x	Eq. (2)
Backend reference	m_{dc}	Eq. (4)
Cases 2 and 3: two-level three-phase inverter		
DC-link voltage	v_{dc}	640 V fixed

[†] Provided in PSpice default library.
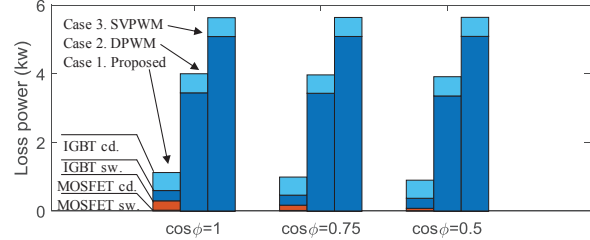[‡] SPICE model downloadable from www.infineon.com.

Fig. 5. Loss breakdown of three different cases under (a) 95% modulation index, (b) 75% modulation index, and (c) 50% modulation index. The switching loss of the FETs is barely visible.
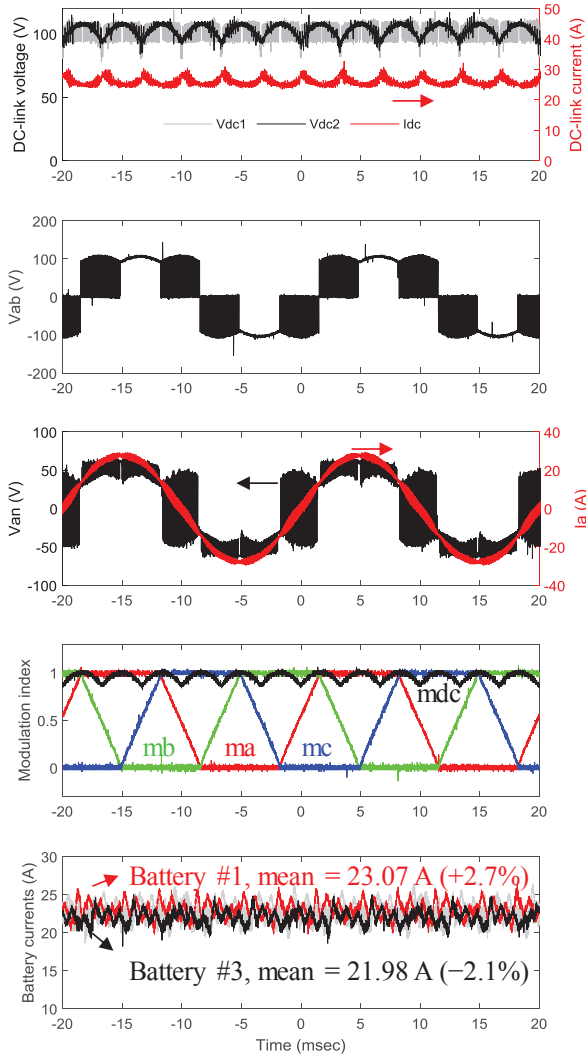
Fig. 6. Waveforms under 3 kW three-phase passive load. Balancing is active between battery #1 and #3.

based on the availability of accurate models and the matched cost. The relative benefit of the proposed solution depends on the choice of the frontend IGBT. There are several motor-drive-specific features favoring the prosed solution: *1)* at low speeds and thus smaller back emf, the frontend IGBTs of the proposed solution experience significantly less switching stress as is evidenced by Fig. 5(a)–(c); *2)* at high speeds and thus lower power factor due to field-weakening, the currents mostly cancel at the dc link, producing small conduction loss at the FETs; and *3)* the FET loss is dominated by the conduction loss, which can be reduced and easily scaled for higher current loads by paralleling more silicon, whereas the IGBTs' switching loss does not decrease in the same manner.

We further used passive loads to evaluate the THDs of the three configurations. For each phase $R_{load} = 1.75\ \Omega$, $L_{load} = 200\ \mu H$. The results are shown in Fig. 3. The proposed converter maintains a low THD (5.3%) across all modulation indices whereas both DPWM and SVPWM suffer higher distortion at lower modulation indices.

V. EXPERIMENTAL RESULTS

A. Setup

We implemented the adaptive dc battery with eight modules. Each module contains a FET half-bridge, a four-cell LiFePO$_4$ battery, and an L-C filter with $L_{mdl} = 10\ \mu H$, $C_{mdl} = 1.5$ mF to smoothen the battery current. Between the backend and the frontend converters, we placed a dc-link filter with $L = 30\ \mu H$ and $C = 60\ \mu F$, which resonates at 3.75 kHz. To avoid resonance with the filter, the frontend motor inverter operates with a 10-kHz carrier. Under the proposed modulation scheme, each transistor switches at 3.33 kHz on average; whereas the backend modules switch at 5 kHz and thus effectively 40 kHz at v_{dc1}. Both the frontend and the backend are controlled by an FPGA (sbRIO 9627, National Instruments).

B. Results

Fig. 6 presents the measurements under 3-kW inductive load, where each phase is implemented with 2.2 Ω and 100 μH in series. The waveforms of v_{dc1} x-axis and v_{dc2} show a negligible phase lag. The dc-link current is relatively constant. Comparing the phase voltage v_a, phase current i_a, and modulation reference m_a, it is clear that *1)* only a third of the frontend transistors are switching; and *2)* the frontend transistors only switch at low currents. The same observations apply to other phases. As long as the power factor $\cos \varphi > 0.5$, the current peaks are shaped exclusively by the backend converter, which presents small switching ripples and distortion despite the low switching effort.

The above passive-load tests are operated at a modulation index of 95% (i.e., 95% × 1.13 = 107% utilization of the dc-link voltage); meanwhile, the modulation references within the adaptive dc battery are intentionally modified to create an active balancing current between batteries #1 and #3 (bottom of Fig. 6). Only a mild differential current (~2%) is created due to the limited overhead room of the modulation index at 95%; however, the current is still sufficient for battery balancing in practice.

VI. CONCLUSION

The presented distribution of motor control and modulation across an adaptive dc battery and a drive inverter demonstrated lower overall switching loss, superior distortion and low dv/dt stress. Thus, it has great potential for reducing motor insulation stress, bearing currents, and switching loss as well as increasing the output quality and round-trip efficiency. Existing solutions, typically with dc/dc converters, have various drawbacks including limited operating range, no support in active battery management, as well as marginal efficiency gain that can barely justify the additional high-voltage high-power transistors as well as large magnetic components and their substantial cost.

Instead, this paper proposes and comprehensively exploits a modular adaptively reconfigurable multilevel dc battery to modulate the input voltage of a subsequent six-switch motor inverter—a technology that is also studied by the vehicle industry, though for quasi-static voltage adjustment and battery management. The modular adaptive dc battery allows the use

of latest high-performance low-voltage FETs and thus surrogates the hard switching of the main inverter at a negligible switching effort. Despite the additional loss in the FETs, the proposed solution notably reduces the overall loss under various modulation indices and power factors for a wide range of operating conditions. Additionally, the adaptively reconfigurable dc battery offers active balancing of capacitance, power, and ageing, eliminating the high vulnerability from weak cells in conventional hard-wired batteries, while further turning the drive train to a normally-off safe low-voltage system. Further improvements in the future may be achieved by adding dynamic parallel connectivity to the modules [36]–[38]. The advantages of the proposed solution are quantified by accurate SPICE simulations and verified by experiments.

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