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REVIEW

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Reliability challenges of gate dielectric materials in transistors

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Abstract

The gate dielectric plays a critical role in field-effect transistors since it determines the capability of gate control and the reliability of the device. In modern large scale integrated circuits, the stacking of high-k oxides has become an indispensable strategy to enable the continuous shrinking of the device. However, the multiple interfaces, various kinds and large number of defects have brought about significant reliability issues such as threshold voltage shift, gate leakage current, random noise, hysteresis, fixed charges and so on. Effectively dealing with these reliability issues has become the main challenge of dielectric design. On the other hand, with the emerging of two-dimensional (2D) channel materials, traditional oxide dielectrics turn out to be nonideal due to their surface dangling bonds. The development and design of new gate dielectrics become urgent and attractive. In this review, we will summarize the advantages and challenges of different dielectrics that are applicable to several mainstream channel materials, including Si, SiC, GaN and 2D materials. For each kind of dielectric, possible strategies to improve its reliability are discussed.

KEYWORDS

dielectric material, high-k, reliability challenges, transistor

1 | INTRODUCTION

After about 60 years of development, field effect transistors (FETs) have evolved from planar configurations to FinFETs,[1–3] and now going to Gate-All-Around FETs,[4–6] as schematically shown in Figure 1. Accompanying the structural evolution, the supply voltage has been reduced to less than 1V, and the size of each device has been reduced to nanometer scale. All these features have contributed to the realization of high performance, high integration, and low power consumption of modern very-large-scale integration (VLSI) circuits.

At the current state, further development of transistors is more and more challenging. Typically, the dominant channel material, Si, and the traditional gate oxide, silicon dioxide (SiO_2), are both reaching their size and physical limits. Further scaling will result in larger scattering, larger gate leakage, and larger variation. For the gate dielectric, one adopted solution is replacing the SiO_2 by materials with higher dielectric constant (high-k), but this introduces more interfaces and more defects, and thus results in some reliability issues such as threshold voltage shift, fixed charges, interface dipoles, trap assisted leakage currents, and so on. Further physical study and process development is in great demand. For the channel material, one promising strategy is turning to the ultra-thin two-dimensional (2D) semiconductors, but the gate dielectric issue is still an inevitable challenge. Specially, traditional oxides that work well with Si usually present lots of surface dangling bonds, and thus are not

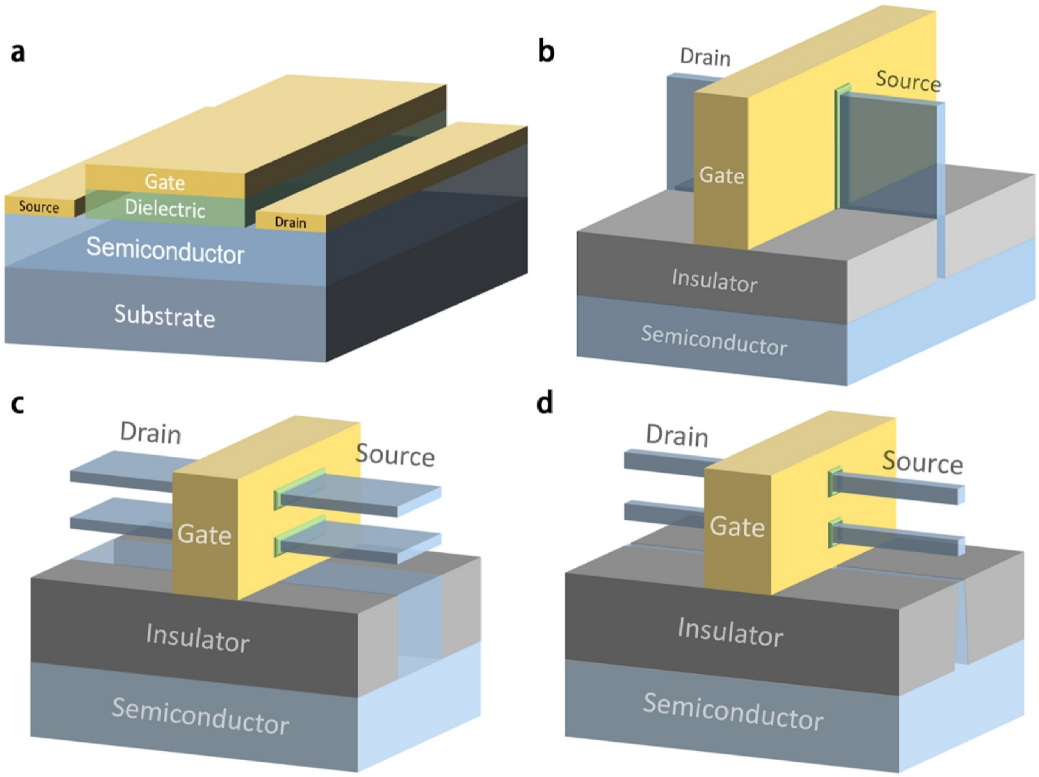


FIGURE 1 The structure evolution of transistors. (A) Planar FET, (B) FinFET, (C) nanosheet GAAFET, (D) nanowire GAAFET. FET, field effect transistor; GAAFET, Gate-All-Around FET.

compatible with the dangling bond free 2D materials. How to find or develop compatible gate dielectrics for 2D materials is an important and attractive mission.

In summary, to promote the further development of advanced transistors, including their performance and reliability, a comprehensive knowledge and in-depth understanding of various gate dielectric materials are definitely indispensable. For this purpose, we reviewed the properties and applications of a series of dielectric materials, including the traditional SiO_2, the commonly used high-k dielectrics for Si, and the emerging dielectrics for 2D semiconductors, aiming to clarify their advantages and limitations, and further provide suggestions to practical applications. In the second section, we will discuss the common reliability issues in existing transistors. In the third section, we introduce some common and novel gate dielectric materials, summarizing their advantages, limitations, and methods commonly used to enhance reliability. Finally, in the fourth section, we present a summary and outlook on the development and application of gate dielectric materials.

2 | TYPICAL RELIABILITY ISSUES

With the development of transistors toward smaller sizes, the impact of atomic defects and quantum effects become more significant, leading to a series of reliability issues in transistors, including random telegraph noise (RTN), bias temperature instability (BTI), time-dependent dielectric breakdown (TDDB), hot carrier degradation (HCD)[7–10] and so on. These reliability issues manifest themselves as the variation in the drain current, shift of threshold voltage, aggravation of leakage current, and so on.

2.1 | Random telegraph noise

RTN is a specific type of electronic noise, as shown in Figure 2A,[11] which is characterized by rapid transitions of measured quantities such as current, voltage, or resistance between two or more discrete values over time.[12,13] These fluctuations are particularly pronounced in devices with scaled-down channel dimensions.[14,15] Additionally, the amplitude of the RTN increases with decreasing gate bias and becomes large in subthreshold conditions.[16] The physical origin of the RTN phenomenon has been deeply explored, and it is believed that it is related to the capture and decapture of single carriers by the defect in the device, as schematically shown in Figure 2B. As device dimensions shrink, predicting RTN in nanoscale Metal-Oxide-Semiconductor (MOS) devices and circuits becomes increasingly crucial. The hole in the inversion layer (HIL) model proposed by L.D. Yau et al.[17] has been

optimized several times to define the hole and to modify its scaling limits and validation range.[18] The HIL model has been shown to be effective in the prediction of RTN phenomena in larger devices. Kirton and Uren et al.[19] studied and summarized the relationship between RTN and the capture and emission of carriers by individual defects in transistors as early as 1989, and the two-state Nonradiative Multi-Phonon (NMP) model was mentioned. Since then, more research has been done on the relationship between RTN phenomena and defects. Grasser et al.[20] analyzed the microscopic oxide defects described by the four-state NMP model, revealing the details of the mechanism of oxide charge defect capture leading to RTN degradation at the microscopic level. Wang et al. investigated the complicated RTN mechanisms, including the impacts of metastable states in a single trap and the coupling mechanisms among different traps.[21]

2.2 | Bias temperature instability

BTI refers to the reduction of saturation current and increase of threshold voltage of a MOS device under continuous operation. The BTI issue depends greatly on gate bias and temperature, and it can happen even at low V and low T. Figure 3A shows the threshold voltage shift and recovery process due to BTI in the experiment.[22] The two main types of BTI are the Negative Bias Temperature Instability (NBTI) occurring in p-MOSFETs and the Positive Bias Temperature Instability (PBTI) occurring in n-MOSFETs.[23–25] in addition, the NBTI in n-MOSFETs and the PBTI in p-MOSFETs have also been reported,[26,27] these two types of BTI degradation generally have less impact on the macroscopic parameters of the device, but are still very important.

Since the discovery of BTI in SiO_2 dielectrics in the 1960s,[28,29] the origins of BTI have been extensively studied. One big advance came in 2011, when Grasser et al. suggested the paradigm shift in understanding BTI from reaction-diffusion model to charge trapping/detrapping model.[30] As shown in Figure 3B, pre-existing and newly generated defects in the oxide of MOS devices can capture charges, especially in elevated oxide electric fields caused by continuous high temperature and high bias, leading to the occurrence of BTI.[31,32]

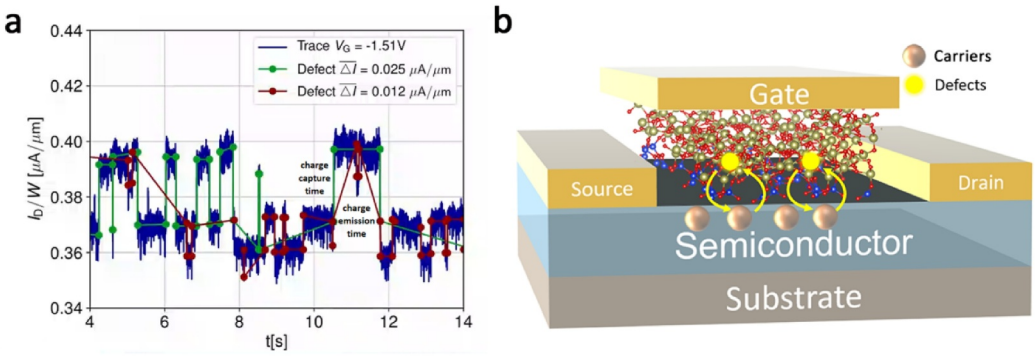


FIGURE 2 (A) Typical experimental random telegraph noise signal. Reproduced with permission.[11] Copyright 2020, Proceedings of the Device Research Conference. (B) The trapping and detrapping of carrier by defect in MOSFET. MOSFET, metal-oxide-semiconductor field-effect transistor.

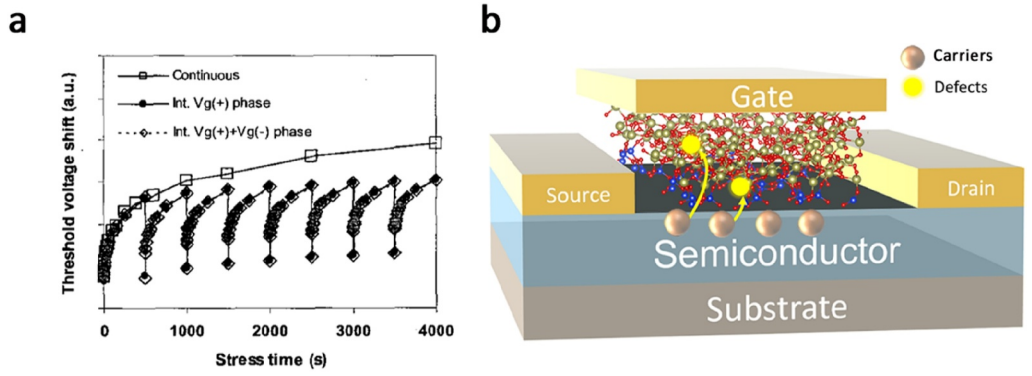


FIGURE 3 (A) Threshold voltage shifts in a 2 nm nitrided oxide for a continuous stress (open squares) at $V_g = -2.5$ V and for interrupted stress with a positive bias interval ($V_g = +1.5$ V) (filled circles). Reproduced with permission.[22] Copyright 2004 Published by Elsevier Ltd. (B) Schematic diagram of trapped charge of defect in gate dielectric layer.

2.3 | Time-dependent dielectric breakdown

TDDB refers to the phenomenon that the gate oxide leakage current gradually increases and finally breaks down even though the applied voltage is not very high.[33] Actually, E. Y. Wu et al. have proved that breakdown is a phenomenon related to temperature, gate voltage, oxide thickness, and time-dependent. Breakdown is a stochastic quantity and is distributed, typically via a Weibull distribution.[34] Figure 4A shows the TDDB results of silicon-based wafers with $Co_{0.65}Ti_{0.35}$ layer added, and it can be clearly seen that breakdown occurred after about 100s.[35] The occurrence of TDDB is primarily due to the formation of conductive paths through traps in the oxide under prolonged stress, eventually resulting in oxide breakdown. Figure 4B is a schematic diagram of the inverted channel formation in Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET). The statistical physical model of the TDDB phenomenon was first proposed in 1990.[36] Subsequently, a new model based on percolation theory was introduced,[37] explaining that thin oxides are more prone to TDDB because they require fewer defects to create a percolation path. In addition, it has been proposed that the hydrogen atom related defects have a large contribution to the stress-induced leakage current, which is one of the main reasons for the time-dependent breakdown of the dielectric layer.[38] A few years ago, the dynamic migration behavior of hydrogen atoms has also been found to be closely related to the dynamic degradation of the gate dielectric.[39]

2.4 | Hot carrier degradation

HCD refers to the phenomenon where the current-voltage characteristics of a device degrade due to the injection of high-energy carriers into the gate oxide layer in transistors.[40,41] The high-energy carrier injection will generate interface and oxide defects, and then induce defect states and capture charges, causing damage to the oxide layer. As the extent of the damage increases, the electrical performance of the device eventually degrades. Figure 5A shows HCD results in Input/Output devices.[42] The theoretical study of HCD

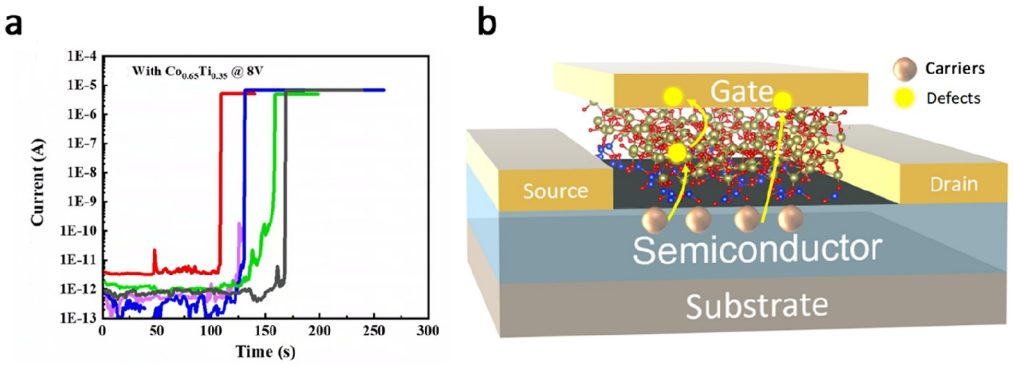


FIGURE 4 (A) Relationship of current and time when devices were applied with 8 V voltage at 100°C with $Co_{0.65}Ti_{0.35}$. Reproduced with permission.[35] Copyright 2022, Zhou et al., under exclusive license to Springer Science Business Media, LLC, part of Springer Nature. (B) Schematic diagram of the inverted channel formation in MOSFET. MOSFET, metal-oxide-semiconductor field-effect transistor.

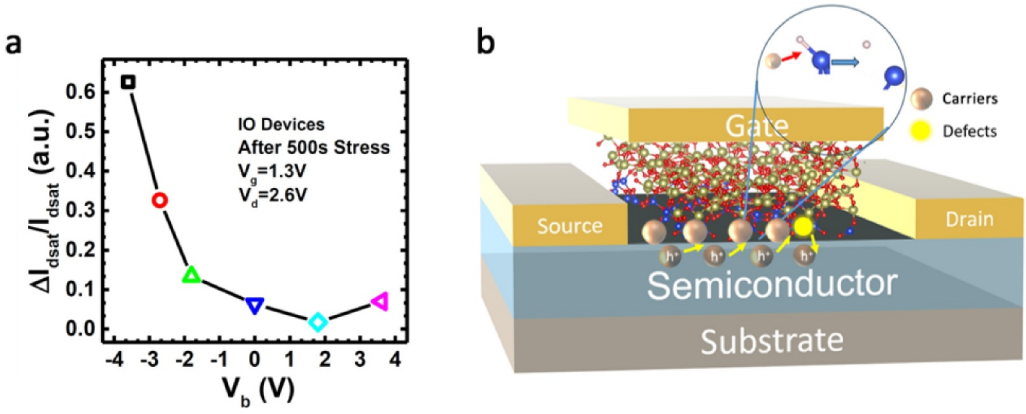


FIGURE 5 (A) The measured hot carrier degradation results in devices after 500 s stress in different body voltage. Reproduced with permission.[42] Copyright 2018, IEEE. (B) Schematic diagram of the high-energy carrier injected into the gate oxide layer and breaking the silicon hydrogen bond.

has been ongoing, and in 1985, a simple functional model, as known as the Hu model relating HCD to substrate current and time was proposed.[40] Subsequent experimental results indicated that HCD tends to saturate after the device experiences a certain level of electrical stress.[43,44] The nature of HCD is believed to involve the generation of trap charges in the oxide layer near the drain and interface states at the Si-SiO_2 boundary.[45] These interface states and charges produce corresponding potentials that prevent subsequent hot carriers from approaching the Si-SiO_2 interface, ultimately causing the saturation of HCD. Figure 5B shows a schematic diagram of the high-energy carrier injected into the gate oxide layer and breaking the silicon hydrogen bond. Liu et al. suggested that the Si-H bond breaking could be facilitated by additional H atoms near the interface.[46]

3 | GATE DIELECTRIC MATERIALS IN CONVENTIONAL TRANSISTORS

In this section, we will summarize the properties of defects in different kinds of gate dielectrics, their impact on transistor reliability issues, and possible improvement strategies. This will help people better understand the microscopic origin of reliability issues, and then think about solutions accordingly.

3.1 | SiO_2

From the early 1970s to the early 2000s, SiO_2 was consistently chosen as the primary material for the insulating gate oxide in MOSFET transistors.[47–49] SiO_2 is an excellent insulator with a bandgap of up to 9 eV, a dielectric breakdown strength of up to 10^7 V/cm, and a dielectric constant of approximately 3.9 at room temperature.[50–52] Additionally, SiO_2 is cost-effective, easy to manufacture, and highly compatible with bulk silicon. High-quality thin films of SiO_2 can be conveniently grown on semiconductor substrates using processes such as thermal oxidation for device fabrication.[53–56] Besides, SiO_2 is not only used in silicon-based transistors, but also widely used in SiC-based transistors. Unfortunately, amorphous SiO_2 contains a variety of defects, such as oxygen vacancies, interstitial hydrogen, and dangling bonds.[57,58] These defects will cause charge capture and emission effects, and then induce notable device reliability issues such as threshold voltage shift, carrier mobility reduction, transconductance decrease, and gate leakage current. Amorphous SiO_2, as the most important dielectric layer material, although its defect density is low compared to other material systems, the reliability problems caused by defects can still not be ignored. Therefore, it is necessary to know the typical types of the defects.

3.1.1 | Typical defects

Among the defects, oxygen vacancies are one of the most prevalent defects in oxides. Figure 6A[59] shows the classical dimer structure of the oxygen vacancy in SiO_2, with an electronic state shared by two silicon atoms. Interstitial hydrogen defects mainly occur when hydrogen atoms from passivation processes enter the amorphous SiO_2 layer. If oxygen vacancies are present, hydrogen atoms can form hydrogen bridge defects at these sites as shown in Figure 6B. Additionally, if a hydrogen atom bonds with an oxygen atom while a Si-O bond is breaking,[58] it creates a silicon dangling bond and a hydroxyl defect as shown in Figure 6C.

Silicon dangling bonds are more common at the Si/SiO_2 interface, primarily formed during silicon oxidation. Common interface dangling bonds, include Pb0 and Pb1 defects, both found on sp^3-hybridized silicon atoms but in different local bonding environments.[60,61] A typical wave function of interface defect is shown in Figure 7A. The researchers simulated the bond-breaking process of Si-H bond on the Si/SiO_2 interface by theoretical calculation, and found that Si-H bond has a high energy barrier, the Si-H bond on the normal interface is generally resistant to electron injection.[62]

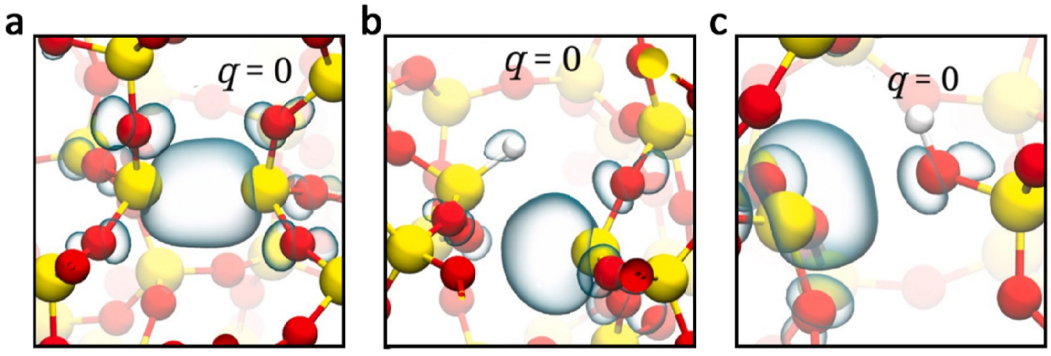


FIGURE 6 Three defects in the amorphous silicon oxide layer of transistors. (A) Oxygen vacancy defect, (B) hydrogen bridge defect, (C) hydroxyl defect (The yellow, red and white spheres represent silicon, oxygen and hydrogen atoms, respectively.). Reproduced with permission.[59] Copyright 2022, published by Elsevier Ltd.

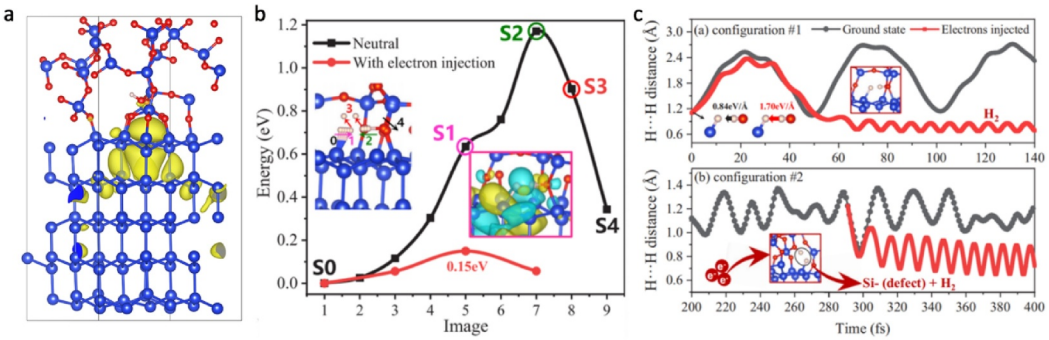


FIGURE 7 (A) The wave function of SiO_2/Si interface defects. (B) The reaction barrier of the precursor with the "Si-H···H-O" complex. (C) The carrier induced Si-H bond breaking and H_2 formation in two different Si-H···H-O configuration. The additional H atom bonds with an O atom (top) at the exact Si-SiO_2 interface and (bottom) inside the amorphous oxide. Reproduced with permission.[62] Copyright 2021, by the American Physical Society.

The hydrogen atom near the silicon hydrogen bond plays an auxiliary role in the breaking of the Si-H bond. An H atom attached to an O atom near the Si-H bond will form a "Si-H…H-O" complex, which is considered to be the more likely structure to form. As shown in Figure 7B, the Si-H bond barrier is further reduced after electron injection. When two H atoms are close to each other, the energy of the unoccupied Si-H state is also greatly reduced. Figure 7C shows the dynamic Time-Dependent Density Functional Theory process of Si-H fracture, which also proves the assistant effect of H-O local configuration on Si-H bond breaking.

3.1.2 | Improvement strategy

Research aimed at improving dielectric reliability has been ongoing for many years. Enhancing gate dielectric quality can primarily be achieved through improving the material quality itself and the interface quality. Both approaches involve attempts to control and reduce the defect concentration to optimize device performance. The fabrication process has been optimized as much as possible to reduce the defect concentration $<1e^{10}$ cm^{-2}. The most common method for fabricating amorphous SiO_2 is thermal oxidation. This involves introducing oxidation gases into a heated furnace containing silicon wafers. The gas molecules then diffuse into the silicon wafers and react with their surface to form a SiO_2 film.[63] To improve the quality of SiO_2, refining the fabrication methods is crucial. In Complementary Metal Oxide Semiconductor (CMOS) processes, factors such as wafer quality, oxidation, and annealing processes can impact gate dielectric reliability. Particularly, high-temperature annealing processes, generally above 1200°C, can reduce the performance of the device.[64,65] Most improvements in fabrication methods focus on surface preparation, such as using two-step plasma-enhanced chemical vapor deposition and low-temperature solvent cleaning techniques,[66] to achieve smoother and more uniform silicon interfaces, thereby reducing scatter-induced mobility reduction and leakage current.

Doping with other atoms can also enhance the reliability of SiO_2 gate dielectrics. In 1989, NISHIOKA et al.[67] discovered that injecting low-energy fluorine atoms onto the polysilicon gate surface and diffusing them into the SiO_2 gate dielectric through high-temperature annealing could reduce the concentration of interface defects and threshold voltage drift within a certain fluorine doping concentration range, and also mitigate HCD effects. Similarly, introducing chlorine atoms into SiO_2 through annealing under specific conditions can suppress interface states generated by hot carrier effects.[68] Doping amorphous SiO_2 with fluorine or chlorine will replace the Si-H bond by more stable Si-F and Si-Cl bonds, thereby reducing interface state density. However, excessive doping of fluorine or chlorine atoms can lead to the formation of non-bridging oxygen centers, which in turn reduces device reliability. Nitrogen doping and hydrogen passivation are also common treatments for SiO_2 gate dielectrics. The introduction of radical plasma nitridation oxide reduces SiO_2 gate leakage current and inhibits the penetration of boron atoms.[69,70] N_2 plasma pretreatment of SiO_2 when stacked as intercalated with high k material has also been shown to effectively reduce oxygen vacancy defect and interface defect density and reduce leakage current density.[71] With advancements in computational materials science, research into the mechanisms of defect formation and the effects of various atomic dopants in SiO_2 continues to progress, offering guidance on determining the optimal doping concentrations.[72–74]

3.1.3 | SiO_2 in SiC device

Currently, SiC-based transistors have a wide bandgap and excellent performance, making them suitable as channel materials for power semiconductor devices. In

SiC-based transistors, the SiO_2 gate dielectric layer can be obtained through methods like thermal oxidation of SiC, Tetraethoxysilane and so on, which inevitably results in the production of defects at the interface. Nitrogen incorporation is a common method to reduce the density of defect states, with NO or N_2O being typically used.[75,76] Recently, it has been reported that using N_2O diluted by N_2 (10%) instead of NO for annealing, and reasonably controlling the annealing time, lower interfacial state density and higher transconductance and mobility can be obtained at 90°C.[77] Additionally, the use of spacer etching technology during device fabrication has been reported to increase the breakdown field strength by approximately 59.2% while also reducing the risk of hidden defects.[78]

Unfortunately, the N passivation will not solve the problem once for all. Interface defects will be generated again during device operation. Recently, the defect generation in N passivated SiC-SiO_2 interface was studied.[79] The upper and lower figures in Figure 8A are respectively the models of the SiC/SiO_2 interface with carbon clusters and silicon vacancies after nitrogen passivation, and Figure 8B shows the simulation results of the structural changes of C cluster defects after nitrogen passivation. It can be seen from the figure that the C-N bond length in this structure fluctuates between 1.4 and 1.8 Å, indicating that at 400 K, when the C-N bond length exceeds 1.8 Å, the C-N bond is not in the normal fluctuation range. The local state energy level associated with the N atom is close to the valence band maximum (VBM) of silicon carbide and far away from the conduction band minimum (CBM) of silicon carbide, which is more difficult to capture electrons than the C-cluster defect. Figure 8C shows the change of C–N bond length after hole injection. The process of bond breaking in SiC/SiO_2 interface models with C-cluster after N passivation can be seen. It has been suggested that the passivated C-clusters are more likely to form new defects than Si vacancies. It is of guiding significance to improve the nitrogen passivation condition and eliminate the failure condition after nitrogen passivation.

3.2 | High-k oxides

Due to the limitations of the dielectric constant of SiO_2, high-k materials have increasingly gained prominence in the microelectronics industry. In 2007, with the advent of Intel's new 45-nm microprocessors, high-k gate dielectrics entered the market, combined with silicon-based insulators to form a new generation of gate dielectric stacking structures.[80] High-k materials offer a lower equivalent oxide thickness (EOT)[81] and higher gate capacitance for a given thickness. EOT can be calculated as Equation (1), where ε stands for dielectric constant and t stands for material thickness:

$$\mathrm{EOT} = \varepsilon_{SiO_2} \times t_{sio_2} / \varepsilon_{HighK} \quad (1)$$

At present, in the entire chip industry market, candidate materials for high-k oxides include alumina, hafnium oxide (HfO_2), zirconium oxide, lanthanum oxide (La_2O_3) and so on.[82–87] Gate dielectric layer materials require a high dielectric constant, a large band gap, and good contact and compatibility with channel materials (generally silicon), and they must also ensure good thermal stability under high-temperature conditions.[88] Figure 9 shows the relationship between bandgap and permittivity of some candidate gate dielectric material. It can be seen that the permittivity and bandgap are in an inverse relationship, which limits the selection of dielectric materials.[89,90] Among the various candidate materials, HfO_2 is currently the most prominent due to its excellent electrical and mechanical properties, as well as its thermal stability.[91–94] The application of high-k materials significantly extends the scale limit of the gate dielectric layer while contributing to the reduction of gate leakage. However, challenges remain in the application of high-k materials in transistor

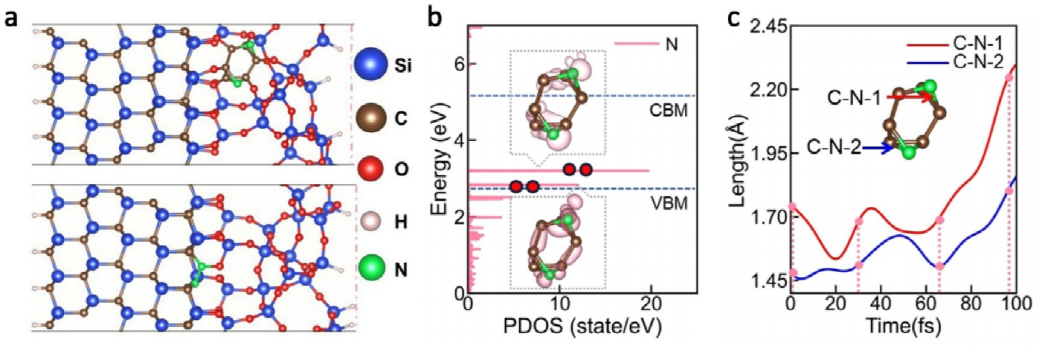


FIGURE 8 (A) SiC/SiO_2 interface models (top) with C-cluster after N passivation, (bottom) with Si vacancy after N passivation. (B) Structural vibration of C–N bond in SiC/SiO_2 interface models with C-cluster after N passivation over time. (C) Change of C–N bond length after hole injection. Bond breaking process in SiC/SiO_2 interface models with C-cluster after N passivation. Reproduced with permission.[79] Copyright 2024, rights managed by AIP Publishing.

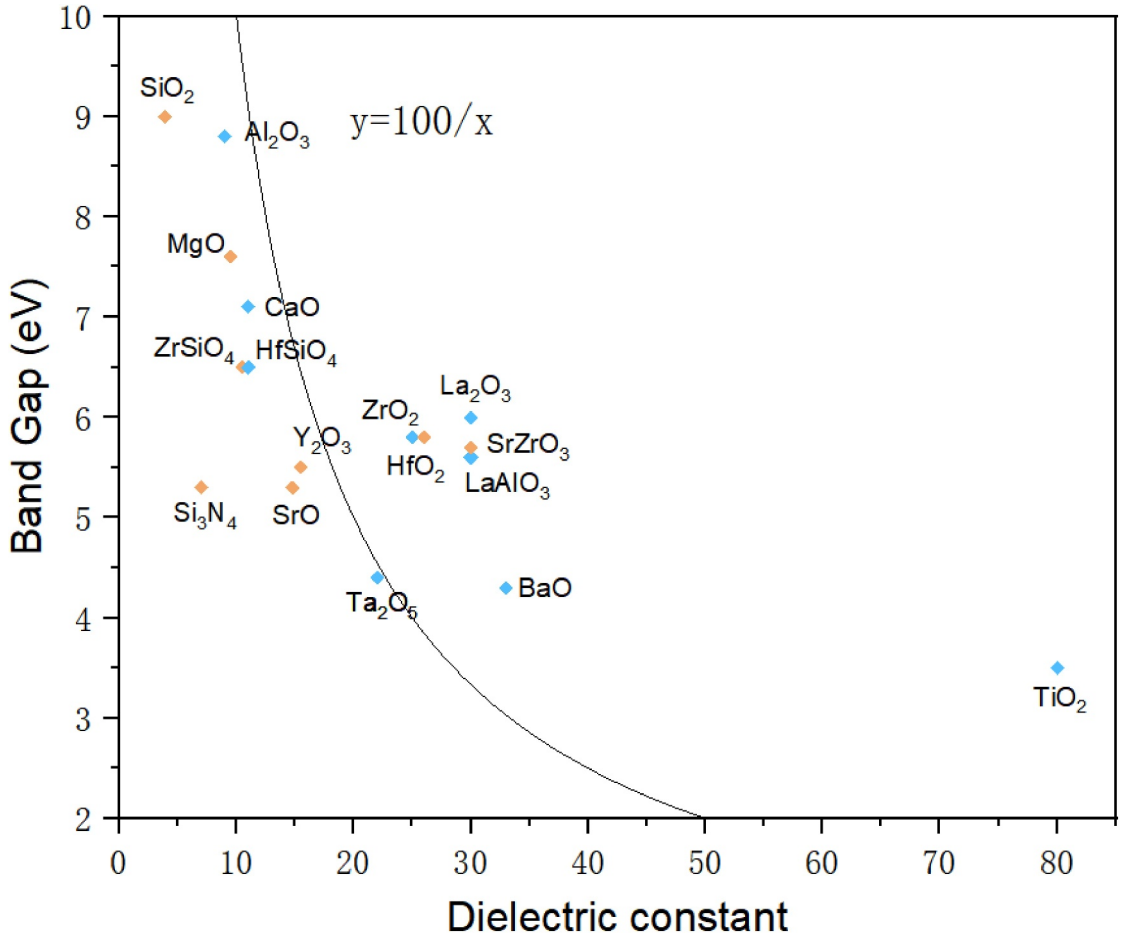


FIGURE 9 The relationship between the band gap and the dielectric constant applies to a number of potential gate dielectric candidates.

dielectrics, such as high defect content in the material and low interfacial lattice configuration, which lead to various device reliability issues.[95–98] Additionally, traditional gate oxide materials like SiO_2 are often used in conjunction with high-k materials to create more ideal interfaces between the gate dielectric and silicon.[99–101] This section will introduce several commonly used high-k materials.

3.2.1 | HfO_2

Due to its superior thermal, electrical, and mechanical properties, HfO_2 is currently the most extensively researched and widely used high-k oxide in the field of integrated circuits. One notable feature of HfO_2 is its high dielectric constant, reaching up to 25, which is 7–8 times greater than that of SiO_2. This significantly benefits the reduction of transistor size limitations. However, HfO_2 has moderate thermal stability, and crystallization can occur around 400°C, in hafnium dioxide (HfO_2), there are more defects at grain boundaries, and the defects assist in the enhancement of the leakage current conduction mechanism, and the leakage current flows along the grain boundaries, which affects the reliability of the device. Additionally, the fabrication process for high-quality HfO_2 layers is complex, which may affect the interface quality.[92–94,102–105]

3.2.1.1 | Typical defects

HfO_2 is a high-k dielectric material that is often used in combination with SiO_2 to form the gate dielectric layer in modern transistors. The inclusion of HfO_2 adds complexity to the distribution and types of defects within the gate dielectric layer, making the mechanisms behind reliability issues more intricate. The defect structure and electronic properties of oxygen vacancies in $Si/SiO_2/HfO_2$ stack have been well-documented.[46] As shown in Figure 10, when the oxygen vacancy is located in the SiO_2 layer, its defect level is much lower than the VBM of Si, when the oxygen vacancy is located at the SiO_2/HfO_2 interface, its defect level is slightly lower than the VBM of Si, and when the oxygen vacancy is located in the HfO_2, its defect level enters the Si band gap. The closer the defects are to the VBM, the easier it is to exchange hole carriers with the VBM. These results show that the oxygen vacancies inside

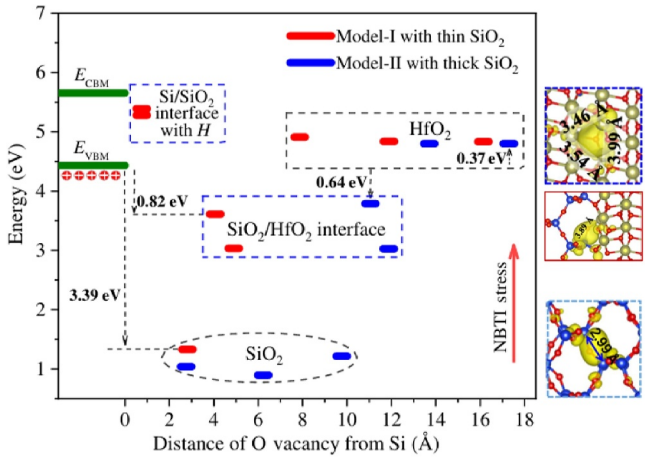


FIGURE 10 Distribution of defect energy level of differently distributed oxygen vacancy defects relative to the silicon band gap edge in the SiO_2/HfO_2 interface model. Reproduced with permission. Reproduced with permission.[46] Copyright 2019, by the American Physical Society.

SiO_2 are not active, but in HfO_2 MOSFETs, both the oxygen vacancies at the SiO_2/HfO_2 interface and inside HfO_2 are active hole trapping centers.

3.2.1.2 | *Improvement strategy*

To passivate the defects in HfO_2 MOSFETs, hydrogen is introduced into high-k MOS devices. However, hydrogen atoms not only interact with defects, but also interact with normal oxygen and hafnium atoms. As a result, some new defects that are related to hydrogen will be generated after hydrogen annealing. Methods for distinguishing different types of defects in MOS devices have been reported,[106] highlighting the significant impact of hydrogen-related defects on the reliability of high-k gate dielectrics. Kaviani et al. investigated the interactions of hydrogen atoms in amorphous HfO_2 (a-HfO_2),[107] while Li Jing et al.[108] studied the interactions between hydrogen atoms and oxygen vacancy defects in a-HfO_2. Their research suggests that the presence of oxygen vacancies near hydrogen atoms can lower the migration barrier for hydrogen, facilitating its movement.

Moreover, the passivation effect of HfO_2 films was found to be related to the annealing time, temperature, atmosphere conditions and so on.[109] Figures 11A,B show the effective minority carrier lifetime (t_{eff}) and surface recombination velocity of thick HfO_x samples with different types silicon substrates and different annealing times at 400 and 450°C. Different temperatures, different annealing times and different substrate types all have effects on the annealing quality of samples. Figures 11C,D show the injection level dependence of the measured t_{eff} of the bare, As-deposited (AD) and annealed samples (450°C, 45 min) of p-Si and n-Si substrate, respectively. In both cases, the bare wafer curve lies above the curve of the AD sample at all injection levels, which indicates that the silicon surface quality was compromised during deposition which might have led to increased surface defects and thus poor passivation quality. The positive effect of the hydrogen annealing environment on the sample quality and electrical properties is demonstrated. Fluorine atom passivation can be achieved by forming Hf-F bonds in the HfO_2 layer, which helps to passivate interface states and defects within the HfO_2 layer.[46,110] However, fluorine plasma treatment can lead to the regeneration of the interface layer (IL), which can result in decreased oxide capacitance and worsened electrical characteristics.

Enhancements in processing techniques and conditions can significantly improve the reliability of HfO_2 materials. The influence of oxygen on the quality of hafnium-based gate dielectrics has been investigated and reported. Specifically, the use of post-deposition annealing (PDA) with oxygen-ion incorporated high-k dielectrics has been shown to enhance device reliability and address reliability issues such as TDDB.[111] Additionally, multiple room-temperature annealing treatments in an ultraviolet ozone (UVO) environment for HfO_2 gate dielectrics have been demonstrated to reduce the concentration of oxygen vacancies.[112] This reduction in both bulk and interface defect densities results in improved electron mobility, reduced threshold voltage shifts, and diminished leakage currents. Fluorine passivation, when performed under low power and low temperature conditions, has also been shown to effectively suppress the formation of interface states.[113] Doping with nitrogen atoms is another widely utilized method for enhancing the performance of hafnium-based oxides. It is reported that the thermal and electrical properties of HfO_xN_y formed by doping N atoms are improved, and the crystallization temperature is increased by N doping, which can obtain greater band migration.[114,115] Furthermore, research indicates that sequential annealing with high-pressure H_2/D_2 followed by N_2 can effectively passivate dangling bonds and eliminate excess hydrogen.[116] This approach reduces threshold voltage drift, optimizes annealing conditions, and thus improves device reliability. In addition, doping of other atoms such as Al and Ti atoms also improves the properties of HfO_2, and Al-doped HfO_2 films have been proved to have better thermal stability and lower oxygen vacancy defect concentration than HfO_2.[117] HfTiO films have also been reported to have a higher k value and a more uniform and smooth indication, while the leakage current is also reduced.[118]

3.2.1.3 | *Ferroelectric HfO_2*

Beneficial from the ferroelectric polarization of HfO_2 with an orthorhombic structure (space group P_{ca21}), it can be used in non-volatile memory devices. The ferroelectricity in fluorite-structured oxides was first reported by Böscke et al. in 2011, which has since garnered widespread

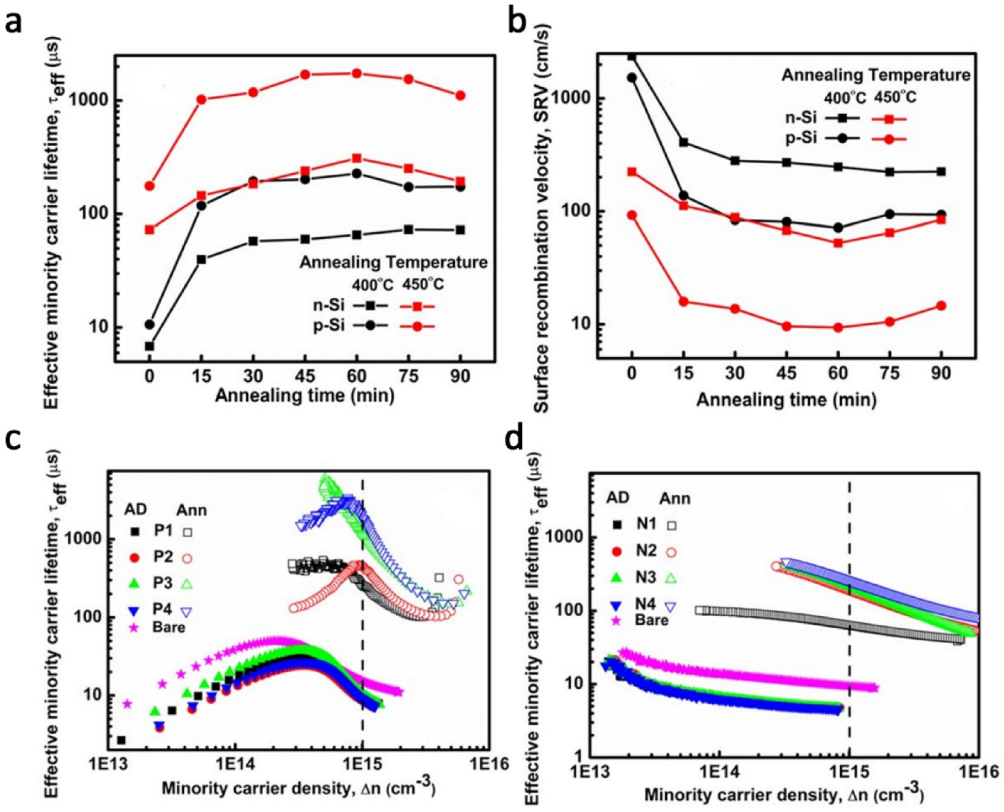


FIGURE 11 Change in (A) effective minority carrier lifetime and (B) surface recombination velocity with annealing temperature for different annealing durations for the sample prepared at 200°C substrate temperature by repeating 300 atomic layer deposition cycle. Injection level (Δn) dependence of the measured effective lifetime (t_{eff}) of as-deposited and annealed samples of (C) p-Si series (D) n-Si series. Reproduced with permission.[109] Copyright 2024, IOP Publishing Ltd.

attention in the fields of ferroelectricity and non-volatile memory.[119] Figure 12A shows the formation process of ferroelectric HfO_2. When the HfO_2 film is cooled with a cap, the shearing of the unit cell will be mechanically inhibited, and then the tetragonal phase HfO_2 will be transformed into the ferroelectric P_{bc21} phase. Figure 12B shows the good ferroelectric and antiferroelectric properties of the device by measuring sample polarization and piezoelectric displacement.[121] Unlike other emerging memories such as phase-change memory, the two spontaneous polarization states of ferroelectric memory can be electrically written and retained even without power. Ferroelectric memory offers fast write speeds and high energy efficiency, enabling non-volatile random access memory.[120] Furthermore, integrating ferroelectric field-effect transistors (FeFETs) into 3D structures may enable memory with greater density compared to Dynamic random access memory (DRAM) and superior random read speeds relative to Not AND flash.[122] Therefore, combined with the compatibility of Si process, HfO_2 is considered a promising candidate for future memory devices.

A memory cell involves write, read, and storage operations. Writing is achieved by applying an appropriate electric field to the ferroelectric material, and reading can be performed through three different methods, resulting in three different memory mechanisms,[123] namely the ferroelectric random access memory (FeRAM), the FeFET, and the ferroelectric tunnel junction. The ferroelectric material in FeRAM is polarized when a voltage is applied, and the polarized state is maintained when the voltage is stopped. Depending on the direction of the electric field, the lattice of the material is in two different stable states, which are used to indicate the "on" and "off" states, thus realizing non-volatile storage. Fe-FET is a ferroelectric transistor based on a conventional transistor with a ferroelectric placed in series with a conventional dielectric. The threshold voltage of the Fe-FET can be changed by changing the polarization state of the ferroelectric. The principle of FTJ is to use a thin film of ferroelectric material as a barrier layer, and to use polarization phenomena to modulate the tunneling barriers of the heterojunction, and hence the resistance. Changes in the applied voltage cause a strain in the lattice of the ferroelectric film in the FTJ, which in turn determines changes in the thickness of the barrier layer, and the FTJ requires a depolarizing field to ensure that the "on" and "off" states have different barrier heights. Studies have shown that reducing

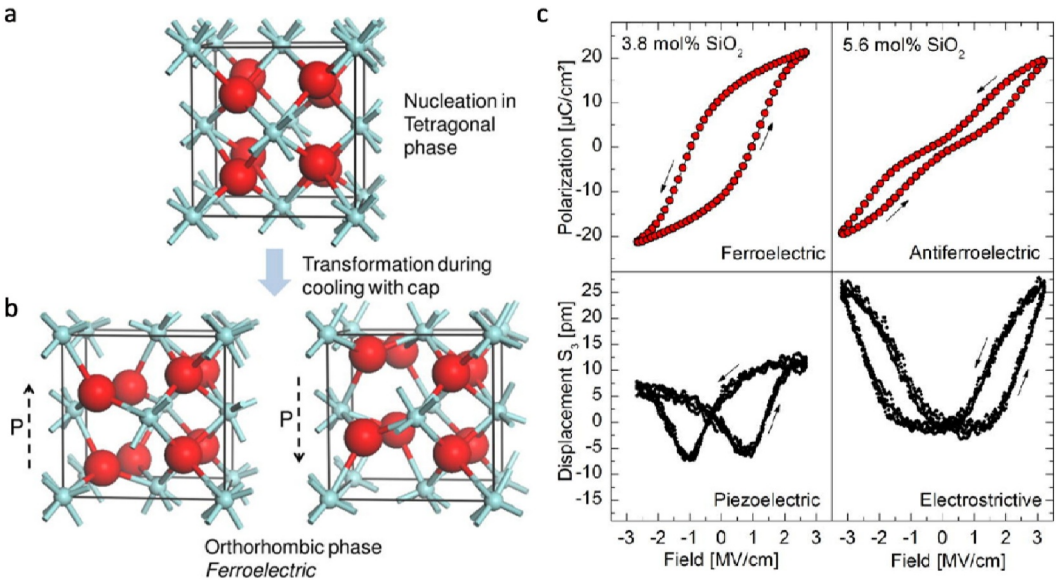


FIGURE 12 (A) The formation of the orthorhombic phase proceeds by transformation from the tetragonal phase during cooling with a cap. The bottom row indicates two different polarization states of the ferroelectric phase (Large atoms are oxygen and small atoms are hafnium.). (B) The formation of the orthorhombic phase proceeds by transformation from the tetragonal phase during cooling with a cap. The bottom row indicates two different polarization states of the ferroelectric phase (Large atoms are oxygen and small atoms are hafnium.). Reproduced with permission.[121] Copyright 2020, Wiley-VCH GmbH.

oxygen vacancy concentration and annealing temperature can significantly improve the endurance of doped HfO_2 films.[124]

All the three types of ferroelectric memory cells are a ferroelectric capacitor consisting of a ferroelectric layer sandwiched between two electrodes. However, depolarization fields generated by surface or interface regions in ferroelectric films can reduce the reliability of the ferroelectric material. In traditional perovskite ferroelectric materials,[125] strong depolarization fields prevent the retention of ferroelectricity in thin films, with the state-of-the-art technology node still at 130 nm.[126] Recent studies have shown that fluorite-structured HfO_2, zirconium dioxide (ZrO_2), and $HfZrO_2$ superlattices can maintain ferroelectricity at 0.5 nm (1 unit cell thickness),[127–129] which is important because traditional ferroelectric materials lose their ferroelectricity at very small sizes, and maintaining the ferroelectricity in the 0.5 nm range can satisfy the requirement of small sizing of ferroelectric devices, potentially avoiding the depolarization issues of perovskite ferroelectrics and providing strong device stability. Currently, HfO_2 and ZrO_2 are used as gate oxides in logic FETs and as dielectrics in DRAM capacitors. HfO_2 and ZrO_2 films can be deposited using atomic layer deposition (ALD), allowing precise thickness control. This precise control is critical for scaling down memory sizes and increasing memory density. Additionally, doping with transition metal elements such as Y and La can stabilize the ferroelectric phase of HfO_2.[130,131]

Despite the significant advantages of HfO_2 films in terms of ferroelectric performance, some reliability issues remain, such as the wake-up effect and endurance (ferroelectric fatigue). The wake-up effect refers to the phenomenon where the remnant polarization gradually increases with the number of electric field cycles. Once this stable state is reached, further cycling typically does not cause significant changes in polarization, and the material is considered to have "woken up" to its full ferroelectric potential. Previous research attributes the wake-up effect to the diffusion and redistribution of oxygen vacancies or charges within the thin film.[132] This phenomenon can affect the initial performance and long-term reliability of devices. The wake-up effect is significantly influenced by annealing temperature. Park et al. observed that higher annealing temperatures reduce the number of cycles needed to wake up $Hf_{0.5}Zr_{0.5}O_2$ films, resulting in increased remanent polarization.[133] Therefore, careful engineering is required when designing ferroelectric materials and devices to ensure they quickly achieve optimal performance and maintain it throughout their operational life. Endurance refers to the decline in a ferroelectric material's ability to undergo polarization switching with an applied electric field after many switching cycles. A common failure mechanism involves a hard breakdown occurring subsequent to a rise in leakage current, possibly due to the accumulation of oxygen vacancies at grain boundaries forming permanent conductive paths.[134] Endurance is a key

factor in determining the reliability and lifespan of ferroelectric devices such as FeRAM and FeFET. Studies have shown that reducing oxygen vacancy concentration and annealing temperature can significantly improve the endurance of doped HfO_2 films.[124]

To summarize, ferroelectric HfO_2 offers numerous advantages. They are compatible with Si and CMOS processes and can exhibit strong ferroelectricity at nanoscale thicknesses. Consequently, the films can be miniaturized to facilitate their incorporation into FeFET or FeRAM capacitor technologies, particularly effective for processes at the 20 nm technology node. Furthermore, thicknesses under 10 nm are beneficial for 3D capacitor configurations.[135] Other emerging directions, such as the realization of negative capacitance FETs,[136] are also being pursued. In conclusion, ferroelectric HfO_2 holds significant promise and offers intriguing opportunities within the field of memory technology. Its most prominent application is as a rapid, energy-efficient, cost-effective, and high-density alternative to traditional embedded flash memory. Additionally, these devices are well-suited to advance neuromorphic computing and memory-intensive applications, marking a progression beyond conventional CMOS integrated circuits.[120]

3.2.2 | ZrO_2

ZrO_2 is a high-k dielectric material with a theoretical dielectric constant of approximately 25, comparable to that of HfO_2, which is widely used in current technology. ZrO_2 has a bandgap of about 5.8 eV, providing excellent thermodynamic stability when in direct contact with silicon substrates. The high melting point and stability of amorphous ZrO_2 contribute to its robustness, and its high refractive index makes it suitable for optical applications as well.[137–140] Research on MOSFETs using ZrO_2 as the gate dielectric layer has demonstrated that its Weibull slope exhibits minimal dependence on both the capacitance area and the thickness of the ZrO_2 layer. The Weibull distribution is the theoretical basis for device reliability analysis and life testing, the dependence of the Weibull slope on the thickness of the ZrO_2 layer is very small, which is advantageous for scaling down the dimensions of MOS devices.[141]

3.2.2.1 | *Challenges*

However, the use of ZrO_2 as a gate dielectric also presents several challenges. Compared with traditional SiO_2, ZrO_2 has a lower crystallization temperature and forms a polycrystalline structure during the annealing process. Unlike single-crystalline structures with regular shapes and amorphous structures that are not at all periodic and symmetric, polycrystalline structures consist of many single crystals assembled in a haphazard way with multiple crystal planes, which greatly increases the leakage current.[142] The quality of ZrO_2 films can vary significantly depending on the preparation method, which somewhat limits the applicability of ZrO_2 as a dielectric material. Particularly in the case of amorphous ZrO_2, Different surface treatment methods can lead to variations in the crystal phase and structure, resulting in non-uniform film thicknesses that affect device performance.[143] Additionally, variations in deposition temperature and rate can impact the surface roughness of the ZrO_2 film, further influencing its properties. The interface performance between ZrO_2 and silicon substrates is notably inferior to that of SiO_2. HfO_2 has the same problem. This difference leads to increased Coulomb impurity scattering and surface optical phonon scattering, which results in a loss of carrier mobility and similarly restricts the application of ZrO_2 in gate dielectric layers.[144] To improve the reliability of ZrO_2, strategies such as doping with other elements and optimizing the deposition process are commonly employed.

3.2.2.2 | *Improvement in fabrication*

Currently, various traditional deposition methods, including sol-gel processes, ALD, molecular beam epitaxy (MBE), and CVD, have been employed for the fabrication of ZrO_2 thin films. However, the search for methods that can consistently produce high-quality, uniform ZrO_2 dielectric films continues.[145–148] ALD is one of the commonly used techniques for producing amorphous ZrO_2 films. Typically, $ZrCl_4$ and H_2O are used as precursors in this process, which can introduce hydrogen impurities. The development of hydrogen-free processes has effectively reduced the defect density in ZrO_2 films. For instance, a method using zirconium tetrachloride and ozone to produce $ZrCl_4$ has been reported.[149] Additionally, researchers have explored the use of highly volatile alkylamide zirconium precursors,[150] employing low-temperature ALD processes to produce high-quality ZrO_2 films, which further enhances the film quality. Physical vapor deposition techniques, including sputtering, are also commonly used for fabricating ZrO_2 films. This method can produce films with good quality and uniform thickness. To address the damage caused by plasma during sputtering and to improve film reliability, high-power impulse magnetron sputtering systems have been utilized for high-rate reactive deposition (140 nm/min).[151] Furthermore, substrate temperature has been reported to impact film quality; elevating the substrate temperature in an oxygen-rich environment can reduce leakage current density in ZrO_2 gate dielectric MOS devices.[152] Different from the above two methods, the advantages of solution method and sol gel method are low cost, which is very important in industrial production. ZrO_2 film prepared by improved spin coating process has been proved to have good reliability and electrical performance.[153] Figure 13A shows the transistor

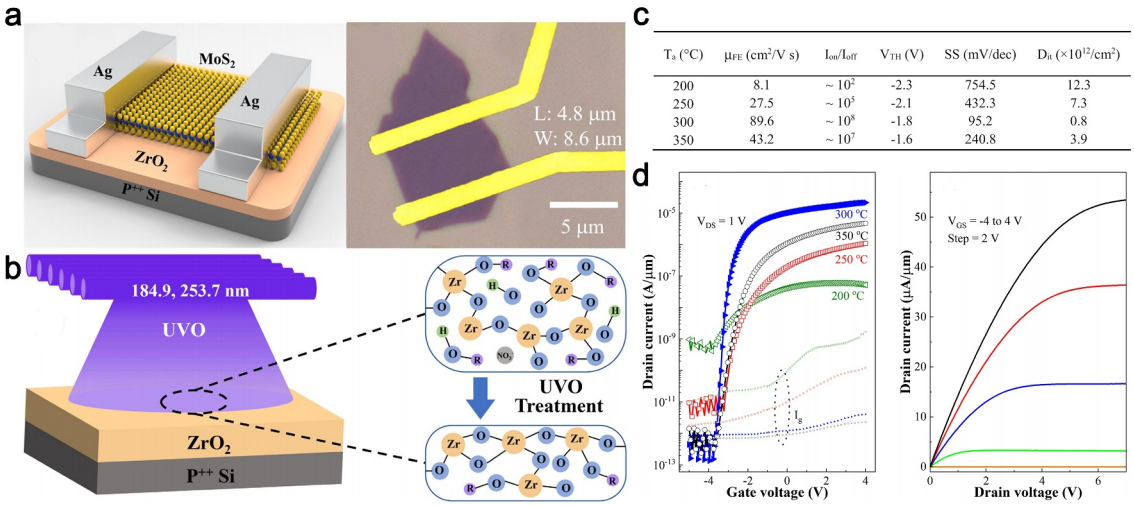


FIGURE 13 (A) Schematic of MoS_2 FET with ZrO_2 dielectric, and optical micrograph of exfoliated MoS_2 FET gated by ZrO_2 dielectric. (B) Scheme and mechanism of ultraviolet ozone-assisted treatment for ZrO_2 thin film. (C) Electrical parameters of MoS_2 FETs utilizing ZrO_2 dielectrics annealed at various temperatures. (D) Transfer curves of MoS_2 FETs based on ZrO_2 dielectrics (VDS = 1 V) and Output curves of MoS_2/ZrO_2-300 FET. Reproduced with permission.[154] Copyright 2024, IEEE. FET, field effect transistor.

structure constructed by ZrO_2 dielectric layer prepared by solution method using UVO auxiliary spin coating process, which can get the transistor with good reliability and electrical performance. It can be seen in Figure 13B that the UVO process can greatly eliminate organic groups in ZrO_2, Figures 13C,D show the best performance at 300°C annealing temperature, and the subthreshold swing (SS) value can be as low as 95.2 mV/dec, with good electrical performance.[154]

Doping with additional elements or incorporating other material layers can also enhance the electrical performance and reliability of ZrO_2 films. Stacked layers of ZrO_2/AlN and ZrO_2/aluminum oxide (Al_2O_3) have been shown to mitigate the issue of reduced charge carrier mobility caused by long-range scattering.[155,156] Additionally, nitrogen doping in the ZrO_2 gate dielectric layer has been demonstrated to effectively reduce the IL thickness and leakage current density.[157] It is noteworthy that crystalline ZrO_2, in its tetragonal and cubic phases, exhibits a higher dielectric constant (k value) compared to amorphous ZrO_2. At present, ultra-thin monoclinic ZrO_2 (m-ZrO_2) has been successfully prepared by in situ thermal oxidation ZrS_2 technology, and Figure 14A shows the FET by using m-ZrO_2 as gate dielectric.[158] As Figure 14B–D show, it has good electrical performance, with a dielectric constant of about 19. The mobility of the MoS_2 FET using m-ZrO_2 as the dielectric layer is comparable to that of FETs using SiO_2 as the gate dielectric, and thus crystalline ZrO_2 is also a very promising dielectric material.

It is worth to note that, due to the potential for significant leakage current in crystalline ZrO_2, its application in gate dielectric materials has been limited. To address this issue, efforts to improve the reliability of single-crystal ZrO_2 primarily focus on the insertion of buffer layers. Materials such as Al_2O_3, AlN, and Ge/ZrO_2/Y_2O_3 have been reported as effective buffer layers for crystalline ZrO_2 gate dielectrics.[159,160]

3.2.3 | Al_2O_3

Al_2O_3 is also commonly explored as a high-k dielectric material for gate oxides. Al_2O_3 possesses excellent thermal stability,[161,162] maintaining a good amorphous state even at temperatures exceeding 1000°C, which makes it well-suited to withstand the high-temperature annealing steps used in CMOS processing. Additionally, Al_2O_3 has a wide bandgap of approximately 8.8 eV, comparable to traditional insulating gate oxides like SiO_2. Furthermore, the interface between Al_2O_3 and crystalline silicon is stable with a low interface state density, ensuring good compatibility with channel materials.[163,164]

3.2.3.1 | Challenges

However, Al_2O_3 faces certain limitations when applied as a high-k dielectric material. Its dielectric constant, approximately 9, is relatively low compared to other high-k materials, making it only about 2.6 times that of SiO_2 and providing less advantage compared to HfO_2. Additionally, Al_2O_3 films typically carry fixed negative charges due to inherent defects within the material. These fixed charges can cause a slight positive shift in the flatband voltage of MOS devices with Al_2O_3 as the gate dielectric and may affect the mobility of charge carriers in the substrate through Coulomb scattering caused by these fixed charges.[102,165] Al_2O_3 is often

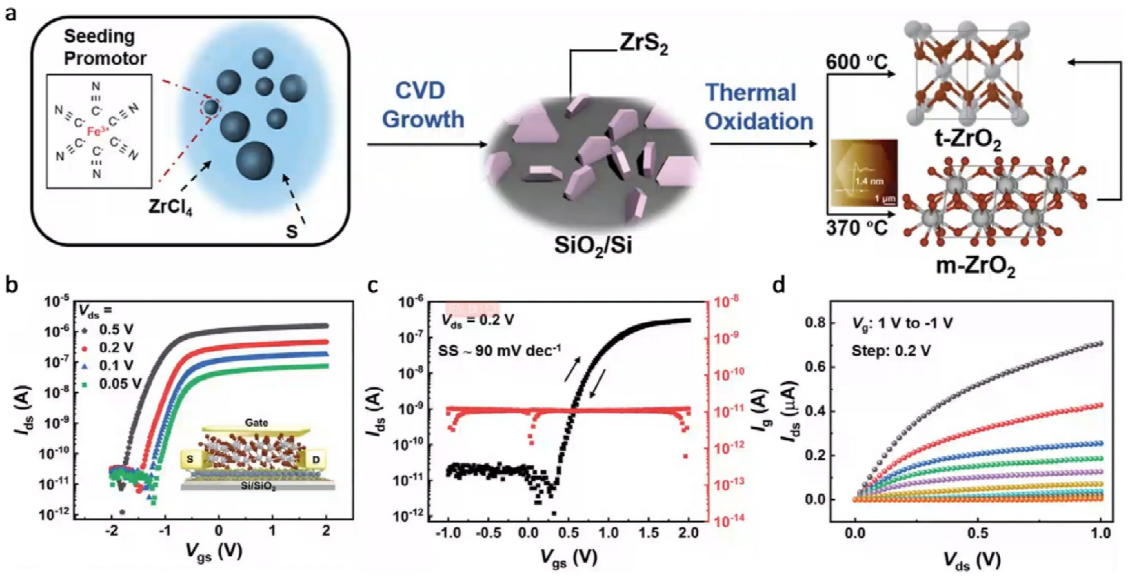


FIGURE 14 (A) Schematic diagram of ZrS_2 growth and thermal oxidation mechanism and preparation of ZrO_2. MoS_2 FET by using m-ZrO_2 as gate dielectric. (B) Transfer curve of MoS_2 FET under different V_{ds}. Inset, the device structure of MoS_2 FET with m-ZrO_2 as the top dielectric. (C) The I_{gs}–V_{gs} curve (black curve) at $V_{ds} = 0.2$ V, showing negligible hysteresis. The I_{gs}–V_{gs} curve (red curve) showing low leakage current. (D) Output curve of MoS_2 FET. Reproduced with permission.[158] Copyright 2023 Wiley-VCH GmbH. FET, field effect transistor.

used as a dielectric layer in SiC-based and GaN-based transistors. The presence of defects leads to inevitable charge trapping, and then gives birth to fixed negative charges in Al_2O_3, which introduces reliability issues in devices. Moreover, high-temperature annealing does not eliminate charge trapping sites within the Al_2O_3, indicating that the problem is not solely due to disorder, as seen in amorphous HfO_2.[166] Research has previously investigated defects in both crystalline and amorphous Al_2O_3. These defects primarily include naturally occurring oxygen vacancies and aluminum vacancies, as well as interstitial hydrogen and oxygen defects. As shown in Figure 15, among these, aluminum vacancies and interstitial oxygen defects are known to possess deep acceptor levels, lying more than 3 eV below the CBM of Al_2O_3. In contrast, interstitial hydrogen and oxygen vacancies are located within the bandgap of Al_2O_3, and defect states in the bandgap are occupied by electrons during electron injection.[167]

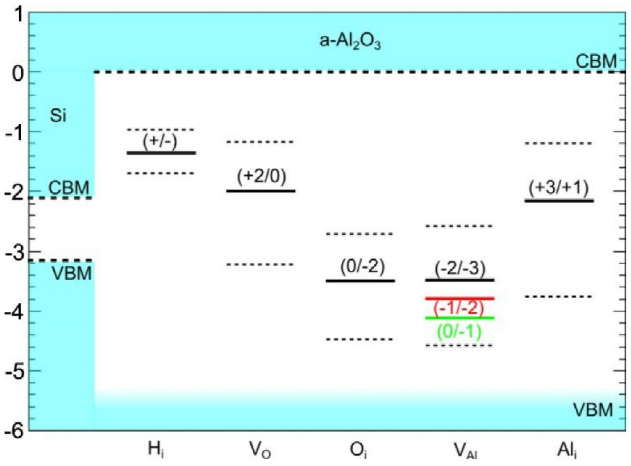


FIGURE 15 The average (solid lines) charge transition levels of H_i, V_O, O_i, V_{Al} and Al_i with respect to the a-Al_2O_3 conduction band minimum, the energy axis is in eV. The dashed lines represent the calculated range of the levels in the different samples. The Si/a-Al_2O_3 conduction band offset is taken from internal electron photoemission measurements. Reproduced with permission.[167] Copyright 2019, IOP Publishing Ltd.

3.2.3.2 | *Improvement strategy*

The preparation method of alumina films has been relatively mature. By using ALD technology, high quality Al_2O_3 films with amorphous structure, stable O/Al ratio and smooth surface structure without cracks can be obtained.[168,169] During the fabrication process, annealing temperature also significantly impacts the properties of Al_2O_3 films. Research indicates that annealing at 800°C can induce a phase transition from amorphous to crystalline Al_2O_3,[170,171] which affects the bandgap structure of the material. The variation of bandgap is mainly caused by the change of atomic structure, for example, from crystalline to amorphous or from one crystalline phase to another. Some defects in lattice will induce localized defect states and semi-localized band tail states, whose energy lies close to the band edge, and thereby changes the bandgap. Furthermore, first-principles calculations suggest that changes in bandgap may be associated with variations in the density of Al_2O_3 compounds and the average coordination number of aluminum atoms.[172]

Although the dielectric constant of Al_2O_3 is relatively low, its performance can be significantly improved when used as an interlayer within a SiO_2/HfO_2 dielectric stack, and it is commonly employed as a gate dielectric in GaN-insulated gate transistors.[173–175] In these applications, extensive interface engineering is necessary. Investigating and improving interface defects are crucial for enhancing the reliability of Al_2O_3 dielectrics. For instance, incorporating a 2 nm thick interfacial layer of SiO_2 or Al_2O_3 in HfO_2/4H-SiC MOS structures has been shown to simultaneously maintain transistor electrical performance and limit leakage current across the entire gate voltage range.[176] Additionally, the sequential selection of interface stacking will also lead to the change of gate dielectric layer properties. In Figure 16A, two stacked structures with different orders are shown. Figure 16B,C show that the $HfO_2/SiO_2/Al_2O_3$/4H-SiC structure is found to have a lower interface density and less fixed interface trap charge, lower device leakage current and more reliable-reliable than the $HfO_2/Al_2O_3/SiO_2$/4H-SiC structure.[177]

3.2.4 | La_2O_3 and TiO_2

La_2O_3 offers significant advantages due to its high dielectric constant of approximately 30, which is nearly 10 times that of SiO_2, thereby addressing the core requirement for introducing high-k materials.[178] Furthermore, La_2O_3 possesses a bandgap of up to 4.3 eV and an acceptable energy band offset with the silicon substrates.[179,180] However, La_2O_3 is susceptible to moisture absorption from the air, which imposes stringent application conditions and may lead to unacceptably high costs. Ongoing advancements in moisture mitigation measures are necessary for the practical use of La_2O_3.[181] La_2O_3 can be directly deposited on silicon substrates, but the high density of fixed positive charges in the dielectric layer may result in elevated surface states and significant flat band voltage shifts.[182] These interface issues can be mitigated by annealing, which can form La-silicate compounds at the interface and potentially improve the field-effect mobility of electrons in the dielectric layer, thus enhancing the performance of La_2O_3 as a gate dielectric.[183] The annealing temperature during the sol-gel process for La_2O_3 films has been shown to affect film quality; higher temperatures increase film density but can also lead to further atomic aggregation.[184] Low-temperature deposition techniques using oxygen-doped solutions have been demonstrated for large-area fabrication of La_2O_3 films.[185]

Additionally, in situ lanthanum dipole ALD methods and PDA in N_2 atmospheres have been reported to reduce interface defect density and leakage current.[186,187] La_2O_3 is also often used as an intercalation layer and stacked with other gate dielectric materials as a gate dielectric layer, such as inserting between Al_2O_3

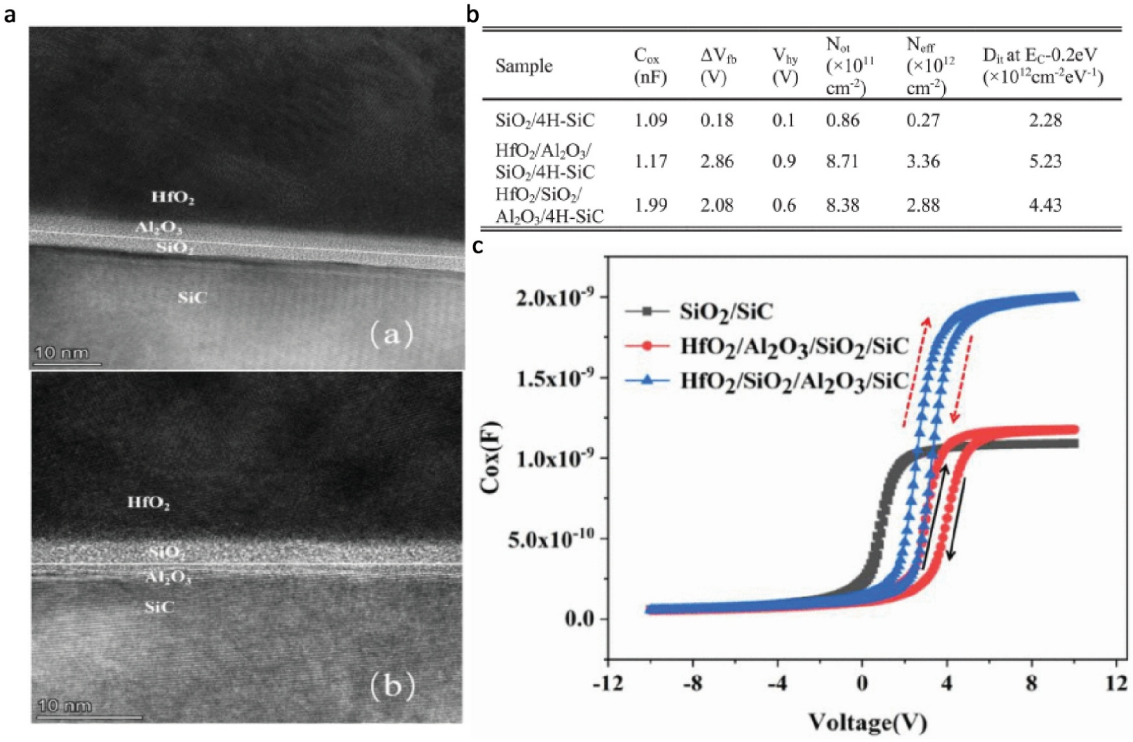


FIGURE 16 (A) TEM of $HfO_2/Al_2O_3/SiO_2$/4H-SiC and $HfO_2/SiO_2/Al_2O_3$/4H-SiC at 300°C annealing. (B) Parameters and (C) C–V curves of different stacked dielectric structures at 300°C annealing. Reproduced with permission.[177] Copyright 2023, IEEE.

and SiO_2 to form the dielectric layer of SiC power transistors.[188] The La_2O_3 and Al_2O_3 stacking structures have been applied to MoS_2 transistors, while it has been found to be converted to $LaAlO_3$ at high temperatures, resulting in a lower density of interface states and higher charge mobility.[187,189] Figure 17A shows the structure of $LaAlO_3$ as a gate medium transistor. Figure 17B clearly shows the current change caused by 650°C annealing. Correspondingly, Figure 17C can conclude that high $LaAlO_3$ conversion can effectively reduce the charge trapping in the gate medium. In thin-film transistors, La_2O_3 combined with polymer layers such as cross-linked polyvinyl alcohol has resulted in lower leakage current and defect density.[190] Moreover, doping La_2O_3 with elements such as Al, Ni, or Ti has been demonstrated to enhance device switching ratios, mobility, and other electrical properties.[189,191,192]

Titanium dioxide (TiO_2) has a high dielectric constant of up to 80, which could substantially address the issue of insufficient dielectric layer thickness in small-scale transistors. However, the application of TiO_2 in the fabrication of industrial transistors faces several challenges. One significant issue is the high density of oxygen vacancies in TiO_2, which can easily create leakage current pathways.[193] TiO_2 exists in two polymorphic forms: anatase and rutile.[194] Improper process control may lead to the formation of polycrystalline structures, which can increase leakage current. Furthermore, the interface quality between TiO_2 and the substrate remains a critical concern.[195]

To improve the reliability of TiO_2, layered structures have been employed. Stacking TiO_2 with materials that have lower dielectric constants and good electrical properties can effectively enhance the electrical characteristics and stability of the gate dielectric interface. Commonly used stack materials include SiO_2,[196] HfO_2,[197] Al_2O_3,[198,199] and Si_3N_4,[200] all of which have been shown to improve device performance. As shown in Figure 18A, some researchers prepared a transistor using TiO_2/Li-Al_2O_3 and a single layer Li-Al_2O_3 as gate dielectric respectively. Figure 18B shows the output characteristics of the two kinds of transistors, and the table in Figure 18C can be seen. The electrical properties (switching ratio, SS and so on) of TiO_2/Li-Al_2O_3 as gate medium are significantly better.[199] Moreover, improvements in fabrication process conditions can also enhance device reliability. For example, it has been observed that after annealing in a nitrogen environment, the trap-assisted leakage current conduction mechanism in devices is eliminated.[201]

4 | EMERGING GATE DIELECTRICS FOR 2D TRANSISTORS

2D semiconductors, such as MoS_2, WSe_2, and InSn[202–204] exhibit exceptional electrical and optical properties and can be stably maintained at atomic-scale thicknesses, making them ideal channel materials for compact, high-integration microelectronic

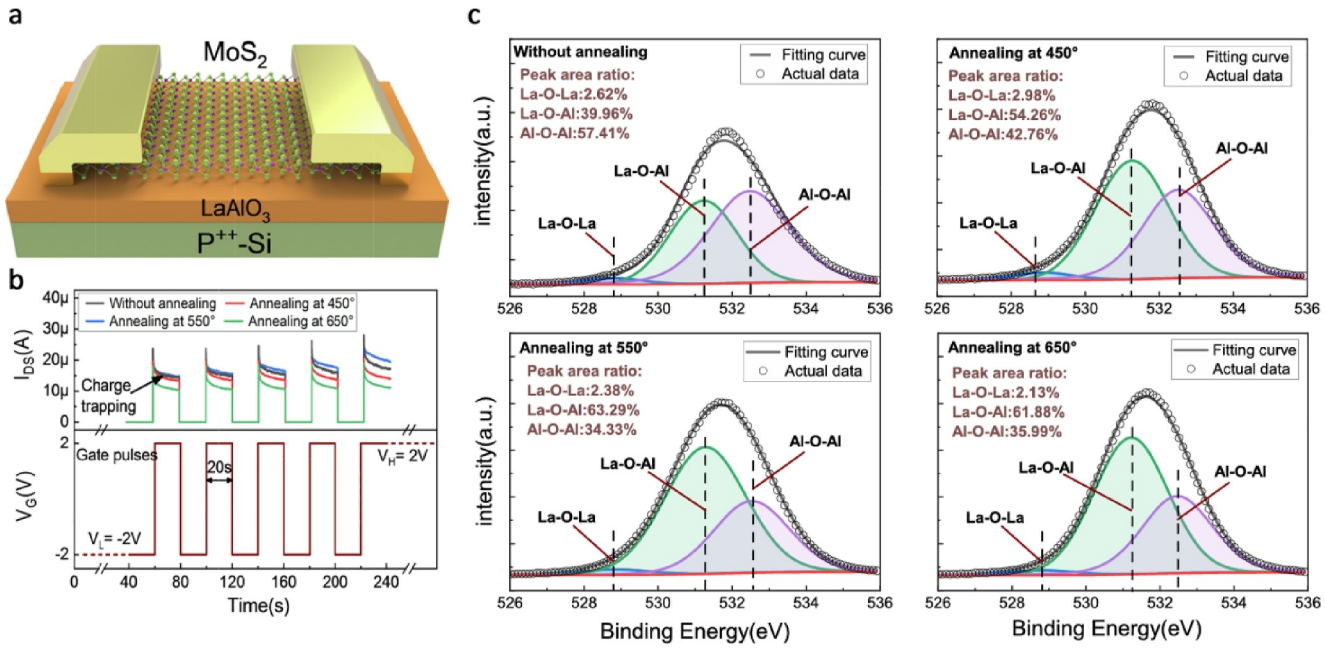
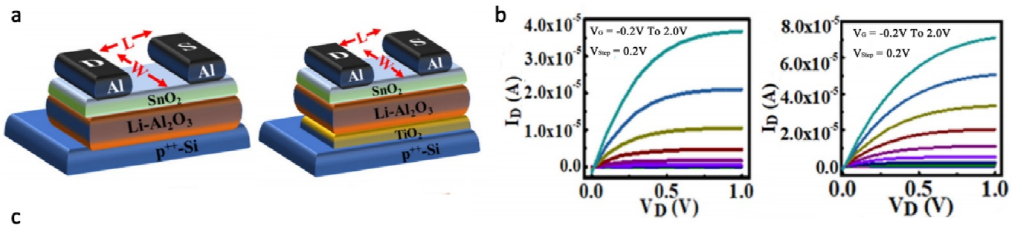


FIGURE 17 (A) The schematic diagram of La-based dielectric MoS_2 field effect transistor. (B) The drain current at applying ±2 V gate pulses with pulse width of 20 s. (C) O_{1s} peak fitted by three Gauss-Lorentz peaks, located at near 528.8, 531.2, 532.5 eV, corresponding to La-O-La, La-O-Al, and Al-O-Al bond respectively. Reproduced with permission.[189] Copyright 2021, IOP Publishing Ltd.



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Device	Threshold voltage (V)	I_{ON}/I_{OFF}	Subthreshold swing (mV decade^{-1})	Saturation mobility (cm^2V^{-1} s^{-1})	Saturation mobility with reliability factor (r_{lin}) (cm^2 V^{-1} s^{-1})	Interface trap-state density (cm^{-2})
Si^{++}/Li–Al_2O_3/SnO_2/Al	0.85	3.6×10^3	280	7.7	7.9 (2.7%↑)	1.6×10^{12}
Si^{++}/TiO_2/Li–Al_2O_3/SnO_2/	0.29	7.2×10^3	250	9.2	9.0 (3%↓)	1.1×10^{12}

FIGURE 18 (A) Schematic diagram of TFT devices. (Left) Device1 with single layer Li-Al_2O_3 gate dielectric, (right) device2 with bilayer TiO_2/Li-Al_2O_3 gate dielectric. (B) Output characteristics of (left) device1 and (right) device2. (C) Summary of the two devices of two different gate dielectrics. Reproduced with permission.[199] Copyright 2022, Pal et al., under exclusive license to Springer Science Business Media, LLC, part of Springer Nature. TFT, thin-film transistor.

devices.[205–208] Although the ideal 2D semiconductor is one with a smooth, defect-free surface, real experimentally prepared 2D materials are defective and have many defects on the surface of the gate dielectric, all of which can lead to reliability Issues such as the hysteresis and bias-temperature instabilities.[209–211] A major challenge lies in the interface quality between traditional dielectrics (e.g., SiO_2, Al_2O_3, HfO_2) and 2D semiconductors. Defects at the interface and within the dielectric can lead to BTI, stress-induced leakage currents, and premature dielectric breakdown.[212,213] To address these interface quality issues, the introduction of an interfacial layer between the traditional dielectric and the channel material has been proposed. h-BN is one of the most commonly used and recognized effective ILs,[214,215] and the HfO_2/Monolayer 3,4,9,10-perylenetetracarboxylic dianhydride/MoS_2 stack has also been shown to significantly reduce leakage current and breakdown time.[216] However, adding such interfacial layers can complicate the fabrication process. To simplify the process, dielectric materials that interact with the channel through van der Waals forces rather than chemical bonds, such as ionic fluorides, perovskites, and van der Waals insulators, are being employed in 2D semiconductor transistors.

4.1 | Fluorides

Recently, fluorides as gate dielectric have come to the spotlight, and are demonstrated to be more superior than traditional oxides.[217–219] These fluorides often have decent dielectric constant and enormous bandgaps. CaF_2, as the representative material, possesses a bandgap of approximately 12.1 eV, making it an excellent insulator with a dielectric constant of 8.43, but someone measured it to be 6.9.[220] The surface of crystalline calcium fluoride films terminates with F atoms, which can generate self-passivation effects without dangling bonds. This property enables CaF_2 to form quasi-van der Waals interfaces with 2D materials. Another important aspect is that CaF_2 is stable in air and does not easily dissolve, ensuring long-term performance stability when used as a gate material.[221–223]

CaF_2 has been widely applied in MoS_2 transistors and graphene transistors. Research indicates that CaF_2 films prepared by MBE exhibit high quality,[224] with leakage currents significantly lower than those of SiO_2.[225] MBE is a physical deposition method for thin film fabrication. CaF_2 has been successfully demonstrated to epitaxially grow on silicon, III-V semiconductors, and copper substrates to wafer-scale dimensions.[226–228] For the preparation of CaF_2, different crystal planes lead to different fabrication outcomes. The (111) surface of CaF_2, with relatively low free energy, has been proven to yield smoother films with better crystallinity.[229,230] The compatibility of the CaF_2 crystal plane with the substrate is also crucial. The crystal plane of CaF_2 varies with the growth temperature, causing fluctuations in the film thickness, which is a primary factor in increased leakage current in MOS devices when CaF_2 is used as a gate dielectric material. MBE growth of ultra-thin CaF_2 film (2 nm) has been successfully prepared, Figure 19A is the film surface morphology, and Figure 19B shows that the CaF_2 (111) surface and 2D material form a clear interface, while Figure 19C shows the MoS_2 device based on ultra-thin CaF_2 film, its subthreshold amplitude as low as 60 mV/dec, with application potential.[231] For MBE technology, the cleanliness of the substrate before CaF_2 growth affects the quality of the films. Cleaning the substrate with deionized water and hydrogen peroxide,[232] followed by annealing the samples under ultra-high vacuum,[220] have been proven to

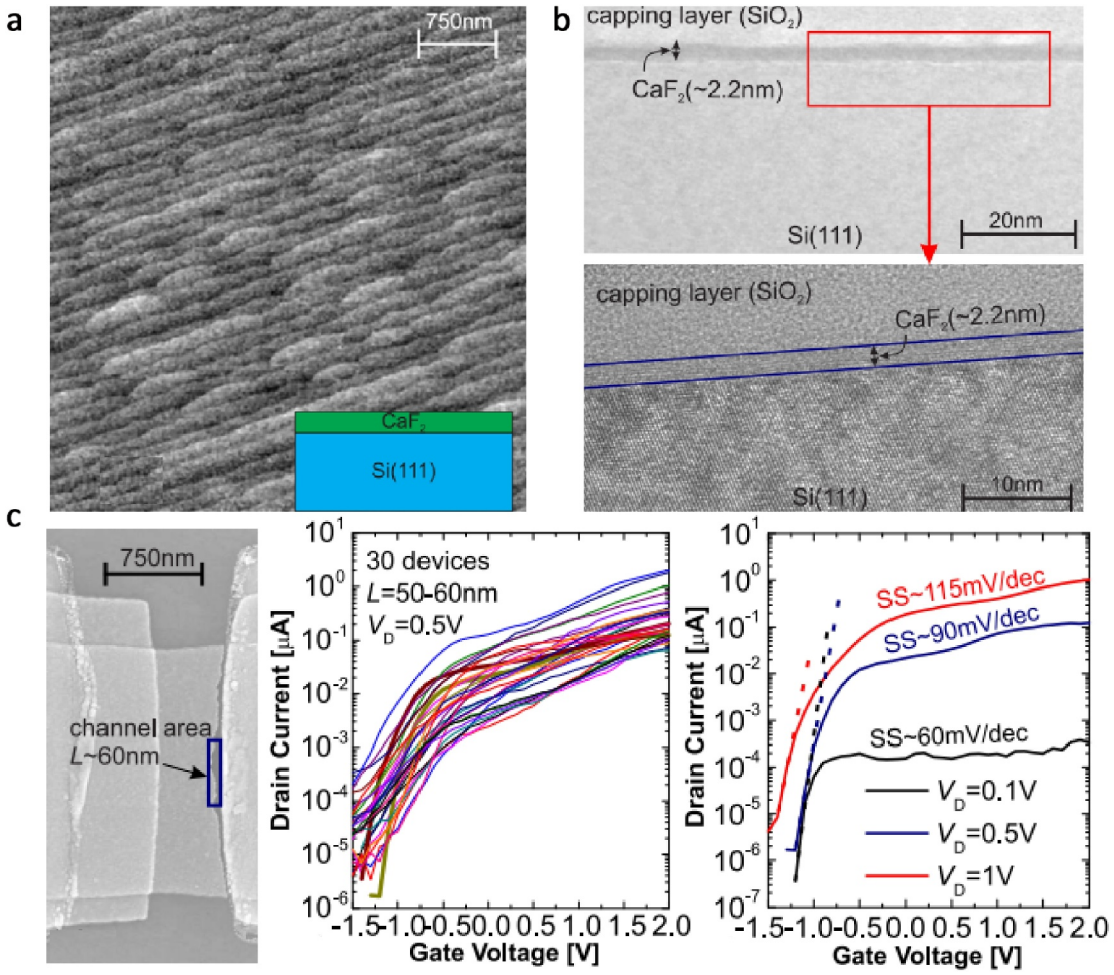


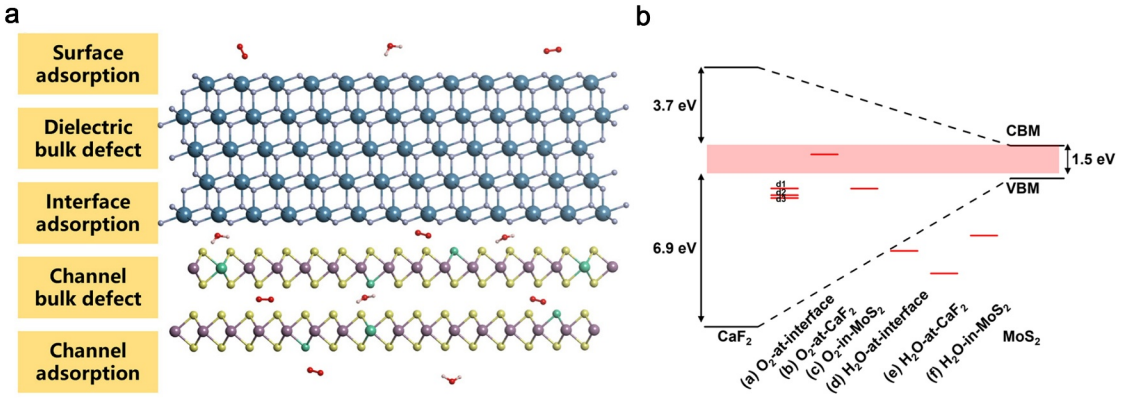
FIGURE 19 (A) Typical surface relief of our ultra-thin CaF_2 films grown by molecular beam epitaxy on Si(111) at 250°C. (B) Low (top) and high (bottom) resolution TEM images of the CaF_2 (2 nm)/Si(111) samples confirm the nominal thickness of CaF_2 of about 2 nm. (C) (Left) SEM image of our nanoscale CaF_2/MoS_2 FET, the channel length is about 60 nm. (Middle) I_D–V_G characteristics of 30 nanoscale CaF_2/MoS_2 FETs. (Right) The best device exhibits SS down to 60 mV/dec and an on/off current ratio up to 10^5. Reproduced with permission.[231] Copyright 2020, IEEE. FET, field effect transistor; TEM, transmission electron microscope.

further clean silicon substrates and improve the growth quality of CaF_2 films.

Despite the advantages over traditional oxides, the reliability issues cannot be completely eliminated, such as the signal hysteresis, which has been attributed to the boundary defects in CaF_2 and the thermally excited charge trapping.[233] Recently, the defects in CaF_2/MoS_2 and $CaF_2/MoSi_2N_4$ interfaces have been systematically studied.[234] Figure 20A shows the atomic structure of CaF_2-MoS_2 interface models with 5-layer CaF_2 and 2-layer MoS_2. In Figure 20B, it shows that the energy level distribution of different molecules (O_2, H_2O) absorbs on CaF_2 the surface and interface of CaF_2-MoS_2. Figure 20C shows the importance of different trapping centers in CaF_2-MoS_2. The research indicates that oxygen molecules adsorbed on the material interface or surface are highly active and unavoidable, even capable of spontaneously converting $MoSi_2N_4$ into a p-type semiconductor. Therefore, the study of vacuum encapsulation for CaF_2 transistors is deemed essential.

4.2 | Van der Waals insulator

In addition to CaF_2, Van der Waals insulators are also regarded as ideal dielectric materials. The Van der Waals insulators have very few dangling bonds on the surfaces, can be used as gate dielectric layers in 2D semiconductor devices to reduce the density of interfacial states, eliminate surface carrier scattering, and greatly improve carrier mobility.[235,236] One typical Van der Waals insulator is hexagonal boron nitride (hBN),



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Defect Types	Defect State	ΔE-VBM (eV)	ΔE-CBM (eV)	n-FET Importance	p-FET Importance	Fromation Energy (eV)	Overall Importance
V_S	d1	−0.38	−1.91	✓	✗	2.91	✓
	d2	0.95	−0.57	✓	✓		
V_{Mo}	d1	−0.06	−1.63	✓	✗	8.52	✓
	d2	0.40	−1.17	✗	✓		
	d3	0.71	−0.86	✗	✓		
V_{MoS3}	d1	−0.25	−1.78	✓	✗	11.81	✓
	d2	0.89	−0.64	✗	✓		
	d3	0.99	−0.53	✗	✓		
V_{MoS6}	type1	<0.50	>1.50	✓	✗	21.41	✗
	type2	<1.00	>1.00	✗	✗		
	type3	>1.75	<0.25	✗	✓		
O_2 at interface	d1	−0.99	−2.45	✓	✗	0.68	✓
	d2	−0.55	−2.00	✓	✗		
	d3	−0.85	−2.31	✓	✗		
H_2O at interface		−3.42	−4.91	✗	✗	0.61	✗
O_2 in MoS_2		−0.37	−2.01	✓	✗	2.35	✓
O_2 at surface		1.11	−0.41	✗	✓	2.25	✓

FIGURE 20 (A) Atomic structure of 5-layer CaF_2 and 2-layer MoS_2. (B) The energy level distribution of different molecules adsorbed on the surface and interface of CaF_2-MoS_2. (C) Importance of different trapping centers in CaF_2-MoS_2. Reproduced with permission.[234] Copyright 2024 by MDPI.

which has a layered hexagonal structure.[237] However, the application is limited by the low dielectric constant of hBN, which is about 3.3 for monolayer hBN.

Other materials such as single-layer MoO_3, WO_3, and V_2O_5 have been demonstrated to possess considerable potential for use in 2D material semiconductors.[238,239] Nevertheless, these oxides often contain oxygen vacancy defects, which can lead to current leakage.[240,241] To address this issue, alternative materials such as $MnAl_2S_4$, Sb_2O_3, and Bi_2SeO_5 have been reported to be well-suited for 2D semiconductor devices, exhibiting superior performance characteristics including high on/off ratios, high electron mobility, low hysteresis, and low SS.[242–244] However, the fabrication of van der Waals materials on a wafer scale and their integration with 2D semiconductors present significant challenges. The synthesis of these materials typically necessitates mechanical exfoliation or vapor deposition processes, which can compromise the quality of the films and interfaces, thereby affecting the reliability of transistors.[219,245–248] These challenges underscore the need for further research to develop effective solutions.

2D molecular crystals have always been commonly used in the field of organic electronics due to their tunable molecular structure, diverse and varied properties, and outstanding physical and chemical properties. Sb_2O_3 is currently a widely used van der Waals insulator. The first synthesis of 2D Sb_2O_3 without organic molecules was achieved in 2019 using a vapor-phase synthesis method assisted by passivators.[249] This marked a significant advancement, extending the research on 2D molecular crystals from the organic to the inorganic domain. Unlike traditional 2D materials such as graphene and black phosphorus, which exhibit in-plane strong chemical bonding and interlayer weak van der Waals interactions, 2D inorganic molecular crystals are structured with cage-like small molecules that lack dangling bonds. These molecules are bound by weak van der Waals forces in all three dimensions, which facilitates the formation of high-quality van der Waals interfaces between the 2D molecules and the

channels, thereby reducing reliability issues. Uniform deposition of Sb_2O_3 films on 4-inch wafers has been demonstrated using techniques such as precursor-based methods, liquid metal printing transfer, and thermal evaporation deposition.[250,251] The dielectric constant of Sb_2O_3 can reach up to 11.5,[244] and when stacked with MoS_2, the band edge offset is consistently greater than 1 eV. This substantial band offset mitigates interband tunneling when used as a gate dielectric material, thereby enhancing device reliability.

Sb_2O_3 is also often used as an intercalation material and stacked with other high-k materials such as HfO_2. Figure 21A shows the deposition process, Figure 21B,C are the schematic diagram and Atomic Force Microscope image of the device structure, the deposition of Sb_2O_3 on the surface of 2D semiconductors enables the formation of high-quality van der Waals interfaces. Furthermore, the high hydrophilicity of Sb_2O_3 promotes effective adsorption and deposition of precursors during ALD, resulting in the formation of high-quality HfO_2/Sb_2O_3 interfaces. The composite dielectric layer exhibits an EOT as low as 0.67 nm, representing the lowest EOT for current 2D transistor dielectric layers, and the SS of the constructed devices can be as low as 60 mV/decade, as shown in Figure 21D.[252] Sb_2O_3 is already a very promising material for applications, but there is still room to lower costs. More straightforward methods, such as spontaneous oxidation, could significantly expand the applicability of Sb_2O_3, providing a direction for future research.

Bi_2SeO_5 is also a van der Waals layered 2D material widely studied at present. The dielectric constant of Bi_2SeO_5 crystal film can reach 30, and the band gap is about 3.8 eV.[253] The research group of Peng at Peking University has developed a high mobility 2D semiconductor (Bi_2O_2Se) and its ultra-thin natural oxide gate medium Bi_2SeO_5.[253] The first theoretical calculation shows that the band gap of Bi_2SeO_5 increases, and it forms a typical type I heterojunction with Bi_2SeO_5. The band offsets of both conduction and valence bands are greater than 1 eV. The conduction band offset and valance band offset is 1.25 and 1.82 eV, respectively, which are both acceptable for field effect devices.[254] At present, bulk Bi_2SeO_5 single crystals have been shown to be prepared by chemical gas transport (CVT) method[255] and ALD method,[256] and ultra-thin Bi_2SeO_5 crystals grown by CVD have also been found to be easily transferred to other substrates by polymer-free mechanical pressing. This provides a guarantee for its use as an excellent gate dielectric layer for 2D semiconductors.[257] Single crystal transverse size up to centimeters. The interlayer binding force of Bi_2SeO_5 single crystal is special, which is stronger than vdW bonding but not as strong as typical covalent bonds. So the large area uniform and atomically flat nanosheets can be prepared by mechanical cleavage.

The minimum EOT of Bi_2O_2Se/Bi_2SeO_5 based devices can reach 0.9 nm, and the gate drain current is much lower than that of SiO_2 with the same EOT. The inverter (non-gate) CMOS logic circuit further built on

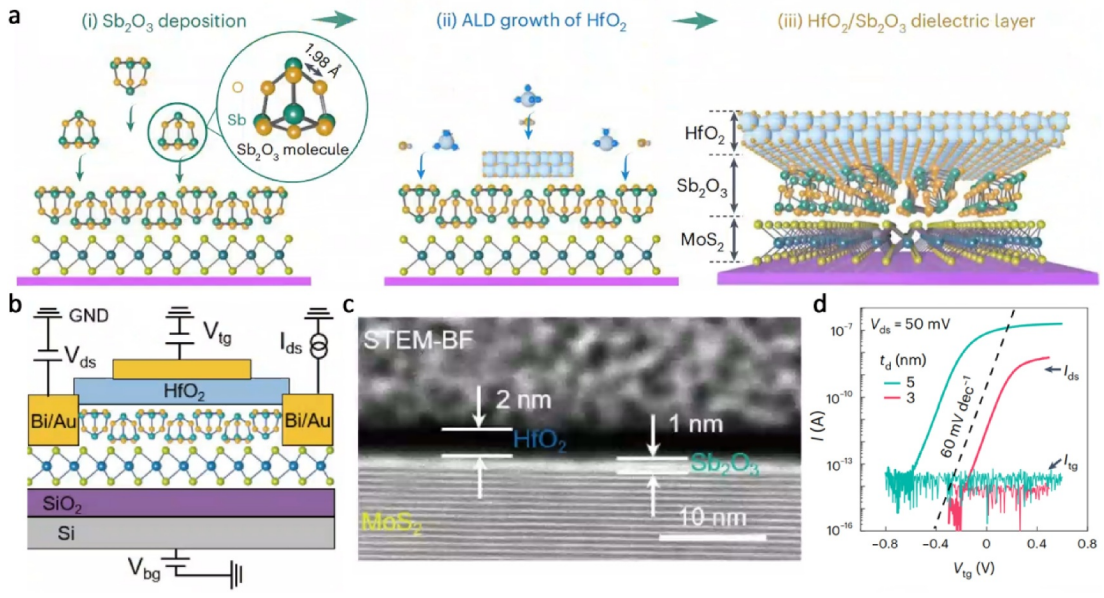

FIGURE 21 (A) Schematic illustration of the hybrid HfO_2/Sb_2O_3 dielectrics integrated on 2D MoS_2. (B) Schematic illustration of the FET structure with the hybrid Sb_2O_3/HfO_2 layer as the gate dielectric. (C) Bright-field (BF) cross-sectional STEM image of HfO_2/Sb_2O_3 on MoS_2. (D) Transfer characteristic curves of monolayer MoS_2 FETs with dielectric thickness t_d of 3 nm (red) and 5 nm (cyan). Reproduced with permission.[252] Copyright 2023, Y. Xu et al., under exclusive license to Springer Nature Limited. FET, field effect transistor; STEM, scanning transmission electron microscopy.

this basis has a maximum voltage gain of more than 150, which is much higher than that of other 2D material electronic devices reported as shown in Figure 22.[258] At the same time, the 2D Bi_2O_2Se/Bi_2SeO_5 is the first reported semiconductor and its natural oxide high κ-gate dielectric system, which not only has a high mobility 2D semiconductor channel, but also achieves an ultra-thin planar gate dielectric layer to suppress leakage current and other reliability problems. The electron mobility (μ) of device is up to 270 $cm^2\ V^{-1}\ s^{-1}$ Low-temperature quantum transport measurements show that the carrier mobility of the 2D semiconductor Bi_2O_2Se is significantly enhanced by the encapsulation of Bi_2SeO_5, with a low-temperature Hall mobility up to 470,000 cm^2/Vs.

Besides, epitaxial growth methods for wafer-level 2D semiconductor Bi_2O_2Se vertical fin arrays on an insulated substrate have also been reported, achieving epitaxial integration of 2D Bi_2O_2Se fins as channels/ with Bi_2SeO_5 heterostructures as high k self-oxides by using a controlled oxidation method. At the same time, the oxidation process of the 2D Bi_2O_2Se surface can be controlled layer by layer, and the thinness can reach 1 unit cell thickness (1.2 nm). Ultimately, atomically flat, lattice-matched high-quality semiconductor/dielectric layer interfaces can be formed. On this basis, high performance 2D FinFETs with channel thickness of about 6 nm (2D FinFET) were fabricated as shown in Figure 23.[253] The new 2D semiconductor channel/ epitaxial integrated high κ-gate dielectric-based 2D fin transistor meets the International Device and Systems Roadmap 2028 low power device target requirements in terms of mobility (270 $cm^2V^{-1}s^{-1}$), off-state current (1 pA/μm) and current switching ratio (10^8). Bi_2O_2Se/Bi_2SeO_5 2D fin transistors also show electronic advantages and potential compared with silicon, germanium and 2D transition metal sulfide (TMD) materials. The 2D Be_2SeO_5/Be_2O_2Se FinFET's mobility (270 cm^2/Vs), off-state current (1 pA/μm) and current switching ratio (10^8) meet the industry's requirements for high performance and low power devices, the on-state current is higher than that of commercial silicon, germanium and 2D TMD at the same channel length.

Bi_2O_2Se 2D single crystal with high dielectric properties can obtain strong gate control ability when applied to electrical devices. It has been reported that Bi_2O_2Se field-effect Hall devices packaged with Bi_2O_2Se 2D nanosheets with high mobility have been designed by using 2D material transfer technology. The low-temperature quantum transport measurement shows that after Bi_2SeO_5 packaging, the carrier mobility of 2D semiconductor Bi_2O_2Se is significantly improved, and the low-temperature Hall mobility is as high as 470,000 $cm^2V^{-1}s^{-1}$ (the highest mobility of Bi_2O_2Se system so far). The quantum Hall effect of Bi_2O_2Se was also observed for the first time. 2D single crystal dielectric material Bi_2SeO_5 can not only be used as an ideal packaging material and gate medium for 2D Bi_2O_2Se, but also for other 2D materials, such as MoS_2, graphene and so on.

4.3 | Perovskite

Perovskite materials also exhibit potential as dielectric materials, characterized by high dielectric constants and moderate band gaps, along with a wide variety of types and tunable band structures. Materials such as $SrTiO_3$, $Sr_2Nb_3O_{10}$ (SNO), and $BaTiO_3$ have been proposed as gate dielectrics for use in 2D transistors.[249,259–262] However, the application of perovskite materials as gate dielectrics is limited by issues

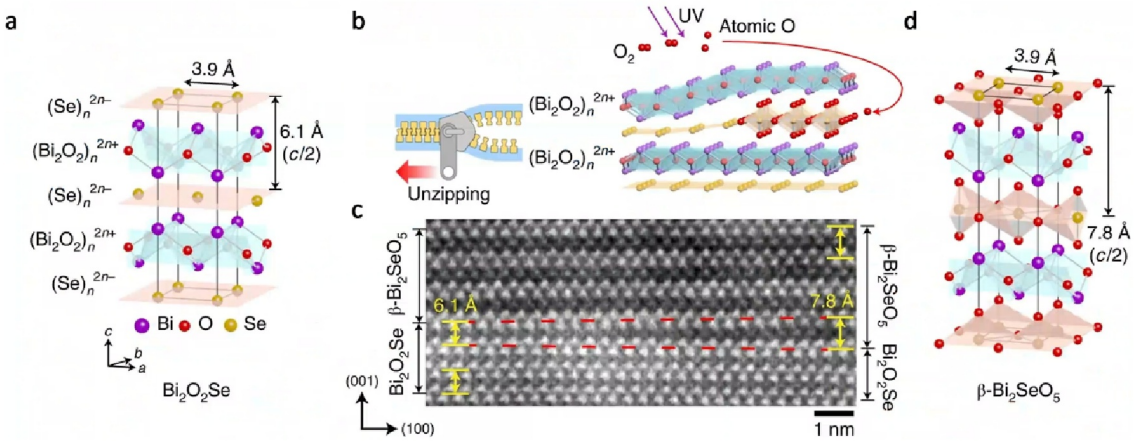

FIGURE 22 (A) Crystal structure of 2D Bi_2O_2Se with alternate $[Bi_2O_2]_n^{2n+}$ and $[Se]_n^{2n-}$ layers. (B) Schematic of the UV-assisted intercalative oxidation process, which preserves the $[Bi_2O_2]$ framework. (C) Cross-sectional STEM-HAADF image, showing the intercalative oxidation process at the interface. The single-crystalline $[Bi_2O_2]$ framework remains intact, whereas the interlayer spacing is enlarged. (D) Crystal structure of the intercalative oxide β-Bi_2SeO_5. Reproduced with permission.[258] Copyright 2020, Y. Zhang et al., under exclusive license to Springer Nature Limited. STEM, scanning transmission electron microscopy.

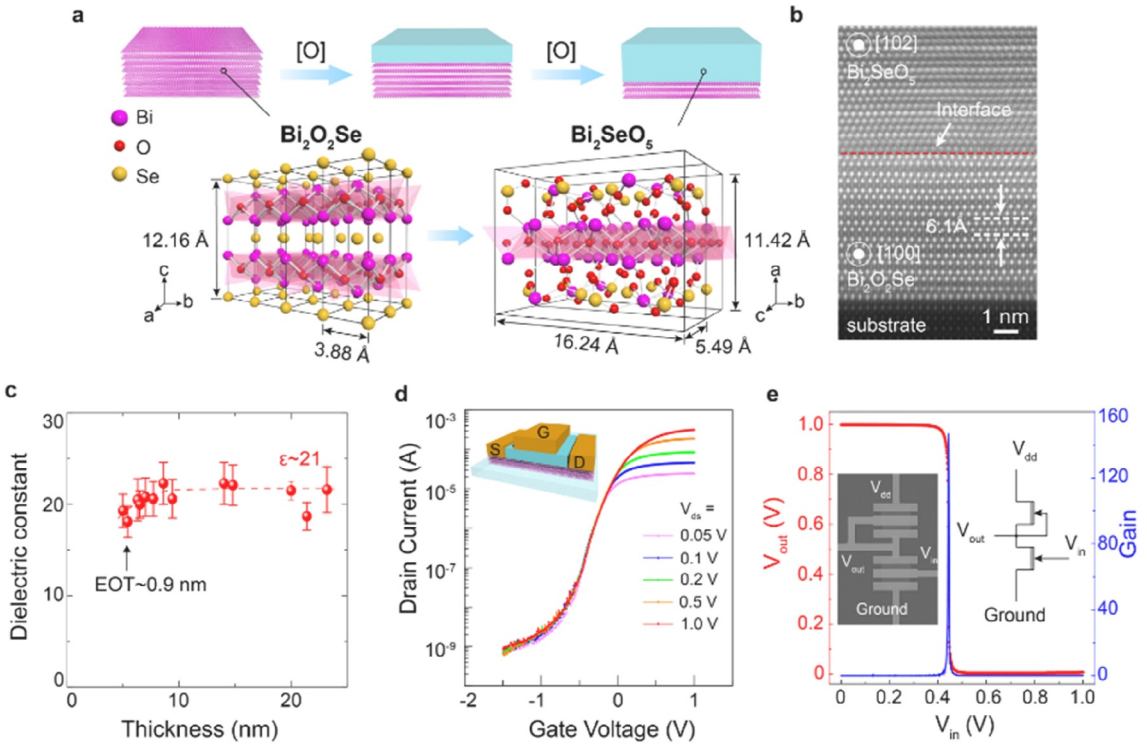

FIGURE 23 (A) Crystal structure of layered Bi_2O_2Se and its native oxide Bi_2SeO_5. Top: step-by-step oxidation of multilayer Bi_2O_2Se. (B) Cross-sectional high-angle annular dark-field image of the Bi_2O_2Se/Bi_2SeO_5 heterostructure, showing an atomically sharp interface. (C) Energy diagrams showing the band alignment between Bi_2O_2Se and Bi_2SeO_5. The band offsets are larger than 1 eV for both the conduction band minimum and VBM. (D) Density of states of Bi_2O_2Se and Bi_2SeO_5 near the gap. The inset illustrates the first Brillouin zone of both materials. Reproduced with permission.[253] Copyright 2020, T. Li et al., under exclusive license to Springer Nature Limited. VBM, valence band maximum.

related to their fabrication quality and integration with 2D semiconductors. Achieving high-quality dielectric layer/channel interfaces remains challenging. Additionally, perovskite materials as dielectric layers may exhibit channel current discrepancies and significant hysteresis, which are believed to arise from ionic migration.[249,263]

At present, it has been reported that 2D perovskite SNO nanosheets can be prepared by a layered precursor system[264] without the need for over-complicated epitaxial growth. The preparation process is shown in Figure 24A,B shows the high-resolution lattice image of the prepared SNO nanosheets after annealing at 600°C. Figure 24C shows that the SNO film annealed at 600°C has a low leakage current density of 3.5×10^{-8}A/cm^2 at 0.2 MV/cm, and the breakdown electric field increases by 0.25 MV/cm, showing good electrical properties. The successful application of this method proves the possibility of perovskite material as dielectric layer can be integrated with 2D semiconductor transfer.[265] Please note that 0.25 MV/cm is a very small electric field. Readers are suggested to contact the original author to verify the value.

The commonly used exfoliation process for layered perovskites involves preparing the perovskite material as a nanogel suspension, which is then exchanged with an acid to form a protonated form. This is subsequently replaced by tetrabutylammonium (TBA^+) ions in a chemical exfoliation process, resulting in negatively charged nanosheets.[223] Techniques such as Layer-By-Layer deposition,[212] Langmuir-Blodgett deposition,[266] and electrophoretic deposition have been employed to deposit these nanosheets onto substrates. Recently, an effective method for removing TBA^+ using a combination of ultraviolet and thermal treatment has been reported, which effectively addresses the issue of reduced dielectric constant in SNO nanosheet devices, thereby enhancing device performance. In addition, $SrTiO_3$ (STO) is also a commonly used chalcogenide dielectric layer with a high dielectric constant. At room temperature, the static dielectric constant of STO is about 200–300, which is nearly two orders of magnitude higher than that of SiO_2 (about 3.9). It has been reported that at low temperatures, the dielectric constant of STO can even increase to 5000–10,000.[267] In measurements of graphene devices, the effective dielectric constant of $SrTiO_3$ can reach between 17 and 20. In addition, the STO bandgap width of about 3.25 eV, is sufficient for the insulation of the gate oxide.

The integration of $SrTiO_3$ with 2D materials such as graphene has now been extensively investigated.[268,269]

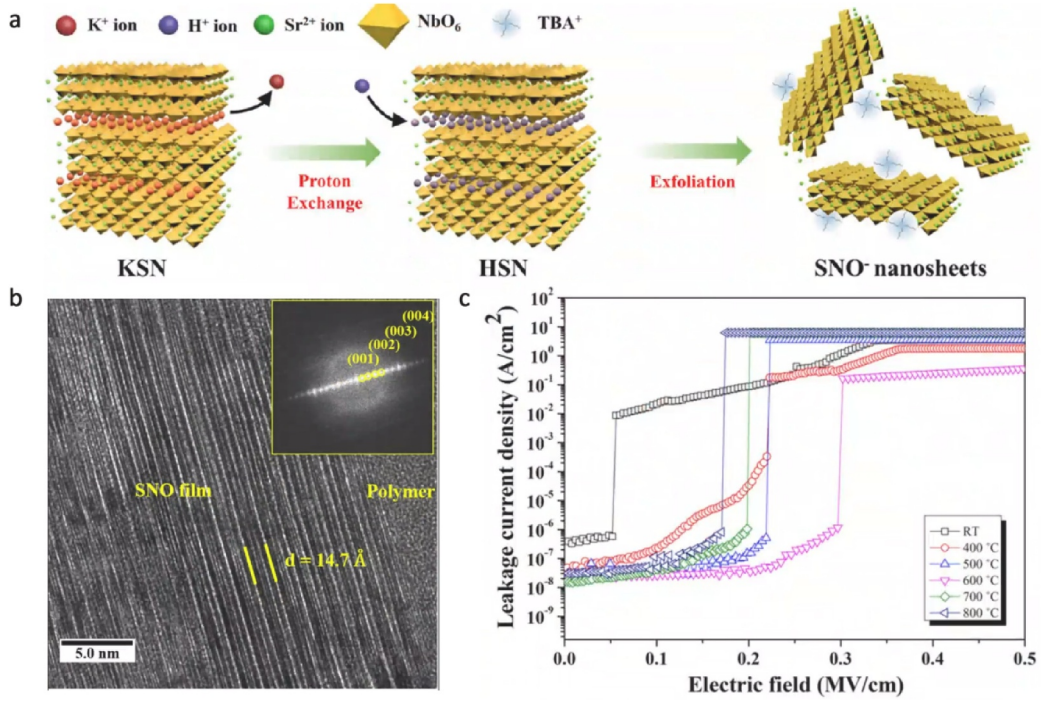

FIGURE 24 (A) Schematic diagrams of the protonic exchange and exfoliation processes. (B) High-resolution lattice image of the SNO film annealed at 600°C. (C) J–E curves of the SNO films grown at RT, and heated at various temperatures. Reproduced with permission.[265] Copyright 2016 The American Ceramic Society. RT, room temperature; SNO, $Sr_2Nb_3O_{10}$.

$SrTiO_3$'s high dielectric constant and the ability to form high-quality thin films make it an excellent candidate for 2D fet dielectric materials. However, the performance of 2D FET is highly dependent on the quality of the gate dielectric layer.

Defects in the material are one of the main reasons for the quality of the gate dielectric layer. Theoretical studies of intrinsic defects in STO have been reported.[270] The defect transition energy levels and recombination energies of four intrinsic defects in $SrTiO_3$: oxygen vacancy V_o, strontium vacancy V_{sr}, titanium vacancy V_{ri}, and titanium antipodal defect T_{is}, have been calculated by first principles, which can give some references for STO device simulations. The quality of the interface between the gate dielectric and the channel material similarly affects device reliability. Currently, STOs have been shown to bind to 2D semiconductors via van der Waals forces, and the van der Waals gap between strontium-titanium oxide dielectrics and 2D semiconductors has been shown to mitigate the unfavorable Foulin-induced barrier lowering effect that occurs with the use of ultrahigh-κ dielectrics. Currently, liquid-phase deposition, CVD, physical vapor deposition, sol-gel method and so on have all been reported to allow for the preparation of STO thin films.[88,271–273] In 2022, the reflection high-energy electron diffraction-assisted pulsed-laser-deposition technique is used to prepare freestanding $SrTiO_3$ dielectric layers, the $SrTiO_3$ film exhibit a desirable sub-one-nanometer capacitance equivalent thickness with a low leakage current (less than 10^{-2} A per square centimeter at 2.5 MV per centimeter). Short-channel transistor devices with $SrTiO_3$ film as the gate dielectric layer also exhibit excellent electrical characteristics, the SSs down to about 70 mV per decade and on/off current ratios up to 10^7.[261]

5 | CONCLUSION AND OUTLOOK

In summary, we have elucidated the advantages, reliability challenges, and improvement strategies of various gate dielectric materials. The application of high-k materials in traditional transistors has progressively matured, but one of the remaining challenges is dealing with the reliability issues that are predominantly caused by defects and their induced charge trapping and detrapping effects. Therefore, some missions are in urgent demand, including the precise experimental characterization of defects, the accurate calculation of charge trapping properties, and the exploration of ways to regulate defect activity. One atomic-accuracy tool for reliability simulation, named MARS, has been proposed by Liu et al. very recently.[274] Moreover, given the different advantages offered by each material, the stacking of multiple materials has become the preferred method for combining the benefits of each material. However, such multilayer stacks introduce corresponding interface issues, making the optimization of interface engineering, such as exploring passivation

methods for dangling bonds, critically important. Additionally, as transistor dimensions continue to shrink and dielectric layer thicknesses decrease, the optimization of thin film fabrication methods becomes essential. Improvements in annealing temperatures, atmospheric conditions, and related processes may significantly enhance film quality. It is worth mentioning that device reliability at cryogenic temperatures are attracting huge attentions. Wang and Liu et al. have revealed the dynamic variation of FinFETs at low temperatures, and more related studies are needed in the future.[275]

In the realm of gate dielectric layers for 2D semiconductor transistors, a plethora of new materials continues to emerge, and the exploration of materials with varying elemental compositions remains ongoing. However, the investigation into the reliability of these new materials is still far from comprehensive, particularly concerning their internal structures, defects, and electrical properties. Many of these aspects have yet to be fully explained, and thus further in-depth research is required. For materials that have already been identified as exhibiting promising performance, a more detailed investigation into their optimal fabrication methods and conditions is also necessary. This includes, in particular, efforts to reduce manufacturing costs, as the path toward the industrial application of new materials remains a considerable challenge. Hence, there is still a significant journey ahead to achieve practical and cost-effective integration of these materials into industrial processes.

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CONFLICT OF INTEREST STATEMENT

The authors declare no conflicts of interest.

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