Spiking Neurons with Neural Dynamics Implemented Using Stochastic Memristors

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Implementing and integrating spiking neurons for neuromorphic hardware realization conforming to spiking neural networks holds great promise in enabling efficient learning and decision-making. The spiking neurons, however, may lack the spiking dynamics to encode the dynamical information in complex real-world problems. Herein, using filamentary memristors from solution-processed hexagonal boron nitride, this study assembles leaky integrate-and-fire spiking neurons and, particularly, harnesses the common switching stochasticity feature in the memristors to allow key neural dynamics, including Poisson-like spiking and adaptation. The neurons, with the dynamics fitted via hardware-algorithm codesign, suggest a potential in realizing spike-based neuromorphic hardware capable of handling complex problems. Simulation of an autoencoder for anomaly detection of time-series real analog and digital data from physical systems is demonstrated, underscoring its promising prospect in applications, especially, at the edges with limited computational resources, for instance, auto-pilot, manufacturing, wearables, and Internet of things.

1. Introduction

Spiking neural networks (SNNs), inspired by information processing in biology, hold great promise for efficient learning and decision-making by enabling computing with sparse, asynchronous spatiotemporal spike signals.[1] The computing, however, can demand substantial computational resources for reliable results, posing challenges for the current von Neumann architecture.[2] Realizing neuromorphic hardware conforming to SNNs is an emerging strategy, where the input can be processed as spike signals in memory arrays in high parallelism.[3] Core to the hardware realization lies in implementing spiking neurons to integrate and transform the input into spike signals. Among the various neurons proposed, leaky integrate-and-fire (LIF) neurons (Figure 1a) are most recognized for the trade-off between the simplicity of the neuron design and the resemblance of the spiking to the action potential firing in biology[4] – the neuron outputs a spike as the potential is elevated over the threshold, and resets to the resting potential once discharged by the spike. Given this concise design and a facile integration potential with CMOS, LIF neurons are promising for practical computing chip realization, as foreseen by the Intel Loihi and IBM TrueNorth prototypes enabled with LIF silicon neurons.[5] Though promising, LIF neurons with well-deterministic spiking behavior can consume considerable computational resources and time to approximate the dynamical information in complex real-world problems.[2] This is problematic, especially for timely learning and decision-making where...
a delay can result in serious consequences.\cite{6} Achieving richer spiking dynamics in the current technological advances, however, requires more complex neuron models, such as Hodgkin-Huxley neurons, with more detailed operating instructions.\cite{7}

Memristors are electronic devices with readily switchable resistive states.\cite{8} Arising from the underlying switching mechanisms, for instance, conductive filaments, phase change, and Mott transition, memristors collate an inherent memory, allowing their exploitation in neuromorphic electronics and circuit development.\cite{9} Their simplified device configuration can also greatly facilitate large-scale, high-level, dense circuit integration.\cite{10} While the ongoing efforts are devoted to achieving non-volatile memristors with stabilized resistive states for biological synapse emulation toward neuromorphic computing, volatile memristors can be realized with self-reset threshold switching to fit the LIF neuron design while avoiding peripheral threshold and reset circuits for spike generation and resetting.\cite{9} Importantly, different from the well-deterministicity exhibited in the current LIF silicon neurons, memristors tend to show inherent stochasticity in switching arising from the underlying temporal switching dynamics, allowing them to naturally embody the bioplausible spiking dynamics in LIF neuron implementation.\cite{11} This stochastic feature has long been considered non-ideal, limiting the development of neuromorphic hardware, as mapping.

Figure 1. Self-reset threshold switching hBN memristors by inkjet printing. a) Schematic biological neuron and the LIF neuron model, with the spiking unit circled. $U_{th}$ and $U_{rest}$ are the spiking and resting potential, respectively. b) Schematic hBN memristor configuration, with the aggregated pellets representing the silver filaments. c) Cross-sectional scanning electron microscopic image of a typical device and d) the corresponding energy-dispersive X-ray spectroscopic elemental profiles along the dashed line, showing hBN sandwiched by the silver electrodes and no silver traces in the hBN layer after switching operations. A typical device area is $≈50 \mu m \times 50 \mu m$. Scale bar--1 $\mu m$. e) $I-V$ characteristics of 100 consecutive sweeping cycles at the positive voltage polarity, exhibiting self-reset threshold switching with switching stochasticity. The inset shows symmetric switching at positive and negative voltage polarities. The compliance current is 1 $\mu A$. The switching ratio is $>10^5$ at the compliance. The corresponding normalized cumulative probability functions (CDF) of f) the threshold ($V_{th}$) and hold voltages ($V_{hold}$), and g) the low (LRS) and high resistive states (HRS). The mean and standard deviation of $V_{th}$ are 0.96 and 0.16 V, respectively. The mean and standard deviation of $V_{hold}$ are 0.20 and 0.12 V, respectively. The mean and standard deviation of LRS are 1.34 and 0.44 M$\Omega$, respectively. The mean and standard deviation of HRS are 17.8 and 2.72 G$\Omega$, respectively. h) Ornstein–Uhlenbeck process modeling for the threshold voltage across 100 consecutive sweeping cycles. The experimental data points are well-fitted to those from an Ornstein–Uhlenbeck process, where the parameters $\theta$, $\mu$, and $\sigma$ are 0.55, 1.04, and 0.22, respectively.
algorithms to the hardware with stochasticity can cause faults in computation.\textsuperscript{[5]} Though considerable efforts are being paid to engineer the switching medium to address this stochastic non-ideal, an effective solution has thus far remained elusive.\textsuperscript{[12]} On the other hand, concurrently, the action potential in biology tends to fire with stochasticity in response to dynamical real-world stimuli.\textsuperscript{[17]} Considering the possible resemblance of the stochasticity in the memristors to that in biology, we propose that this stochasticity may be embraced and harnessed to lead to LIF neurons with richer spiking dynamics. This is expected to facilitate dynamical information encoding, critical for timely learning and decision-making.\textsuperscript{[11]} Indeed, the spiking neurons in SNNs are being designed with spiking stochasticity to form sparse networks, in order to endow the computing with fewer spikes and reduced power consumption, however, in higher efficiency and robustness.\textsuperscript{[6]}

Here, we assemble LIF neurons using filamentary memristors from solution-processed hexagonal boron nitride (hBN), and harness the switching stochasticity of the memristors to incur two key neural dynamics, including Poisson-like spiking and adaptation. The neurons with the dynamics fitted via hardware-algorithm codesign may enable spike-based neuromorphic hardware capable of handling complex problems. We demonstrate this by simulating an autoencoder for anomaly detection of timeseries real analog and digital data from physical systems, forecasting the potential in enabling efficient anomaly detection at the edges with limited computing sources.

2. Results

2.1. Scalable Stochastic hBN Memristors

We develop the memristors from liquid-phase exfoliated hBN (Figure S1, Supporting Information; see Experimental Section). As an insulating 2D material, hBN is well-suited to the design of metal-insulator-metal filamentary memristors,\textsuperscript{[13]} as schematically illustrated in Figure 1b. The filamentary behavior of the metal cations through the hBN layer governs the switching characteristic of the memristors. As such, different from the typical 2D material filamentary memristors where the interplay between the material defects and the filaments leads to non-volatile memristors for biological synapse emulation,\textsuperscript{[14]} we expect the dangling-bond-free nature of hBN can enable volatile memristors with self-reset threshold switching. As discussed, memristors with self-reset threshold switching can allow a convenient fit with the LIF neuron design while avoiding peripheral threshold and reset circuits for spike generation and resetting. Figure 1c presents the cross-sectional microscopic image of a typical hBN memristor, where the hBN layer and the top and bottom silver electrodes are all deposited by inkjet printing (see Experimental Section). See also Figure S2a,b (Supporting Information) for more device geometrical details. As shown in Figure 1e, the current output of a typical memristor indeed demonstrates self-reset threshold switching in full sweeping testing—its switches to a low resistive state at the threshold voltage as the silver ions diffuse and form conduction filaments and spontaneously resets to a high resistive state once the bias drops below the hold voltage. The self-reset is attributed to the interplay between the bias and the Joule heat,\textsuperscript{[15,16]} where the silver filaments maintain an equilibrium yet metastable state driven by the bias and the accompanying Joule heat. The dangling-bond-free nature of hBN accounts for the metastability of the silver filaments, as evidenced in Figure 1d where no trace of silver is observed among hBN after switching operations.

Notably, as shown in Figure 1e–g, stochastic variations are proven in the switching. The stochasticity is ascribed to the temporal dynamics of the diffusing silver ions when forming and rupturing the silver filaments.\textsuperscript{[17]} Here we evaluate the temporal dynamics via an Ornstein–Uhlenbeck process modeling. An Ornstein–Uhlenbeck process is a stochastic process with a mean-reverting behavior that describes the random fluctuations in a complex, dynamical system.\textsuperscript{[38]} Specifically, we model the measured threshold voltage ($V_{th}$) from the memristor as presented in Figure 1e. The variation in $V_{th}$ is approximated using a stochastic differential equation:\textsuperscript{[18]} $\Delta V_{th} = \theta (\mu - V_{th}) \Delta t + \Delta W$, where $\theta$ determines the magnitude of the mean reversion, $\mu$ represents the asymptotic mean, $\Delta t$ is the time step interval, $\sigma$ stands for the degree of randomness, and $\Delta W$ means the variation of a Wiener process. As demonstrated in Figure 1h, the measured threshold voltage data points are well-fitted to those from an Ornstein–Uhlenbeck process modeling, proving the stability of the switching stochasticity in prolonged switching operations. A stochastic yet stable switching will be critical in enabling spiking dynamics from the assembled neurons.

As spike-based neuromorphic hardware computes with spike signals, we carry out pulsed signal testing to study the transient response of our memristors besides the above full sweeping testing. Figure S2 (Supporting Information) presents the transient switching behavior of a typical memristor under pulsed voltage signals, where the device switches with a delay down to 30 ns and a relaxation down to 120 ns. We further conduct endurance-cycling testing to investigate the endurance of our memristors. We present in Figure S3 (Supporting Information) the 50 000-cycle endurance testing with 100 kHz pulsed voltage signals. As demonstrated, the pulsed signal testing proves a highly stable and robust switching behavior from the device, with the resistive states switched between the high and low resistive states following the pulsed signals with high stochasticity. A fast, stable, robust, and yet stochastic switching is critical for LIF neuron implementation toward spike-based neuromorphic hardware realization.

The scalability of the memristors is a major concern in realizing spike-based neuromorphic hardware. Leveraging solution processing and functional printing, the fabrication is highly scalable, as previewed in our wafer-scale all-inkjet-printing fabrication prototypes (Figure S3, Supporting Information). However, in the preliminary trials, the yield is <20% due to current leakages as a result of the inter-diffusion of the silver and hBN inks and the pinholes. Further work is needed to engineer the drying of the inks, the formation of the pinholes, and the device interfaces to improve the yield. Here we need to point out that the typical size of the memristors is $\approx 50 \times 50 \mu m$. This is limited by the patterning resolution of the inkjet printing technology.\textsuperscript{[19]} Though struggling to meet the miniaturization and integration requirements for the conventional microelectronics, the printed memristors with the low patterning resolution may enable promising neuromorphic electronics and applications in, for instance, plastic electronics, flexible electronics, and soft robotics.\textsuperscript{[19–23]}
To investigate the miniaturization of our memristors and also the integration possibility with CMOS, we adopt photolithography for memristor array patterning (Figure 2a). Specifically, as shown in Figure 2b, c (see also Figure S2c, d, Supporting Information), a layer of 10–20 nm SiO₂ is evaporated between the hBN layer and the top silver electrode to minimize the wash-off of hBN during the patterning processes and as such, increase the yield. Oxides such as SiOₓ and TiOₓ are widely used as the insulating medium in electrochemical metallization memristors, where the metal cations can diffuse through and form conductive filaments. [24–26] We expect that the silver ions after electrochemical metallization can first diffuse through the SiO₂ layer, and then diffuse in the hBN layer underneath upon memristor operation. As the silver filamentary behavior through the hBN layer essentially governs the switching, we expect the memristors can preserve the self-reset threshold, stochastic, and yet stable switching characteristics. Indeed, this is demonstrated in Figure 2f. Notably, this interface engineering leads to a yield of 100% (sampled with 20 randomly selected devices in the 12 × 12 device array).

Here we note that the typical size of the photolithographic patterned memristors is ≈20 μm × 20 μm, limited by our lab-based photolithographic system. Toward further miniaturization of the memristors, advanced photolithographic systems and alternative lithographic techniques may be used.

2.2. LIF Neurons with Spiking Dynamics

We connect a typical memristor to an RC circuit to assemble a LIF neuron. Circuit simulation and hardware testing are conducted in parallel to study the spiking behavior. Particularly, the circuit simulation serves as a control for spiking irregularity analyses as the switching stochasticity is not incorporated in the memristor modeling limited by the modeling platform. When in operation, the input as well as the time constant of the RC circuit govern the potential across the memristor and thus, the switching and reset of the memristor, that is, the spiking of the LIF neuron. As information in SNNs is contained in the presence of the spikes.
Figure 3. Spiking characteristics of the neurons. Spiking characteristics from the spiking neuron obtained from circuit simulation a) and hardware testing b) when fed with pulse trains of varying frequencies. In circuit simulation, the neuron exhibits a one-to-one spiking at low-frequency (≤ 1 kHz) pulse trains, and leaky integrate-and-fire characteristics at higher frequency (10 kHz–10 MHz) pulse trains. In hardware testing, the neuron exhibits a one-to-one spiking at low-frequency (≤ 1 kHz) pulse trains, and shows irregular spiking and even cut-off at higher frequency (10 kHz–10 MHz) pulse trains. The orange outputs represent the spiking. The black outputs represent the potential across the capacitor of the RC circuit. The input pulse frequencies are in blue for clarity. The duty cycle is fixed at 80%, and the time constant is fixed at 0.47 ms.

rather than their forms,[7] we study the spiking frequency from the neuron in response to the input frequency. Note that the input amplitude also well modulates the spiking (Figure S4, Supporting Information).

Figure 3 presents the input frequency-modulated spiking from the circuit simulation and hardware testing. When fed with a low-frequency pulse (e.g., ≤1 kHz), the neuron spikes correspondingly in both the circuit simulation and hardware testing. In this case, the RC circuit does not integrate the pulses as the pulse width is larger than the time constant of the RC circuit. The potential elevated during one pulse is larger than the threshold voltage of the memristor and thus, the neuron outputs one spike to one pulse. As the input increases to a high frequency (e.g., 10 kHz–10 MHz), the pulse width decreases below the time constant and thus, the RC circuit starts to integrate the pulses, leading to the leaky integrate-and-fire characteristic of LIF neurons.[27] Therefore, the spiking frequency in both the circuit simulation and hardware testing gets stabilized as the input frequency varies, as in this case the charging rate of the RC circuit remains invariant. However, interestingly, the neuron in the circuit simulation (Figure 3a) exhibits a tonic spiking at a saturated frequency, while the neuron in the hardware testing (Figure 3b) spikes irregularly by skipping certain pulses, with the spiking frequency dropping by three orders of magnitude to a frequency of ≤10 Hz. This spiking irregularity, common in biology, is termed adaptation to refers to a decaying neural activity in response to repeated, enhanced, and prolonged stimuli.[28] The spiking at 10 MHz input in the hardware testing even transits to negligible, similar to suprathreshold adaptation in biology.[29]

The hardware testing proves the irregular, adaptative spiking dynamics in our neuron resembling to that in biology. We ascribe these dynamics to the switching stochasticity of the memristor—the temporal dynamics of the diffusing silver ions cause the memristor not to be fully switched on or fully self-reset at the high-frequency input, leading to the irregular, adaptive spiking behavior with a reduced spiking frequency. A quantitative analysis of the spiking dynamics is discussed later in detail. In contrast, the simulated neuron presents ideal, well-deterministic spiking, as the switching stochasticity is not incorporated in memristor modeling. Besides the spiking dynamics, we note that our LIF neurons demonstrate a high data processing speed, allowing processing of 100 Hz to 10 MHz pulsed signals with the neuronal dynamics. As LIF neurons and the spike-based neuromorphic hardware aim to emulate how human brains process the
spiking neuron with the spiking dynamics. This is due to the hardware implementation with memristors and, especially, the hardware realized with our neurons using CV = \sigma(\Delta t)/\mu(\Delta t), where CV denotes the coefficient of variation that measures the standard deviation \sigma over the mean \mu of interspike interval. \cite{31} Here CV is estimated as 2.04, 1.08, 2.61, and 6.64 at 10, 100 kHz, 1, and 10 MHz input, respectively. Note that CV of a biological neuron with Poisson spiking is typically 1, and CV > 1 implies spiking bursting. Bursting, common in biology, refers to a dynamical state where a neuron outputs discrete groups of action potential spikes. \cite{7} Indeed, spiking bursting is observed in Figure 3b. The above analysis leads us to conclude that the spiking of our neurons approximates a Poisson process with bursting. In comparison, the probability density \( P(\Delta t) \) from the circuit simulation as presented in Figure S5 (Supporting Information) does not follow the Poisson process, and the CV \( \approx 0 \), showing that the simulated neuron gives an ideal, well-deterministic LIF neuron spiking behavior. In this context, we will thereby adopt the Poisson-like spiking process to the spike transmission in further spike-based neuromorphic computing.

Besides the irregular spiking, we also harness the spiking adaptation of our neurons in spike-based neuromorphic computing. For the convenience of understanding the adaptation, we plot in Figure 4b the relation between the spiking frequency and the input pulse frequency as we present in Figure 3. As discussed, practically mapping algorithms that assume no hardware non-idealities to the hardware realized with neurons can bring faults in computation. As shown in Figure 4b, as the spiking frequency of our neurons deviates from an ideal, well-deterministic spiking, here we introduce a dropout probability \( \beta \) to calibrate the spiking frequency (Figure 4c). Specifically, \( \beta \) is a function of the input frequency, \( i \), and is defined as the ratio of the spiking frequency in the hardware testing to that in the circuit simulation. A random dropout of the output spikes at certain timestamps with a dropout probability will generate mass zero outputs, thereby

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**Figure 4.** Hardware-algorithm codesign. a) Probability density histogram, and the corresponding exponential fittings, with respect to the interspike interval from the hardware testing at the spiking adaptation region, that is, 10 kHz–10 MHz frequency regions. The well-fitting to exponential functions suggests that the spiking follows a Poisson process, meaning the spiking is independent of one another. See Figure S5 (Supporting Information) for \( P(\Delta t) \) from the circuit simulation. b) The relation between the spiking frequency and the input pulse frequency of the neuron obtained from Figure 3, showing the adaptation region for the neurons. c) Mapping scheme to map the ideal, well-deterministic spiking in the circuit simulation to the practical spiking in the hardware testing, using the dropout probability \( \beta \). The blue and black lines schematically represent the input pulses and the membrane potential, respectively. The solid orange line schematically represents the ideal spiking. The dashed orange line schematically represents the practical spiking after dropout with a probability \( \beta \).
improving the network sparsity. The improved network sparsity can cut unnecessary memory access and computing operations.\cite{32} Therefore, the introduction of the dropout probability not only addresses the hardware non-ideality but also satisfies the network target in SNNs. The subsequent network will then be trained with the dropout probability, that is, the consideration of the spiking adaptation, such that a hardware-friendly algorithm can be designed to implement spike-based neuromorphic computing.

2.4. Spike-Based Neuromorphic Computing

The SNNs as a framework computing with spatiotemporal spikes are well-suited to handle time-series tasks, such as temporal pattern recognition, action localization, and anomaly detection.\cite{6} Amongst them, anomaly detection to identify and locate deviations from the baseline is considered a powerful technique for early detection of anomalies and thus, timely prevention of major problems. However, as discussed, SNNs can demand substantial computation resources for deployment. Realizing spike-based neuromorphic hardware with the dynamics capable of handling complex problems, therefore, is promising for anomaly detection, especially, at the edges with limited computation resources.

As a demonstration, we fit our neurons in the simulation of an autoencoder for anomaly detection (Figure S6, Supporting Information). Particularly, we perform anomaly detection testing of a public dataset consisting of time-series real spacecraft telemetry data collected from the Curiosity rover on Mars. Figure 5a illustrates the overall working principle of the autoencoder. Briefly, the spacecraft telemetry data as the input is rate-coded into spike trains, weighted, and then integrated by the spiking neurons for spiking to perform anomaly detection. To accommodate this workflow, as shown in Figure 5b, each layer of the autoencoder is designed as crossbars of artificial synapses and spiking neurons, where the synapses are non-volatile memories with reconfigurable weights. Figure 5c illustrates the corresponding 3-layer network topology with an encoder for compressing the input, a code for storing the compressed features, and a decoder for reconstructing the information from the code. This encoder-decoder, that is, the autoencoder, learns the compressed features and identifies anomalies based on the reconstruction errors.\cite{33} The spiking dynamics of our neurons are fitted via the above hardware-algorithm codesign and incorporated into the network: the Poisson-like spiking is adopted in the spike transmission, while the adaptation is used to improve the network sparsity.

To perform anomaly detection, we adopt semi-supervised learning of the time-series real spacecraft telemetry data. As the anomalies usually occur within a time span rather than at a specific timestamp, we set a time window to group the raw...
event-based data into frame-based ones for the convenience of spike-based neuromorphic computing. Figure 5d presents the raw telemetry data and the detected anomalies in time series, as well as the label and accuracy. Specifically, the label represents the actual anomalies labeled in the dataset to determine the detection accuracy. The accuracy thus represents the accuracy of the anomalies detected by the anomaly detection with respect to the anomalies labeled. As demonstrated, the simulation performs a successful anomaly detection, with an accuracy of 75% with only 20 training epochs. It is foreseeable that adopting variational and convolutional autoencoders with hyperparameter optimization can improve the performance. This, however, is outside the scope of this work on spiking neuron implementation. Nevertheless, the computationally efficient autoencoder for anomaly detection of complex analog and digital data proves the potential of employing our neurons in realizing spike-based neuromorphic hardware.

3. Conclusion

In this work, we have implemented spiking neurons with neural dynamics using solution-processed hBN filamentary memristors. The fabrication of the memristors is highly scalable and facile and, via interface engineering, statistically demonstrates a yield of 100%. Integrated into RC circuits, the memristors allow for simplified LIF neuron assembling and, intriguingly, enable two types of key neural dynamics by harnessing their common stochastic switching feature, including Poisson-like spiking and adaptation. We fit these dynamics via a hardware-algorithm code-sign to fill the possible gaps when mapping algorithms to the hardware realized with our neurons, ensuring fault-tolerant computation. Given the scalability of the memristors, the simplicity of the neuron design, and the spiking dynamics, our neurons suggest a potential in realizing spike-based neuromorphic hardware for dealing with complex problems. We envisage, once large scales of hardware with high levels of circuit integration are possible through collative efforts, a promising prospect of the spike-based neuromorphic hardware in implementing timely learning and decision-making, especially at the edges, for instance, the anomaly detection demonstrated in this work. Beyond spike neurons and the spike-based neuromorphic hardware, we expect our method of exploiting and fitting the common stochastic non-ideality in memristors can readily lend itself to other memristor-based neuromorphic electronics and hardware development.

4. Experimental Section

Solution-Processed hBN Memristors: hBN powder and all chemicals including the silver ink were purchased from Sigma–Aldrich and used as received. Liquid-phase exfoliation, ink formulation, and printing/coating of hBN followed the method previously reported in. The liquid-phase exfoliation workflow, as well as the X-ray diffraction, Raman scattering, absorption spectroscopy, and transmission electron microscope images of the hBN samples, are shown in Figure S1 (Supporting Information). In the inkjet-printing device fabrication process, the memristor was fabricated in a vertical structure of silver/hBN/silver, where hBN and the silver electrodes were all deposited by inkjet printing. A typical device area was ≈50 µm × 50 µm. A preliminary wafer-scale fully-inkjet-printing fabrication integrating 100 × 100 memristor devices is shown in Figure S3 (Supporting Information). The fabrication yield was <20%. In the photolithographic device fabrication process, the memristor was fabricated in a vertical structure of silver/SiO2/hBN/silver, where hBN was deposited by inkjet printing, the silver electrodes were deposited by electron-beam evaporation, and the thin layer (≈10–20 nm) of SiO2 was deposited via electron-beam evaporation between hBN and the top electrode. A typical device area was ≈20 µm × 20 µm. The device substrates used can be Si/SiO2, glass, and plastics such as Kapton, etc. The inkjet printer was Fujifilm Dimatix Printer DMP-2850. The evaporator was IKS EB-600. During device fabrication, the hBN layer after deposition was baked at 200 °C for 2 h, and the silver electrodes after deposition by inkjet printing were baked at 130 °C for 30 min for annealing.

Electrical Characterizations: Tektronix Keithley 4200-SCS parameter analyzer was used to measure the electrical characteristics of the memristor with direct-current signal. For the memristor transient response testing and the spiking neuron spiking testing, Siglent arbitrary waveform generator and Agilent digital storage oscilloscope were used to generate the pulsed signal and measure the output waveforms, respectively. In the spiking frequency testing, as the capacitor potential was not constant but oscillated with the input voltage, the center potential V\textsubscript{centre} = V\textsubscript{th} × duty cycle was considered to represent the capacitor potential when fully charged. An appropriate center potential ensures the memristor was triggered for spiking at varying frequencies. The input frequency was regulated by adjusting the pulse width while keeping both V\textsubscript{th} and duty cycle fixed, to ensure that the frequency was the only variable and that the central potential was always sufficiently larger than the threshold voltage of the memristor. Specifically, the duty cycle is fixed at 80% and the time constant was fixed at 0.47 ms.

Memristor Modeling: The memristor is modeled by Verilog-A and then connected to an RC circuit in Cadence Virtuoso for circuit simulation. The Verilog-A model was originally designed for memory switching devices and modified to adapt the self-reset threshold switching device, following:

\[
V(p,n) = I(p,n) \times \left( R_{on} \left( \frac{x}{D} \right) + R_{off} \left( 1 - \frac{x}{D} \right) \right)
\]

\[
x = x_{last} + \Delta x
\]

\[
\begin{align*}
\Delta x_{dk} &= K_{on} \times [V(p,n) - V_{th}] \quad \text{when} \ V(p,n) > V_{th} \\
\Delta x_{dk} &= K_{off} \times [V(p,n) - V_{hold}] \quad \text{when} \ V(p,n) < V_{th}
\end{align*}
\]

where V(p,n) is the voltage across the memristor, I(p,n) is the current, R\textsubscript{on} and R\textsubscript{off} are the low and high resistive states, x is the current resistive state, and D is the resistive state change range. Transient simulation is carried out at discrete simulation points with fixed step intervals, where \(\Delta x\) is the state change at each point, \(x_{last}\) is the x state at the previous point, and x is the updated state based on \(x_{last}\) and \(\Delta x\). \(\Delta x\) increases when V(p,n) exceeds V\textsubscript{th} until x reaches D, and \(\Delta x\) decreases when V(p,n) is below V\textsubscript{hold} until x reaches 0. K\textsubscript{on} and K\textsubscript{off} are the switching coefficients for the on and off states. See Figure S7 (Supporting Information) for the memristor electrical characteristics from the modified Verilog-A model.

Neuromorphic Hardware Simulation: The simulation was carried out in Python 3 and based on the snnTorch framework. The public dataset for anomaly detection was from the National Aeronautics and Space Administration (NASA) Mars Science Laboratory (MSL) (available at https://github.com/NetManAIOps/OmniAnomaly). The dataset consists of real spacecraft telemetry data and anomalies from the Curiosity rover on Mars. Part of, for example, 40%, the 132,046 data points in the dataset was used for training to learn the feature space and the rest for testing.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

G.H.H. acknowledges support from RGC (24200521) and SHIAE (RNE-p3-21). YL from SHIAE (RNE-p3-21), JFP and YYW from RGC (24200521),
and LWTN from NTU (start-up grant). The authors thank the snnTorch group at the University of Michigan for the snnTorch package, and NASA Mars Science Laboratory for the public dataset.

**Conflict of Interest**
The authors declare no conflict of interest.

**Data Availability Statement**
The data that support the findings of this study are available from the corresponding author upon reasonable request.

**Keywords**
novel spiking dynamics, self-reset threshold switching memristors, spike-based neuromorphic computing, spiking neurons, switching stochasticity

Received: August 22, 2023
Revised: September 21, 2023
Published online: