Effects of post-deposition vacuum annealing on film characteristics of p-type Cu_2O and its impact on thin film transistor characteristics

Sanggil Han, Kham. M. Niang, Girish Rughoobur, and Andrew J. Flewitt[a)]

Electrical Engineering Division, Cambridge University, 9 JJ Thomson Avenue, Cambridge, CB3 0FA, United Kingdom

Annealing of cuprous oxide (Cu_2O) thin films in vacuum without phase conversion for subsequent inclusion as the channel layer in p-type thin film transistors (TFTs) has been demonstrated. This is based on a systematic study of vacuum annealing effects on sputtered p-type Cu_2O as well as the performance of TFTs on the basis of the crystallographic, optical, and electrical characteristics. It was previously believed that high-temperature annealing of Cu_2O thin films would lead to phase conversion. In this work, it was observed that an increase in vacuum annealing temperature leads to an improvement in film crystallinity and a reduction in band tail states based on X-ray diffraction patterns and a reduction in the Urbach tail respectively. This gave rise to a considerable increase in Hall mobility from 0.14 $cm^2/V{\cdot}s$ of an as-deposited film to 28 $cm^2/V{\cdot}s$. It was also observed that intrinsic carrier density reduces significantly from 1.8×10^{16} to 1.7×10^{13} cm^{-3} as annealing temperature increases. It was found that the TFT performance enhanced significantly, resulting from the improvement in film quality of the Cu_2O active layer: enhancement in the field-effect mobility and the on/off current ratio, and a reduction in the off-state current. Finally, bottom-gate staggered p-type TFTs using Cu_2O annealed at 700 °C showed a field-effect mobility of ~0.9 $cm^2/V{\cdot}s$ and an on/off current ratio of $\sim3.4\times10^2$.

Cuprous oxide (Cu_2O) has come into the spotlight as a promising candidate for achieving p-type metal oxide thin film transistors (TFTs). This is because in contrast to most metal oxide materials with the strong localization of positive holes at the valence band edge consisting mainly of localized O 2*p* orbitals,[1] Cu_2O has chemical bonds with considerable covalency between copper cations and oxygen anions due to the close energy levels of the Cu 3*d* and O 2*p* orbitals. This leads to a significant reduction in the localization nature of the valence band maximum (VBM)[2,3] and therefore more effective hole transport (i.e. high hole mobility). In addition, Cu_2O can also be used as a p-type semiconductor layer for solar cells because of its direct band gap characteristic with a high absorption coefficient in the visible region.[4] Cu_2O films can be formed by a variety of methods such as reactive sputtering,[1] pulsed laser deposition (PLD),[5] chemical vapor deposition (CVD),[6] thermal oxidation,[7] radical oxidation by O_2 plasma,[8] electrochemical deposition,[9] and sol-gel.[10] Among them, reactive sputtering is a relatively cost-effective method for large area deposition[11] and a simple and conventional process that can directly deposit Cu_2O.

Author to whom correspondence should be addressed. Electronic mail: ajf@eng.cam.ac.uk.

However, spatial directivity of non-spherical Cu 3*d* orbitals mainly forming the VBM makes them sensitive to bonding angle. This leads to severe disorder in films especially in the case of Cu_2O formed by reactive sputtering at room temperature (i.e. without substrate heating), thereby degrading hole mobility. Thus, thermal annealing of disordered Cu_2O films is necessary in order to obtain a satisfactory hole mobility. However, either oxidation or oxide reduction of copper oxide films easily occurs according to the annealing environment (i.e. air or vacuum), which leads to phase conversion (i.e. $Cu_2O \rightarrow CuO$ or vice versa).[12] To be specific, the oxidation of copper oxide ($Cu_2O \rightarrow CuO$) occurs by air annealing because of the diffusion of oxygen into films and the following reaction ($2Cu_2O + O_2 \rightarrow 4CuO$),[9] whereas the oxide reduction ($CuO \rightarrow Cu_2O \rightarrow Cu$) is induced by vacuum annealing because of the desorption of oxygen under vacuum through the reactions of $4CuO \rightarrow 2Cu_2O + O_2$ and $2Cu_2O \rightarrow 4Cu + O_2$.[13,14] Thus, it is difficult to maintain the phase of Cu_2O while improving film quality by thermal annealing, which also limits annealing temperature. For this reason, few groups have performed thermal annealing of sputtered copper oxide to improve electrical performance of copper oxide TFTs, and they also observed the phase conversion of copper oxide. Specifically, Fortunato et al. fabricated Cu_2O TFTs annealed at 200 °C in air with a field-effect mobility (μ_{FE}) of 1.2×10^{-3} $cm^2/V\cdot s$ and the CuO phase appeared in a Cu_2O film in the X-ray diffraction pattern.[1] Sung et al. fabricated p-type CuO TFTs with μ_{FE} of 0.4 $cm^2/V\cdot s$ through air annealing of Cu_2O.[15] Although Sohn et al. investigated the effects of vacuum annealing on electrical properties of copper oxide TFTs (the highest μ_{FE} = 0.07 $cm^2/V\cdot s$), they used as-deposited CuO and observed that phase conversion from CuO to Cu_2O occurred by vacuum annealing.[16] However, there have been no reports yet on the effects of annealing temperature, especially at a high temperature ≥ 500 °C, on film properties of sputtered Cu_2O and the performance of Cu_2O TFTs without the phase conversion by either its oxidation or oxide reduction.

In this letter, it is demonstrated that, by the vacuum annealing of as-deposited Cu_2O, it is possible to perform the thermal treatment of Cu_2O up to 700 °C without concern about phase conversion, such as oxidation or reduction. Here, the oxidation is avoided with vacuum annealing, and oxide reduction is also screened since it requires a higher temperature > ~800 °C in vacuum based on the pressure-temperature diagram in the Cu-O system.[12] This enabled investigation of the pure effects of annealing temperature on film properties as well as electrical characteristics of Cu_2O TFTs without any phase conversion at the temperature range applied here (500 ~ 700 °C). This has also allowed fabrication of Cu_2O TFTs with μ_{FE} of 0.9 $cm^2/V\cdot s$ which is a higher value compared to those of sputter-deposited copper oxide TFTs using post-deposition annealing.[1,15,16]

Cu_2O was grown by reactive sputtering using a high target utilization sputtering (HiTUS) system (Plasma Quest Limited) which enables independent control of Ar plasma density and ion energy by generating the Ar plasma in a remote chamber. The main features and advantages of HiTUS are well described with its schematic diagram in Refs. 17 and 18. The base pressure was 6.0×10^{-6} mbar, and then Ar gas was supplied to give a process pressure of 1.5×10^{-3} mbar. The reactive sputtering was performed at an RF launch power of 1.2 kW, a DC bias power of 0.95 kW, an oxygen flow rate of 16 sccm, and with no substrate heating. The as-deposited Cu_2O was annealed in vacuum in an Aixtron Cambridge Nanoinstruments Black Magic 2 system under a base pressure of 9.5×10^{-4} mbar at various temperatures for 10 min. Annealing temperature was monitored with an infrared (IR) radiation pyrometer (Infratherm IGA8 plus) and all the samples were unloaded at a chamber temperature of 50 °C after a cooling time of 20 min. Film thickness was about 500 nm, which was measured by surface profilometry (Veeco Dektak 200SI). Film characteristics of Cu_2O were obtained by a Bruker D8 Discover X-ray diffractometer (XRD), an ATI Unicam UV/Vis spectrometer (UV2-200), and an MMR Technologies Hall Effect Measurement System (K2500-7).

First of all, XRD was used to examine the vacuum annealing effect on the sample microstructure by comparing annealed samples with as-deposited material. As seen in Fig. 1, the intense peak close to 42.33° is detected in the as-deposited film, which is related to the (200) diffraction peak of Cu_2O. An increase in vacuum annealing temperature leads to a significant increase in the intensity of the Cu_2O (200) peak from 95 cps of the as-deposited film to 4175 cps. The intensity was obtained by subtracting each baseline (i.e. background noise) from the peak maximum. This shows that an increase in vacuum annealing temperature gives rise to more enhancement of film crystallinity, indicating a reduction in disorder in the

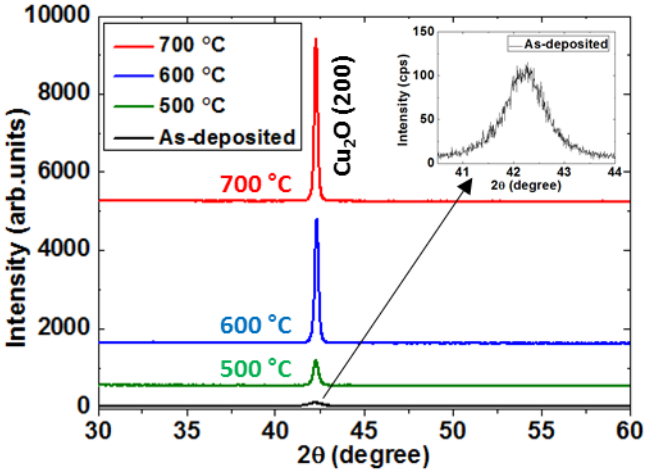

FIG. 1. X-ray diffraction patterns of Cu_2O before and after vacuum annealing at 500, 600, and 700 °C; an increase in the intensity of the (200) peak is observed: 95 cps (as-deposited), 650 cps (500 °C), 3200 cps (600 °C), and 4175 cps (700 °C). Inset shows an enlarged X-ray diffraction pattern of as-deposited Cu_2O.

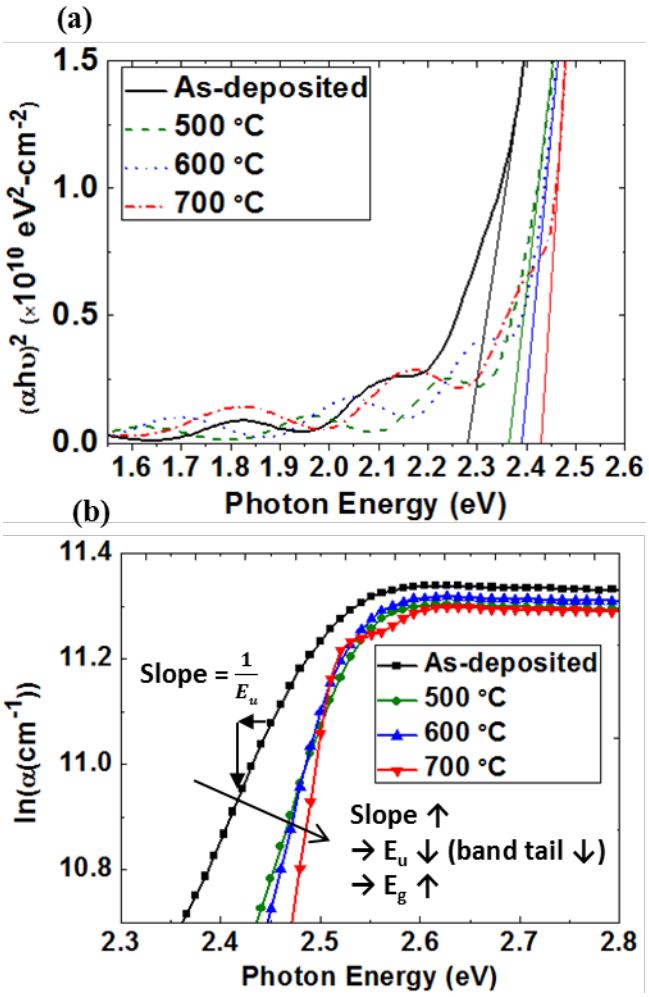

FIG. 2. (a) $(\alpha h\upsilon)^2$ and (b) ln(α) versus photon energy plot for Cu_2O with different vacuum annealing temperatures for extracting the optical band gap and the Urbach tail respectively.

film. In addition, although Cu_2O was exposed to the high temperature of 700 °C, the Cu phase is not observed, showing that it is possible to apply the vacuum annealing up to 700 °C without oxide reduction to Cu.

For investigating the vacuum annealing effect on the optical band gap, the films deposited on quartz (Spectrosil B) substrates were annealed at different temperatures from 500 to 700 °C. As shown in Fig. 2(a), the optical band gap of Cu_2O was deduced from the x-intercept of the linear part of the Tauc plot of $(\alpha h\upsilon)^2$ versus $h\upsilon$, where α, h and υ are the optical absorption coefficient, the Planck's constant and the photon frequency.[7] Figure 2(a) clearly shows that as annealing temperature increases, the extracted optical band gap increases from about 2.28 eV (as-deposited) to 2.43 eV (700 °C), which can be attributed to a reduction in band tail states. In order to confirm this, we examined a change in the Urbach tail which is interpreted as the width of tail states caused by disorder in films.[19] As for the method for extracting the Urbach tail, the optical absorption coefficient $\alpha(\upsilon)$ in the low photon energy range follows the empirical exponential law represented by (1),

$$\alpha(\upsilon) = \alpha_0 \exp\left(\frac{h\upsilon}{E_u}\right), \quad (1)$$

where α_0 is a constant and E_u denotes the Urbach energy (i.e. the Urbach tail).[20] Equation (1) can be written as $\ln(\alpha) = (1/E_u)(h\upsilon) - \ln(\alpha_0)$, as a result Urbach tails can be extracted from the reciprocal of the slopes of the linear portion of the $\ln(\alpha)$ versus $h\upsilon$ plot as seen in Fig. 2(b). This represents that an increase in vacuum annealing temperature leads to a reduction in the Urbach tail from about 220 meV (as-deposited) to 160 meV (500 °C), 120 meV (600 °C), and 78 meV (700 °C), which is clear evidence that widening of the optical band gap results from a reduction in the band tail states. This also indicates a decrease in disorder in the Cu_2O film by an increase in annealing temperature considering the fact that disorder produces band tail states.[19–21]

As for the vacuum annealing effect on Hall mobility (μ_{Hall}), as shown in Fig. 3(a), μ_{Hall} improves significantly from about 0.14 to 28 $cm^2/V{\cdot}s$ as vacuum annealing temperature increases. The enhancement of μ_{Hall} is consistent with a reduction in hole trapping/de-trapping events by donor-like trap states, arising from a decrease in the valence band tail (i.e. donor-like states) with the increase in annealing temperature, as indicated by a reduction in the Urbach tail. In addition, as seen in Fig.

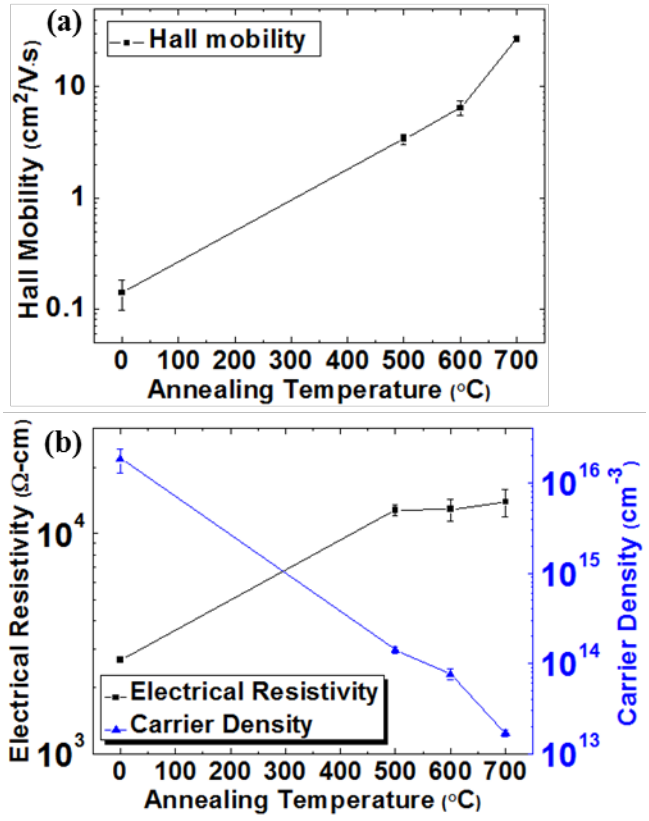

FIG. 3. (a) Hall mobility and (b) electrical resistivity and carrier density of Cu_2O thin films as a function of the vacuum annealing temperature.

3(b), an increase in annealing temperature leads to an increase in electrical resistivity from 2.7×10^{3} to 1.4×10^{4} Ω·cm and a significant reduction in intrinsic carrier density from 1.8×10^{16} to 1.7×10^{13} cm^{-3}.

Bottom-gate staggered p-type Cu_2O TFTs were fabricated in order to examine the effects of vacuum annealing temperature on their electrical characteristics. Cu_2O was formed on thermally-grown SiO_2-coated 4 inch p^+-Si wafers with AZ5214E photoresist by a lift-off process. The heavily doped p-type Si wafer was used as a common gate electrode and the 260-nm-thick thermal SiO_2 coating was employed as a gate insulator. The Cu_2O active layers were subjected to vacuum annealing at 500, 600, and 700 °C. Finally, source/drain (S/D) electrodes were formed on the annealed Cu_2O active layers by thermal evaporation (Edwards E306A) of Au and the lift-off process used to achieve a channel width-to-length ratio (*W*/*L*) of 10 with a channel length of 100 μm. The electrical characteristics were measured by a semiconductor parameter analyzer (HP 4140B) in a dark box at ambient atmosphere.

The transfer characteristics of Cu_2O TFTs annealed at 500, 600, and 700 °C are shown in Fig. 4(a). They show that the off-state current (scaled for channel width) at V_{DS} = -5 V decreases from ~1.35 nA/μm (500 °C) to ~0.1 nA/μm (700 °C), which results from a decrease in intrinsic carrier density in the Cu_2O active layer from ~1.4×10^{14} cm^{-3} (500 °C) to ~1.7×10^{13} cm^{-3} (700 °C). In addition, the on/off current ratio increases from ~3 (500 °C) to ~340 (700 °C), which is due to improvement

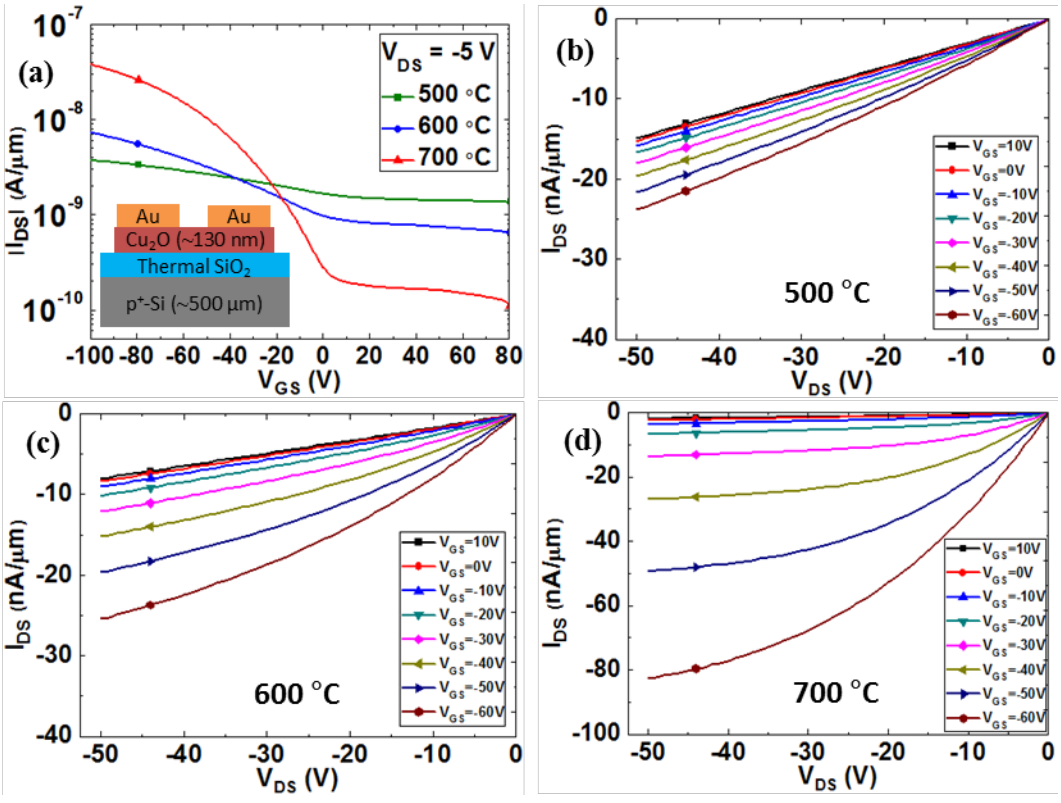

FIG. 4. (a) Transfer characteristics at V_{DS} = -5 V of Cu_2O TFTs annealed at different temperatures and output characteristics of Cu_2O TFTs annealed at (b) 500, (c) 600, and (d) 700 ˚C. Inset shows the schematic structure of the fabricated Cu_2O TFTs.

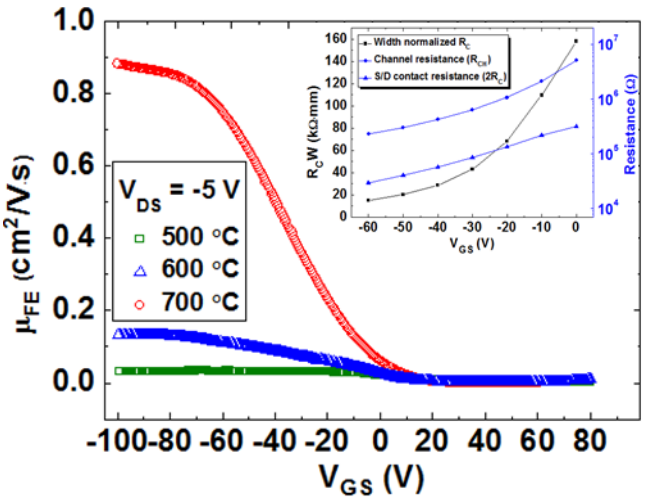

FIG. 5. The extracted linear field-effect mobility as a function of V_{GS} at V_{DS} = -5 V. Inset shows width normalized contact resistance (R_CW) (left-axis), R_{CH} and $2R_C$ (right-axis) with various V_{GS}.

in the transfer characteristic (i.e. I_{DS} modulation by V_{GS}) and a reduction in the off-state current. The output characteristics (Fig. 4(b), (c), and (d)) show that linear and saturation regions become more distinct as annealing temperature increases, and especially Cu_2O TFTs annealed at 700 °C (Fig. 4(d)) exhibit a clear pinch-off behavior without current crowding in the low V_{DS} region. Fig. 5 shows the linear field-effect mobility (μ_{FE}) as a function of a gate voltage calculated from $\mu_{FE} = (\partial I_{DS}/\partial V_{GS}) \times (L/WC_iV_{DS})$ using the transfer curves at V_{DS} = -5 V, where L, W, and C_i are the channel length, channel width, and gate dielectric capacitance per unit area respectively. As shown in Fig. 5, the extracted μ_{FE} improves significantly from ~0.03 $cm^2/V{\cdot}s$ to ~0.9 $cm^2/V{\cdot}s$ as annealing temperature increases from 500 to 700 °C. In addition, since the contact resistance (R_C) of S/D Ohmic contacts leads to a lower extracted μ_{FE} than its actual intrinsic value in the channel region,[22] the Ohmic contact quality of fabricated Cu_2O TFTs should be considered. The channel resistance per unit channel length (R_{ch}) and the S/D contact resistance ($2R_C$) were extracted from the slope and R_T-intercept of the R_T versus L plot (i.e. $R_T = R_{ch}L + 2R_C$, R_T is measured total resistance) using the transmission line method (TLM). We used four TFTs with a fixed channel width (1 mm) and a different channel length ranging from 10 to 100 μm as the TLM patterns. Here, unlike silicon based TFTs, we should note that R_C of metal oxide based TFTs is dependent on V_{GS} since there is no highly doped S/D contact region between the active layer and S/D electrodes.[23,24] For this reason, R_C was extracted at various V_{GS} ranging from 0 to -60 V. As seen in the inset (left-axis) of Fig. 5, the width normalized contact resistance (R_CW) decreases from 160 kΩ·mm (off-state) to 15 kΩ·mm (on-state) with an increase in V_{GS} from 0 to -60 V. In order to examine the effect of R_C on extracted μ_{FE}, $R_{CH} = R_{ch}L$ (L = 100 μm) and $2R_C$ were also compared as shown in the inset (right-axis) of Fig. 5. Considering that the S/D contact resistance ($2R_C$) as a fraction of the total resistance ($R_T = R_{CH} + 2R_C$) is ~10 %, it is expected that the extracted μ_{FE} can be enhanced further if the S/D ohmic contacts are improved. Finally, Cu_2O TFTs annealed at 700 °C operated in the enhancement mode with a

threshold voltage (V_T) of around -30 V and a sub-threshold slop (SS) of ~26 V/dec. The high V_T can be resolved by reducing the thickness of a gate insulator (SiO_2) or using a high-*k* insulator. By doing so, it is also expected to reduce the operating voltage of TFTs. In addition, the high SS indicates that there are high-density interface traps between the gate insulator and Cu_2O active layer. Thus, if the interface traps can be reduced by improving the interface quality, then it is expected to lead to not only improvement in SS but also a further enhancement in μ_{FE}.

In conclusion, it is shown that as-deposited Cu_2O can be vacuum annealed to improve the film quality without any phase conversion, and the performance of TFTs also enhances significantly by the resulting improvement in the Cu_2O film quality by the enhancement of film crystallinity and a decrease in band tail states. Although further work is required to enhance the interface quality for a further improvement in device performance, these results provide evidence that vacuum annealing of as-deposited Cu_2O can be performed up to 700 °C in order to further enhance Cu_2O TFT performance without concern about phase conversion based on the improvement in μ_{FE} and on/off current ratio. Finally, the control of intrinsic carrier density in the Cu_2O active layer by vacuum annealing can also be a useful technique for reducing the high off-state current; this is essential for commercial use of Cu_2O TFTs.

This work was supported by the Engineering and Physical Sciences Research Council under Grant No. EP/M013650/1. Additional data related to this publication is available at the DSpace@Cambridge data repository (http://www.repository.cam.ac.uk). S.H. wishes to thank Hayley Brown from Plasma Quest Limited for providing beneficial information about her previous research on copper oxide using the HiTUS system. G.R. acknowledges the support of the Cambridge Trusts.

[1]Elvira Fortunato, Vitor Figueiredo, Pedro Barquinha, Elangovan Elamurugu, Raquel Barros, Goncalo Goncalves, Sang-Hee Ko Park, Chi-Sun Hwang, and Rodrigo Martins, Appl. Phys. Lett. **96**, 192102 (2010).

[2]Hiroshi Kawazoe, Hiroshi Yanagi, Kazushige Ueda, and Hideo Hosono, MRS Bull. **25**, 28 (2000).

[3]Hiroshi Yanagi, Hiroshi Kawazoe, Atsushi Kudo, Masahiro Yasukawa, and Hideo Hosono, J. Electroceram. **4**, 407 (2000).

[4]Zhigang Zang, Atsushi Nakamura, and Jiro Temmyo, Opt. Express **21**, 11448 (2013).

[5]K. Matsuzaki, K. Nomura, H. Yanagi, T. Kamiya, M. Hirano, and H. Hosono, Appl. Phys. Lett. **93**, 202107 (2008).

[6]S. Y. Lee, S. H. Choi, and C. O. Park, Thin Solid Films **359**, 261 (2000).

[7] V. Figueiredo, E. Elangovan, G. Goncalves, P. Barquinha, L. Pereira, N. Franco, E. Alves, R. Martins, E. Fortunato, Appl. Surf. Sci. **254**, 3949 (2007).

[8]Zhigang Zang, Atsushi Nakamura, and Jiro Temmyo, Mater. Lett. **92**, 188 (2013).

[9]Mohd Rafie Johan, Mohd Shahadan Mohd Suan, Nor Liza Hawari, and Hee Ay Ching, Int. J. Electrochem. Sci. **6**, 6094 (2011).

[10]S. Y. Kim, C. H. Ahn, J. H. Lee, Y. H. Kwon, S. Hwang, J. Y. Lee, and H. K. Cho, ACS Appl. Mater. Interfaces **5**, 2417 (2013).

[11]E. Fortunato, P. Barquinha, and R. Martins, Adv. Mater. **24**, 2945 (2012).

[12]Jian Li, G. Vizkelethy, P. Revesz, and J. W. Mayer, J. Appl. Phys. **69**, 1020 (1991).

[13]S. Y. Lee, N. Mettlach, N. Nguyen, Y. M. Sun, and J. M. White, Appl. Surf. Sci. **206**, 102 (2003).

[14]Jianmin Yu, Guoxia Liu, Ao Liu, You Meng, Byoungchul Shin, and Fukai Shan, J. Mater. Chem. C **3**, 9509 (2015).

[15]Sang-Yun Sung, Se-Yun Kim, Kwang-Min Jo, Joon-Hyung Lee, Jeong-Joo Kim, Sang-Gon Kim, Kyoung-Hoon Chai, S. J. Pearton, D. P. Norton, and Young-Woo Heo, Appl. Phys. Lett. **97**, 222109 (2010).

[16]Joonsung Sohn, Sang-Hun Song, Dong-Woo Nam, In-Tak Cho, Eou-Sik Cho, Jong-Ho Lee, and Hyuck-In Kwon, Semicond. Sci. Technol. **28**, 015005 (2013).

[17]A. J. Flewitt, J. D. Dutson, P. Beecher, D. Paul, S. J. Wakeham, M. E. Vickers, C. Ducati, S. P. Speakman, W. I. Milne, and M. J. Thwaites, Semicond. Sci. Technol. **24**, 085002 (2009).

[18]L. Garcia-Gancedo, J. Pedros, Z. Zhu, A. J. Flewitt, W. I. Milne, J. K. Luo, and C. J. B. Ford, J. Appl. Phys. **112**, 014907 (2012).

[19]Y. Natsume, H. Sakata, and T. Hirayama, Phys. Status Solidi A **148**, 485 (1995).

[20]Shadia Jamil Ikhmayies and Riyad N. Ahmad-Bitar, J. Mater. Res. Technol. **2**, 221 (2013).

[21]J. Robertson, B. Falabretti, and D. S. Ginley (ed.), *Handbook of Transparent Conductors* (Springer, 2011) pp. 27–50.

[22]Elizabeth von Hauff, Nicolas Spethmann, and Jurgen Parisi, Z. Naturforsch. **63a**, 591 (2008).

[23]Jaechul Park, Changjung Kim, Sunil Kim, Ihun Song, Sangwook Kim, Donghun Kang, Hyuck Lim, Huaxiang Yin, Ranju Jung, Eunha Lee, Jaecheol Lee, Kee-Won Kwon, and Youngsoo Park, IEEE Electron Device Lett. **29**, 879 (2008).

[24]Manoj Nag, Adrian Chasin, Maarten Rockele, Soeren Steudel, Kris Myny, Ajay Bhoolokam, Ashutosh Tripathi, Bas van der Putten, Abhishek Kumar, Jan-Laurens van der Steen, Jan Genoe, Flora Li, Joris Maas, Erik van Veenendaal, Gerwin Gelinck, and Paul Heremans, J. Soc. Inf. Display **21**, 129 (2013).