Critical challenges in the development of electronics based on two-dimensional transition metal dichalcogenides

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Abstract: The development of high-performance electronic devices based on two-dimensional (2D) transition metal dichalcogenide semiconductors has recently advanced from one-off proof of principle demonstrations to more reproducible integrated devices. It has, in particular, reached a point where the material quality — as well as the interfaces between the metal contacts, dielectrics and 2D semiconductors — must be optimized to increase device performance. Here we examine the key immediate challenges for the development of electronics based on 2D transition metal dichalcogenides, and identify doping, p-type contacts, and high-*k* dielectrics as critical issues. We argue that these challenges stem from the high density of defects present in 2D transition metal dichalcogenides, and suggest that the community focus more on the growth of high-quality materials with a low concentration of defects. We also provide recommendations on identifying industry compatible dielectrics for these 2D devices.

Introduction:

Electronics based on two-dimensional (2D) transition metal dichalcogenides (TMDs) is advancing rapidly[1]. Recent developments include field-effect transistors (FETs) based on monolayer tungsten diselenide (WSe_2) with room temperature mobilities of more than 1000 cm^2-V^{-1}-s^{-1} (ref. [2,3]), n-type FETs based on monolayer molybdenum disulfide (MoS_2) with contact resistance values close to the quantum limit[4], and massive arrays of FETs for active pixel sensors[5]. 2D TMDs are also now firmly on the technology roadmaps of companies including the Taiwan Semiconductor Manufacturing Corporation (TSMC), Intel, Imec, and Samsung[6]. However, a number critical challenges still need to be addressed - and in an industry compatible way - before such devices can be of wider practical value.

In this Perspective, we explore the challenges involved in the development of electronics based on 2D TMDs. We highlight three key issues: doping[7,8], low resistance contacts (especially p-type), and industry compatible high-*k* dielectrics. We argue that these challenges stem from the fact that 2D TMDs are riddled with point defects (Fig. 1a) such as charged chalcogen vacancies and isovalent impurities[2,9] — something that the community has been reluctant to discuss openly in context of performance of electronic devices. The defects in 2D TMDs detrimentally affect device properties including on-state current, variation in threshold voltage, and mobility. For optics and photonics, the influence of point defects in 2D TMDs is less pronounced but for electronics, decreasing defect concentration is essential. For example, a photoluminescence quantum yield of close to 100 % can be achieved in 2D TMDs[10,11] but electrically driven luminescence yield is typically less than few percent due to scattering, recombination of carriers, and poor contacts[12].

Charged chalcogen vacancies in mechanically exfoliated or chemical vapour deposited 2D TMDs induce high carrier concentration (up to 10^{12} per cm^2) (ref. [13]). The large starting carrier concentration due to vacancies along with presence of neutral impurity atoms make it challenging to modulate the carrier concentration with substitutional doping. The inability to dope 2D TMDs also makes it difficult to make good contacts (both p- and n-type): that is, degenerately doped regions are used in silicon for n- and p-type contacts, but similar strategies cannot be used in 2D TMDs.

The high chalcogen vacancy concentration also leads to stronger interactions with charges in the dielectric, which introduce interface states and unintentional doping from the substrate[14–16]. For example, p-type FETs with van der Waals (vdW) contacts can only be achieved by suppressing the contribution from the dielectric by passivating the substrate[17–19]. Unintentional doping from vacancies and dielectric also leads to large variation in threshold voltage of transistors. In addition, the defects increase scattering, which leads to low mobilities. For example, room-temperature mobilities of more than 1,000 cm^2-V^{-1}-s^{-1} have been achieved in low vacancy WSe_2 (ref. [2,3]) — which is well above the theoretical upper limit of ~ 400 cm^2-V^{-1}-s^{-1} (ref. [20]) — by encapsulating monolayer TMD in hexagonal boron nitride.

Wafer scale but defective

2D TMDs consist of a transition metal (such as Mo, W, or Nb) and two chalcogens (S, Se, or Te). The melting temperature of transition metals is substantially higher (> 2000 °C) than that of chalcogens (< 450 °C). Therefore, high temperature synthesis of bulk crystals by chemical vapour transport and single layers of TMDs by chemical vapour deposition inevitably leads to chalcogen vacancies upon cooling from the growth temperature (typically > 650 °C)[21]. Other types of point defects, including transition metal vacancies and substitutional atoms, from the growth precursors can also be present[2]. Point defects can be easily observed in high-resolution scanning transmission electron microscopy (STEM) (Fig. 1b)[22].

While there are contradictory calculation results about the energy levels of the vacancies and whether they are charged[23,24], there is general consensus that chalcogen vacancies result in in-gap defect states located close to the conduction band (Fig. 1c)[23]. This is validated by differential conductance (dI/dV) spectra of sulfur vacancies using scanning tunnelling spectroscopy (STS) in a scanning tunnelling microscopy (STM), which show in-gap peaks near the conduction band edge[9,25,26]. Stoichiometry analysis of bulk MoS_2 indicates that the Mo:S ratio can range from 1:1.8 to 1:2.05 (ref. [27]), as measured by high-resolution Rutherford backscattering spectrometry and X-ray photoemission spectroscopy (XPS). The large number of chalcogen vacancies give rise to a low energy shoulder in the XPS Mo peak due to undercoordinated Mo sites[28]. This shoulder has been shown to decrease when the defective sample is exposed to oxygen during XPS measurements[29].

Studies also show that the isovalent defects (density of around 10^{12} cm^{-2}) such as oxygen passivated sulfur vacancies and impurity metal atoms are not charged[9,30]. Calculations and STS measurements suggest that oxygen can passivate in-gap states[31–33]. It has been shown that oxygen-incorporated MoS_2 exhibits enhanced photoluminescence, higher work function, and improved contact resistance due to passivated in-gap states[33]. However, whether passivation of sulfur vacancies with oxygen can improve the channel mobility has yet to be confirmed.

It is generally known that thermal[22] or metal organic chemical vapour deposition (MOCVD)[34] grown 2D TMDs contain substantial amounts of vacancies and other point defects. Despite this, synthesis papers routinely claim “high quality” and “wafer scale” 2D TMDs. While large scale growth at low temperature is essential for complementary metal oxide semiconductor (CMOS) processing, the quality of the materials will ultimately determine their value for electronic devices. Quality of 2D TMDs is often assessed by measuring the mobility of FETs. Typically, mobility values achieved on mechanically exfoliated, thermal and MOCVD samples can range from 10 – 200 cm^2-V^{-1}-s^{-1} (Fig. 1d) and these are taken as good quality materials. We now know that mobilities are limited by scattering and decreasing charged and isovalent defect densities below 10^{10} cm^{-2} and 10^{11} cm^{-2} (Fig. 1e), respectively, using two-step flux method can lead to room temperature mobilities of > 1000 cm^2-V^{-1}-s^{-1} and low temperature values of ~50,000 cm^2-V^{-1}-s^{-1} (Fig. 1d)[2,3,35]. Thus, the focus should be on growth of 2D TMDs with low defect concentration and the quality of the grown materials should be determined by the amount of charged vacancies and isovalent substitution defects.

While the growth by MOCVD continues to improve, defects of up to 10^{12} cm^{-2} remain along with a sizeable fraction of grain boundaries[36]. Also, most MOCVD growth of 2D TMDs involves the use of salts (such as NaCl) as growth facilitators – especially for low temperature growth[37]. The growth facilitators can be incorporated into the lattice and are not compatible with CMOS fabrication processes. It is therefore important to clearly specify the use of such additives and more importantly to eliminate them altogether. A promising direction on growth is the work on highly oriented epitaxial growth on sapphire for large crystal 2D TMDs over macroscopic areas[38,39]. Understanding how these materials nucleate and grow will provide valuable insight into growth of highly oriented and large grain 2D TMDs. This, along with methods to passivate chalcogen vacancies and minimising impurities will be crucial for realising high quality materials.

Strategies similar to the two-flux method in which crystal growth occurs in excess chalcogen atmosphere to minimise vacancies should be adopted for wafer scale (MO)CVD approaches. While modest success has been achieved towards chalcogen vacancy healing in monolayers[40], high-quality materials with low defect concentrations remain elusive. The low vapour pressure of sulfur makes it difficult to grow sulphide 2D TMDs using this approach, however.

It is challenging to quantify atomic defects over wafer scale samples. Scanning tunnelling microscope (STM) and STEM analysis have been used but they probe small areas. The vacancy concentration obtained by STM (10^{10} - 10^{11} cm^{-2}) is generally lower than that measured by STEM (10^{12} - 10^{13} cm^{-2}). Progress in conductive atomic force microscopy (CAFM) provides pathway for quantitatively characterising defects over large areas[41]. Recent work on dilute substitutional doping and their identification using CAFM is promising for realizing doped 2D TMDs if defects and the associated carrier concentration can be reduced to ~ 10^{10} cm^{-2} in wafer scale samples[42]. Xu *et al* also demonstrated that CAFM and STM could image identical defects, both qualitatively and quantitatively (Fig. 1f) [43].

CVD grown 2D TMDs contain significant amounts of chalcogen vacancies and other defects. We therefore recommend that studies that focus more on improving quality of grown materials and not just on wafer scale growth or exotic heterostructures will be more valuable to the community. Authors should report atomic defect densities for new growth processes. High quality TMDs with much lower or passivated vacancies are required for doping. A focus on developing methods for controllable doping of 2D TMDs with initial free carrier concentration of < 10^{10} cm^{-2} will be useful towards developing doping strategies.

Doping 2D TMD semiconductors

Doping 2D TMDs with foreign atoms such as Niobium or Rhenium[44,45] has to be done during growth. Post growth implantation of dopants will destroy the 2D TMD structure. In addition, incorporation of substitutional dopants with different concentrations for the channel and contacts regions during growth will be challenging. Doping via surface charge transfer could be another approach. Over the past few years, it has been demonstrated that potassium (K) and benzyl viologen (BV) introduce electron doping on TMDs while nitrogen dioxide (NO_2), chloroauric acid ($HAuCl_4$) and ruthenium chloride ($RuCl_3$) cause hole doping effect on TMDs[3,46–49]. However, those dopants are either highly chemical reactive or have low thermal stability.

Another promising way of doping 2D TMDs is through localized electrostatic dipole doping. Recent work has shown that sub-stoichiometric oxides such as SiO_x, AlO_x, TaO_x, and HfO_x on MoS_2 (ref. [50–52]) can achieve electron doping of up to 2×10^{13} cm^{-2}. Native oxide of WSe_2 have been demonstrated to hole dope WSe_2 FETs[53]. However, the mechanism and stability of this type of doping is not well understood. It could be due to the electrostatic dipole formed at oxide surface or hybridization between the oxide and TMDs. Localized electrostatic doping can tune of threshold voltage of FETs. For example, HfO_2 dielectric with different La or Al interface dipoles can shift the threshold voltage of silicon nanosheet FETs over 0.6 V [54]. SiN_x/Al_2O_3 interface dipoles with and without Al_2O_3 have also been demonstrated to change the polarity of carbon nanotube FETs from N-type to P-type[55]. These studies have yet to be applied on 2D TMDs.

We recommend that in addition to measuring FET devices, complementary methods such as Raman and XPS that are better for accurately assessing the doping level should be used. For example, A_{1g} mode is MoS_2 is sensitive to the carrier concentration due to strong electron-phonon coupling[56]. The Mo 3*d* peak position in XPS measures core level to Fermi level that reflects electron/hole doping in MoS_2 (ref. [57]).

Degenerate doping of TMDs for contacts is urgently needed, especially p-type doping. Insights into how dielectrics contribute to doping of TMDs are also needed as this interface is critical in the FET device. Chemical and thermal stability of the doping strategy should also be considered.

2D TMD semiconductor/metal contacts

It is now widely understood that deposition of metals on top of 2D TMDs leads to damage[58]. Recent developments in clean vdW contacts using indium then bismuth and antimony on 2D TMDs have improved the on state currents of n-type FETs and decreased the contact resistance close to the quantum limit (Fig. 2a,b,c)[4,58,59]. N-type contacts are facilitated by the excess of electrons from defects in the materials. Thus, while these development in n-type contacts are important, they can be classified as low hanging fruit. P-type contacts on 2D TMDs are particularly challenging because they require high work function metals with high melting temperatures. The evaporation of such metals requires high energy, which leads to sublimated atoms with high kinetic energy that is transferred to 2D TMDs upon deposition – leading to defects at the metal/2D TMD interface and pinning of the Fermi level. Our recent work[19] on using gentle deposition of Pt or Pd vdW contacts onto 2D TMDs provides a pathway for realizing high performance p-type FETs (Figure 2d). The resistance for these contacts remains high (as indicated in Fig. 2e) due to low work function of the metals when in contact with WSe_2. Studies show that high hole current can be achieved by growing high work function metallic VSe_2 as contacts for WSe_2 FETs[60,61]. NbS_2 and TiS_2 as well as semimetal $Co_3Sn_2S_2$ are predicted to have high work functions and can be used as hole injection contacts for WSe_2 FETs[62]. In addition to the high work function van der Waals contacts, hole doping of 2D TMDs is required to achieve high performance p-type FETs. The suppression of electron concentration through reduction of point defects is also critical for achieving p-type FETs.

It should be noted that most of the academic work on contacts is focused on top contacts while practical implementation of 2D TMDs into devices will most likely utilise edge contacts[63]. However, edge contacts are difficult to characterise and therefore top contacts can provide fundamental understanding that can be applied for making edge contacts. In both top and edge contacts, degenerately doped regions will be essential for achieving p- and n-type FETs.

High quality ferromagnetic (FM) contacts that can efficiently inject and collect spins are needed for spintronic memories based on 2D TMDs[64]. The challenge with FM metals as contacts is that they have high chemical reactivity and therefore readily react with the 2D TMDs – causing spin scattering and loss at the FM/TMD interface[65]. The realisation of vdW contacts on 2D TMDs could enable spin based devices[64,66].

In summary, thin metal film deposition on TMDs needs to be further studied and strategies for depositing high work function metal contacts on 2D TMDs without causing damage are required. Degenerately hole doped 2D TMDs with clean van der Waals contacts to achieve p-type contacts with resistances of $< 100\ \Omega\cdot\ \mu m$ are needed.

2D TMD semiconductor/dielectric interface

The dielectric/2D TMD interface has been less studied. However, the dielectric is critically important for devices. The main reason silicon was selected over other semiconductors for modern electronics is because it forms the ideal semiconductor/dielectric (Si/SiO_2) interface. The chemical inertness of 2D TMDs makes it challenging to nucleate and uniformly grow high *k* dielectrics. It is generally assumed that the dielectric on which the 2D TMDs are grown or transferred is chemically and electronically inert. However, studies have reported different trion/exciton ratios in photoluminescence of 2D TMDs placed on different dielectric substrates[67]. In FETs, p-type operation requires using dielectric substrates that suppress electron doping[19]. These results suggest that the semiconductor/dielectric interface is not passive and can strongly influence the electronic properties. Dielectrics grown by atomic layer deposition (ALD) can contain charged impurities or oxygen deficiencies that can lead to fixed positive charges that create dipoles that can extend into the 2D TMDs[68] (Fig. 3a and 3b) – influencing the metal/semiconductor junction and Schottky barrier height associated with it and activating dopants (from point defects) in the material. This leads to further increase in the carrier (electrons in the case of MoS_2) concentration. Strategies to suppress dielectric doping include using PMMA, self-assembled monolayers, or hBN as inert layers[69]. These materials however are not suitable dielectrics for CMOS processes and therefore insulating layers that do not perturb the electronic properties of 2D TMDs are required.

In the case of 2D TMDs, the surface states of dielectrics become important because unlike on Si, there is no chemical interaction between the dielectric and semiconductor. That is, for 2D TMDs on different dielectrics, the surface states of dielectrics remain unpassivated, which can induce dipoles and electrostatic doping. The development of high k dielectrics for 2D TMD FETs should consider the following key requirements:

First, the k value of dielectrics should be high enough for scaling. hBN is widely used by the community because it forms clean van der Waals interface with 2D TMDs. However, the low dielectric constant of hBN means that ultra-thin (1.3 nm) layer is required for achieving an equivalent oxide thickness (EOT) of 1 nm. Calculations and experiments show that even with ideal defect-free single crystal hBN, the leakage current is too high for practical FETs[70].

Second, inert, stable, and amorphous dielectrics are preferred. The dielectric must be thermodynamically and mechanically stable as well as being chemically inert. For example, while HfO_2 and ZrO_2 possess similar dielectric attributes, ZrO_2 forms ZrSi making it unsuitable for silicon electronics[71]. In the case of 2D TMDs, HfO_2 may be less suitable because calculations indicate that Hf-terminated HfO_2 surface and MoS_2 readily form Hf-S bonds (Fig. 3a)[72]. The interfacial interactions give rise to hysteresis and large subthreshold swing (SS) in the transfer characteristics of FETs (Fig. 3c). Decoupling interactions between 2D TMD semiconductor and oxide dielectric by introducing a vdW gap allows FETs with low hysteresis and low SS as illustrated in Fig. 3d-f (ref. [14]).

Third, the band offset between the dielectrics and 2D TMDs must be > 1 eV to prevent carrier injection. Dielectrics with band gaps of < 5 eV such as $SrTiO_3$ (band gap ~ 3.2 eV) therefore may not be ideal for 2D TMDs. The band offset at the semiconductor/dielectric interface is affected by dipoles formed by charge transfer (Fig. 3b)[73]. Thus, charge transfer or chemical interaction should be avoided to prevent the band realignment.

Lastly, low interface defect/trap states should be realized to achieve low subthreshold swing. Defects at the interface arise from chalcogen vacancies in 2D TMDs, oxygen vacancies in the oxide dielectric, impurities, and interface reactions[74]. These defects lead to large threshold voltage shifts, low mobility, large subthreshold swing, large hysteresis in the transfer characteristics (Fig. 3c), and instability in the devices.

Single-crystal dielectrics such as CaF_2, $SrTiO_3$ and Al_2O_3 that have low defect states exhibit low subthreshold swing for 2D TMD FETs[75–77]. Although crystalline dielectrics typically have higher dielectric constant and lower defect states than their amorphous counterparts, amorphous dielectrics are more uniform and exhibit better thermal and mechanical stability. Furthermore, the low defect interface with amorphous dielectric can be achieved to create a sharp van der Waals interface[14,78]. A bonus of vdW interface between 2D TMD semiconductor and dielectric is that the presence of vdW gap reduces fringing induced barrier lowering, which allows high *k* dielectric to be used to achieve low subthreshold swing FETs[77].

For practical electronic devices, top gated FETs are required. This is fundamentally challenging because 2D TMDs are chemically inert and therefore growth of uniform and continuous dielectric layer on top is challenging[79]. Further, since 2D TMDs are three atoms thick, nucleation of the oxide layer at defects leads to rapid deterioration of the electronic properties of the semiconductor. Strategies using molecules as buffer layers between the 2D TMDs and oxide dielectrics have been used to grow uniform layers[79]. Recent work has shown that it is possible to grow antimony trioxide as a buffer layer on 2D TMDs to allow integration of high-*k* dielectrics through ALD growth[80].

Here we propose that the deposition of vdW contacted thin metal layers on top of 2D TMDs and preferentially oxidising them to form oxide dielectrics could be an interesting way to overcome the nucleation and growth challenges of high *k* dielectrics on top of 2D TMDs.

A chemically inert and mechanically robust CMOS compatible dielectric with high *k* should be developed. The semiconductor/dielectric interface defect density should be reduced to lower than 10^{10} cm^{-2} eV^{-1} to achieve low subthreshold swing and no hysteresis in the transfer curve. Strategies to develop n-type FETs with small positive threshold voltage and p-type FETs with small negative threshold voltage are needed.

Outlook:

The central challenge in the development of electronics based on 2D TMDs lies in achieving low-defect wafer-scale synthesis, which will be crucial for creating intrinsic channels and potential doping strategies. The development of clean van der Waals interfaces between metals/semiconductors and semiconductors/dielectrics is also essential for achieving high-performance FETs. In particular, a CMOS compatible high-*k* dielectric that does not detrimentally influence 2D TMD channels is required. Furthermore, it is essential that any breakthrough in device performance now also considers industrial compatibility, scalability, and stability, to ensure that innovations are practical, reproducible and viable for widespread adoption.

Fig. 1: Defects in 2D TMDs. **a**, Schematic of monolayer TMD with different point defects. **b**, High-angle annular dark-field scanning transmission electron microscopy image of a single layer MoS_2 showing different types of vacancies[22] [single sulfur vacancy (yellow circles), double sulfur vacancy (orange circles), and less observed single molybdenum vacancy (green circle)]. **c**, Local density of states of monolayer MoS_2 showing in-gap states from sulfur vacancy (V_S) near the conduction band edge[33]. The V_S site is highlighted by the dashed circle shown in the inset. **d**, Comparison of mobility values versus temperature of WSe_2 fabricated using different approaches[2,18,19,60,83–85]. Most values are in the range of 10 – 200 cm^2-V^{-1}-s^{-1}. Room

temperature mobility of ~ 1000 cm^{2}-V^{-1}-s^{-1} and low temperature value of ~50,000 cm^{2}-V^{-1}-s^{-1} are achieved in low defect density WSe_2 (ref.[2]). **e**, Topographic STM images of single-crystal WSe_2 grown by CVT[35] (left) and two-step flux method[2] (right). Defects in the CVT sample (dark spots) are readily visible while no defect features are apparent in the two-step flux sample image. **f**, CAFM (left) and STM (right) images of a flake of $MoSe_2$ at the same location[43]. E_C, conduction band energy; E_V, valence band energy; LDOS, Local density of states.

Fig. 2: Summary of results on electrical contacts for 2D TMDs. a-c, Transfer characteristics of 2D MoS_2 channel FETs with indium, bismuth, and antimony source and drain contacts. The results show ON state currents of FETs in excess of 10 μA-μm^{-1} due to low contact resistance. Inset in **a** and **c** are cross-sectional STEM images of metal-MoS_2 interface. Inset in **b** is DOS of Bi and MoS_2 interface showing MoS_2 is degenerately doped by the metal contact. **d**, Transfer curve of monolayer WSe_2 channel FET with van der Waals Pt contact showing pure p-type characteristics. Inset: cross-sectional STEM image showing clean interface between Pt and monolayer WSe_2. **e**, Contact resistance versus carrier concentration for MoS_2 (solid symbols) and WSe_2 (empty symbols) with different contact metals and varying size of the van der Waals gap. The solid purple line ($d = 0$ Å) represents the quantum limit for contact resistance and it can be seen that mature semiconductors technologies approach this limit. The dashed lines represent van der Waals gap values. However, the state-of-art hole contact resistance of WSe_2 is still one order higher than practical requirements. The contact resistance values are reproduced from refs[4,18,19,49,58,59,86–90]. hBN, hexagonal boron nitride; UHV, ultra-high vacuum. Panels adapted from refs[4,19,58,59].

Fig. 3. Oxide Dielectrics for 2D TMDs. a, Schematic of a non-ideal 2D TMD semiconductor/dielectric interface. An amorphous oxide dielectric with defects is represented. The presence of defects leads to following effects: (i) electrons are easily scattered at the interface; (ii) interface dipoles form due to charge impurities within the dielectric; (iii) charge transfer between the dielectric and semiconductor; and (iv) hybridization between non-passivated dielectric surface and the 2D TMDs. **b**, Energy band diagram of a 2D TMD semiconductor and dielectric interface under thermal equilibrium. Oxide insulators such as HfO_2 or SiO_2 have acceptor traps close to the

conduction band and donor type traps close to the valence band[81,82]. The acceptor type traps are neutral when empty and negatively charged when filled. The donor type traps are neutral when filled and positively charged when empty. When the 2D TMD semiconductor is placed on the dielectric, interface states created by any interactions between the oxide and 2D TMDs can trap and de-trap carriers of the semiconductors at the interface, causing hysteresis in the transfer characteristics, threshold voltage shifts, and high subthreshold swing values in the device. **c**, Typical transfer curve of n-type FET with non-ideal interfaces. The large hysteresis, large threshold voltage shift, and subthreshold swing value much higher than 60 mV/dec are caused by interface defects. The high current at the y-axis intercept indicates substantial electron doping from defects and dielectric. The presence of defects leads to low FET mobility as indicated by the small slope at high gate voltage region (the red dashed circle in linear transfer curve is typically used to extract the mobility). **d**, Schematic of an ideal 2D TMD semiconductor/dielectric interface with minimal defects and interactions due to the presence of a van der Waals gap between the two materials. **e**, Energy band diagram of a semiconductor/dielectric interface under thermal equilibrium without interfacial interactions. **f**, Ideal transfer characteristics of a n-type FET showing high ON current, high mobility, no hysteresis, low subthreshold swing, and small positive threshold voltage. χ_s, electron affinity of the semiconductor; χ_i, electron affinity of the dielectric; E_C, conduction band energy of the semiconductor; E_F, energy of the Fermi level; E_V, valence band energy of the semiconductor; q, charge; SS, subthreshold swing; V_{th}, subthreshold voltage.

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Y.W. and M.C. wrote and edited the paper. S. S. and H. Y. contributed to the contact and dielectric studies. All authors commented on the final version of the manuscript.

Competing interests

The authors declare no competing interests.