# Investigation of Threshold Voltage Instability in Normally Off GaN on Si HEMT


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*To my kids and wife*
*Dheerann, Thamilinie and Manimozhi*

*To my parents*
*Murukesan and Girija*

*To my friends*
*Dr. Karthikayan, Dr.Venkat (late) and Raja Rajan*

*“கற்றது கைமண் அளவு, கல்லாதது உலகளவு”*

- *ஔவையார், தனிப்பாடல்*

*“Known is the amount of sand in the fist, unknown is the total sand in the world”*

- *Avvaiyar, Thanipadal, 12th Century, CE*

# Declaration

This thesis is the result of my own work and includes nothing which is the outcome of work done in collaboration except as declared in the preface and specified in the text. It is not substantially the same as any work that has already been submitted, or is being concurrently submitted, for any degree, diploma or other qualification at the University of Cambridge or any other University or similar institution except as declared in the preface and specified in the text. It does not exceed the prescribed word limit for the relevant Degree Committee.

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# Abstract

Wide bandgap semiconductor by virtue of its high critical electric field, low intrinsic carrier concentration, high thermal conductivity is considered a promising material for enabling high density power conversion systems with a smaller form factor. Gallium Nitride (GaN) in particular, with its ability to form heterointerfaces naturally forms a high mobility 2-dimensional electron gas (2-DEG) at hetero interfaces like AlGaN/GaN making it an apt candidate for making power devices with lower on state resistance and higher frequency of operation. With the recent advances in epitaxial growth of GaN on Silicon (Si) substrates, AlGaN/GaN on Si High Electron Mobility Transistors (HEMT) have gained unprecedented commercial attention. Normally off HEMT devices are essential to design robust power systems. Of the various normally off HEMT architectures p- GaN HEMT has significant traction. Despite the advancements, reliability of HEMTs remains a challenge. Significant work has been done in the recent few years to mitigate reliability issues like Dynamic on resistance (D-$R_{ON}$), by continuously improving the quality of the GaN buffer and transition layers. However, threshold voltage instability exists as a key reliability issue which is not well understood. In this thesis, we investigate on threshold voltage instability of normally off 600-650V p-GaN AlGaN/GaN on Si HEMT.

This thesis aims to advance the physical understanding of the threshold voltage ($V_{TH}$) instability arising during the $V_{TH}$ measurement, nominal ON state and OFF state stresses by novel measurement techniques and a comprehensive TCAD modelling.

This thesis starts by analytically understanding the design parameters across the gate stack which have a significant control on the threshold voltage ($V_{TH}$). The measurement induced $V_{TH}$ instability is quantified for the first time and the best practices to mitigate them are proposed. Physical models explaining the instability mechanism are proposed and validated using detailed TCAD simulations. The effect of Schottky gate and ohmic gate contacts on the $V_{TH}$ instability and the challenges in making reliable measurements of $V_{TH}$ are summarised. Subsequently the nominal ON state, OFF state stress induced effect on threshold voltage is studied in detail. It has been shown that OFF state stress voltages (600V) at the drain terminal creates a dynamic threshold voltage in addition

to creating a D-$R_{ON}$. The physical mechanisms behind the OFF-state stress induced dynamic threshold voltage are proposed and validated using TCAD simulations.

Threshold voltage is a key parameter for the designer to design power systems and its instability is a crucial issue. The implications of the $V_{TH}$ instability at the system level are reviewed and a technique to extract the recovery time of the threshold voltage, post instability is developed.

This thesis investigates and advances the science around the threshold voltage instability of the normally off p-GaN AlGaN /GaN on Si HEMT. In summary, this work has quantified the measurement induced $V_{TH}$ instability and addressed the challenges of the $V_{TH}$ measurement in the Ohmic/Schottky type p-GaN gate with detailed TCAD analysis. This work also demonstrates the existence of the OFF-state stress induced dynamic threshold voltage with TCAD validated physical models. In addition to the above this work also showcases a novel measurement technique to extract the recovery time post threshold voltage instability.

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**List of commom acronyms**

| | |
|---|---|
| 2-DEG | Two Dimensional Electron Gas |
| 2-DHG | Two Dimensional Hole Gas |
| AlGaN | Aluminum Gallium Nitride |
| AlN | Aluminum Nitride |
| DUT | Device Under Test |
| GaN | Gallium Nitride |
| GIT | Gate Injection Transistor |
| HEMT | High Electron Mobility Transistor |
| IGBT | Insulating Gate Bipolar Transistor |
| MOSFET | Metal Oxide Semiconductor Field Effect Transistor |
| Si | Silicon |
| Mg. | Magnesium |
| SiC | Silicon Carbide |
| SMU | Source Measure Unit |
| TCAD | Technology Computer Aided Design |
| CMOS | Complementary Metal Oxide Semiconductor |

# 1. Introduction

*This chapter describes the overview of the field of power microelectronics, the history of power device development, their ideal characteristics, and the potential of the wide bandgap semiconductors. The chapter also summarises the characteristics of an ideal power switch and the features which make GaN HEMT an ideal power switch. GaN HEMT's application scenario and present industry penetration is summarised. An outline of this thesis, research problem being addressed is also included*

## 1.1 IC industry overview and scope of power IC

Silicon has been the work horse behind the electronic industry's growth story since the invention of the integrated circuit (IC) in 1958. The invention of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) [1] and the evolution of Complementary Metal Oxide Semiconductor (CMOS) silicon design brought in great value in terms of performance in the computation, telecommunication Industries. Driven by continuous improvements in technology, growth in demand, innovation in end user applications, semiconductors were instrumental in the industrial transformation across various domains and today it has grown to a 500 billion $ industry dominated mainly by silicon. The Moore's law [2], a prediction made by Intel founder Gordon Moore in 1965 that the number of transistors in the integrated circuit doubles every 2 years set the trend for scaling of transistors which made smart, life changing computing devices reality today. The aggressive scaling of the transistors have become increasingly difficult in memories & microprocessors now [3] and price/transistor is no more reducing with control gate dimensions reaching 2 nm (1nm = $10^{-9}$m). With this being the case value, addition to microelectronic systems based on *"more than Moore"* approach is seen as a viable path and has gained significant traction. In *more than Moore* approach emphasis is laid on 3D integration, integrating efficient power management electronic-systems, RF devices, biosensors, and Micro Electromechanical systems (MEMS) into CMOS based speciality technologies, thereby adding value by cost and operation. Power management electronics play a pivotal role in improving operating efficiency of systems spanning wide range of applications as shown in *Figure* 1.1. The focus of this work will be CMOS compatible power integrated circuits (IC) which

regulate power in applications (20V to 800V) like display drivers, variable speed drives, automotive to mention a few. In the recent times high efficiency power ICs are based on switched mode electronics with a power switching device being a core component as explained later in chapter 1.2.

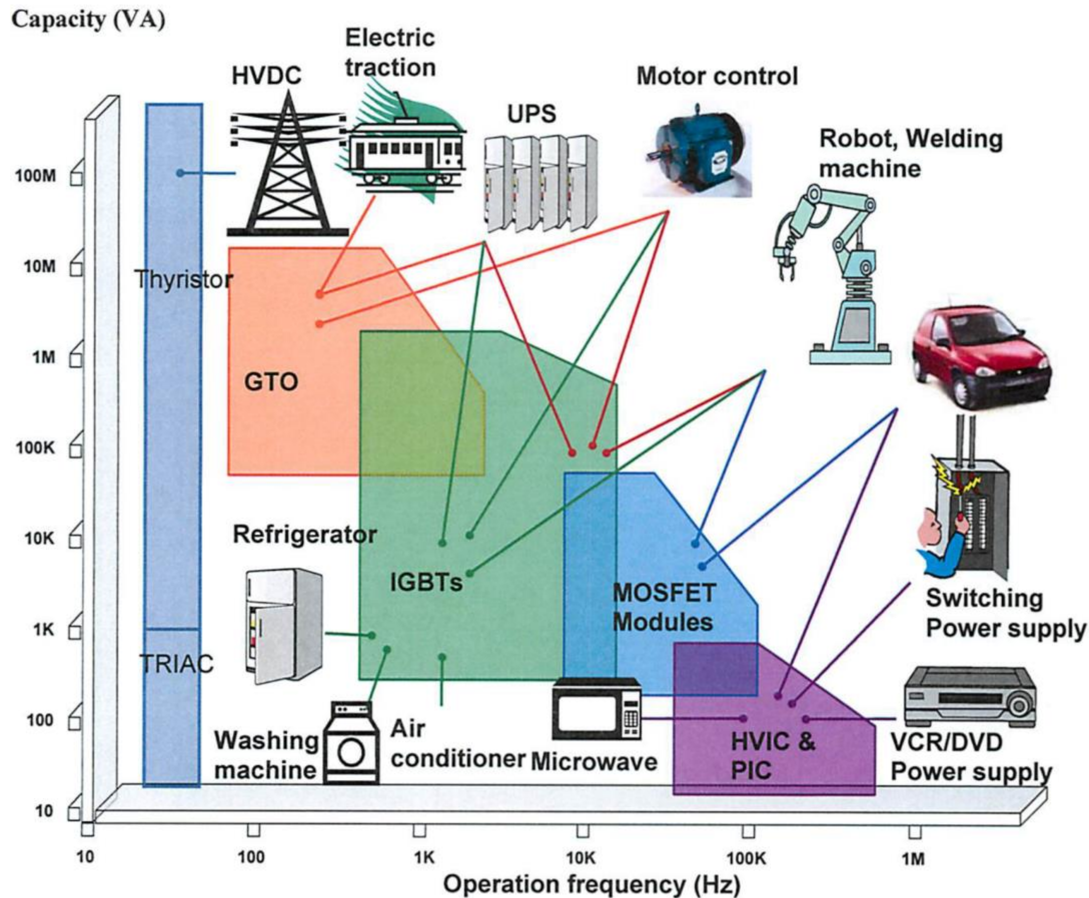



*Figure 1.1: Various application scenarios for power management electronics and devices [4]*

### 1.2 Switched mode power electronics and significance of power device

Power electronics play a vital role in efficient conversion, control and conditioning of electrical energy from generation to the point of load. The purpose of the power management block in a microelectronic system or a system on chip or a large-scale electrical machine is to process the voltage, current, frequency and phase(s) into specific forms which are optimal to the load. Power conversion systems have become ubiquitous in the modern industrial and consumer products offering point of load regulation for various circuit subsystems. Front end AC-DC converters, multiple DC- DC converters

are key components which provide the required point of load voltage, current to the output circuits.

The main component of the power electronics block are one or more power electronic device switches designed to switch high voltages and high current [4]. With the adoption of the switch mode power electronics and migration from the linear mode power electronics, power system components have become smaller, efficient and reliable.

An AC-DC switch mode power converter is reviewed for better understanding. The AC-DC power electronic converter shown in *Figure* 1.2 exemplifies the use of power devices as switches to dramatically increase the efficiency of the system while also considerably reducing its size. The signal from the utility supply which is of the line frequency (50 or 60 Hz) is first rectified and filtered to obtain a high DC voltage $V_D$. The DC voltage is then converted back into AC form by switching the transistor ON/OFF at higher frequencies (~100KHz). This allows the use of high frequency transformer which is compact, less bulky to step up/down the voltage and the discrete power switching transistor is placed at the primary of the transformer thereby seeing a high voltage (in OFF state) and a lower current in the ON state (when compared to the output current). For a 240V RMS voltage coming from the utility supply the transistor needs to have a breakdown more than 600V to account for large transient peaks that develop during switching from ON to OFF state. Since the transistor operates ON/OFF with relatively low losses the efficiency of the system can be dramatically improved from 30-40% (linear mode electronics) to 80-90% (switched mode electronics). The output voltage of the switched mode power electronics converter is given in equation 1.1

$$V_{out} = \frac{\mathrm{N2}}{\mathrm{N1}} * V_d * \frac{\mathrm{Ton}}{\mathrm{Ts}} \qquad 1.1$$

Where N2 is the number of turns of the secondary of the transformer and N1 is the number of turns of the primary of the transformer. Ton/Ts is the duty cycle of the switch. Thus, by varying the duty cycle, the DC output could be effectively controlled. In linear mode power electronics, the utility supply is stepped up/down using a large

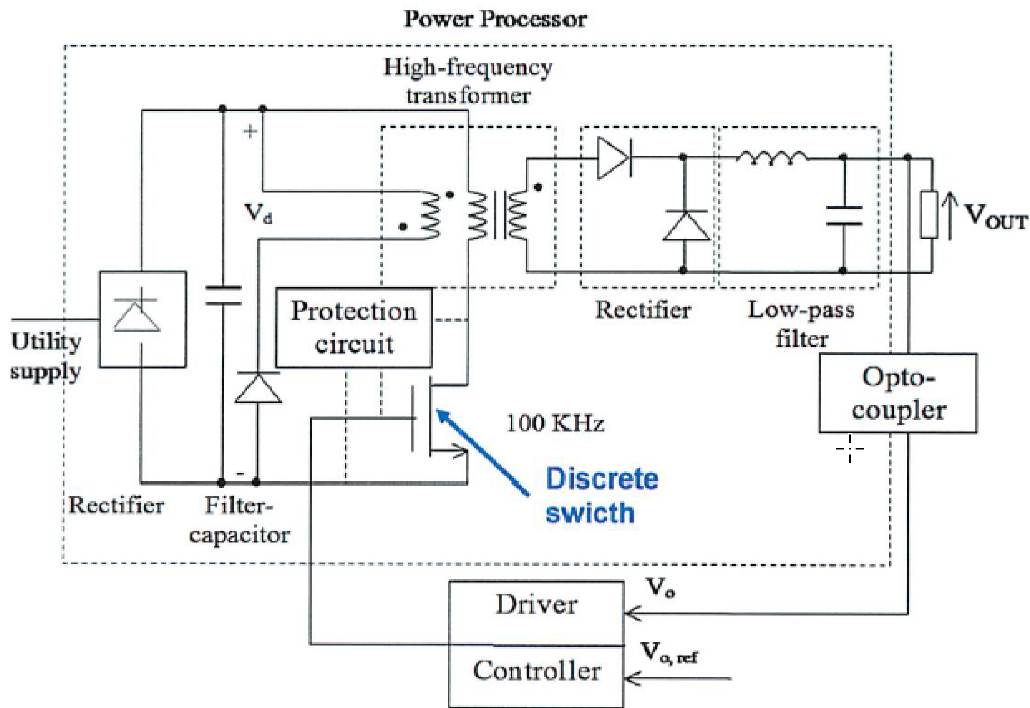



*Figure 1.2: AC-DC switch mode power electronics converter [4]*

bulkier lossy line frequency (50 or 60Hz) transformer and then the secondary output of the transformer is rectified and filtered to DC as shown in *Figure* 1.3. The transistor used in common base configuration absorbs the voltage difference between Vo and Vd and behaves like a controlled resistor. In this configuration the transistor leads to a lot of power dissipation as the current flowing from collector to emitter is very high. The discrete power switching device which switches at higher frequency in the switch mode power electronics as marked in *Figure* 1.2 plays a pivotal role in adding improvement in terms of efficiency, power dissipation, form factor reduction, effective output control and thus forms the heart of the power electronics block.

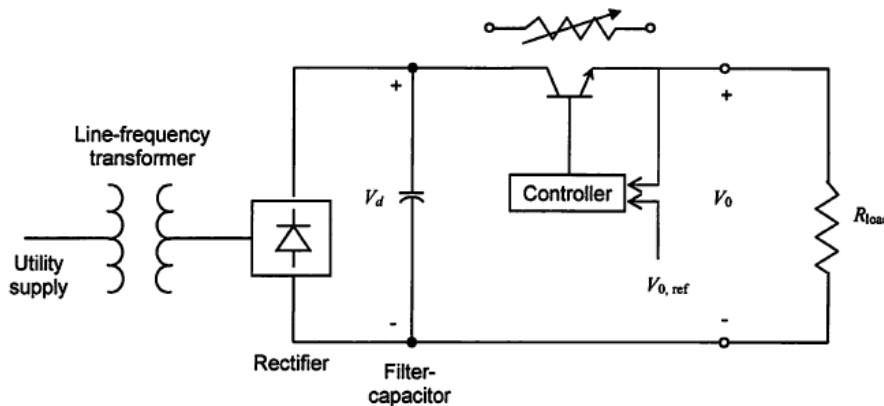



*Figure 1.3: AC-DC linear mode power electronics converter [4]*

Significant research efforts have been put to engineer these power semiconductor devices to work as an efficient power switch with reduced form factor, high frequency response, lower leakage, high temperature performance and more functionality integration.

## 1.3 History of power device development

With power semiconductor switches having paramount importance in deciding the efficiency of power microelectronics block it is worthwhile to know their history of development. Power semiconductor devices have its historical roots in the invention of the bipolar transistor in the late 1940s with the main specific contribution from Hall in 1952 when he reported the first 200V/35A power rectifier based on germanium mesa alloy [5]. However, germanium had a short life in the field of semiconductors, and silicon (Si) had established its place by late 1950s with the introduction of diffused deep junctions suitable for high voltage blocking. With the advancement in process technology and ability to form deep diffused junctions in silicon, Moll et al. in 1956 proposed the thyristor concept, the first power device that was capable of handling concomitantly high voltages and high currents. This was followed by the development of the Gate-Turn-Off thyristor (GTO) in 1961, the first device with a control gate terminal. The power Metal-Oxide-Semiconductor Field Effect-Transistor (MOSFET) was commercially introduced in the 1970s [6]. Because of its high input impedance and voltage control, the complexity and the cost of its driving circuit was drastically reduced. However, power MOSFETs are majority carrier devices and, therefore, their on-state performance is limited by the blocking ability, which in turn is given by the thickness and the doping of the drift region. The need for a device with higher current capability, lower conduction losses while still maintaining the high impedance control to cover a wide variety of applications (between those addressed by the power MOSFET and those addressed by the thyristor) led to the invention of the Insulated-Gate Bipolar Transistors (IGBTs) [7], also known previously as the Conductivity-Modulated Field-Effect Transistors (COMFETs)[8].

The IGBT combines the bipolar transport in the drift region with the MOSFET gate control. Moreover, it has a significantly lower on-state voltage drop than power MOSFETs and offers a relatively high switching speed when compared to thyristors.

IGBTs are commonly adopted for medium to high voltage applications, typically ranging from 600V – 3kV. At voltages beyond 3kV thermal management in IGBTs become challenging and at voltages lower than 600V, with higher switching frequency requirement, MOSFETs are faster than IGBTs.

In 1998, the first super junction concept were reported in literature[9] and comes in several forms [10] with different technological approaches for different uses. The super junction structure is based on an optimised drift region with highly doped pillars of n and p type with equal doping charge commonly referred to as the principle of charge compensation. The depletion region extends in two dimensions and the whole drift region becomes depleted at lower reverse voltages than in a standard power MOSFET, despite the increased doping levels in the pillars. The increased doping in the n pillar serves to reduce the on-state resistance.

Alongside the development of vertical discrete devices, another class of devices called lateral devices have received considerable attention. Lateral devices enable monolithic integration of the discrete power devices with its gate drive circuit, mixed signal devices, micro electromechanical systems (MEMS) etc., with proper termination designs enabling the development of monolithic integrated circuits with power, analog, mixed signal and sensing functions. Presently, the Lateral Double-diffused Metal-Oxide- Semiconductor (LDMOS) for low power applications and the lateral IGBT (LIGBT) for relatively higher power are incorporated in power integrated circuits. Today, these devices are available in specialised foundry processes such as High Voltage (HV) Bipolar CMOS DMOS (BCD) technology. Power semiconductor devices using materials with bandgap energies larger than in Si for improved performance have been proposed in 1990s [11].

### 1.4 Ideal power device and its design trade off

For the development of the improved power switching devices based on wide bandgap semiconductors such as GaN, it is essential to understand the key performance indices that determine the efficiency of operation of these devices as switches. CMOS compatible GaN on Si lateral power devices being the focus in this thesis, the parameters discussed herein correspond to the lateral power devices with an approximate equivalent circuit as shown in *Figure* 1.4. (a.) For efficient switching the losses of these

power devices should be minimal. The losses associated with discrete power semiconductor switch could be classified as

a) Static losses (On state losses + Off state losses)
b) Switching losses (Turn on and turn off losses)

On state losses are the losses incurred when the power transistor is ON typically operating in its saturation regime and is given by $I^2 R_{DS(ON)}$ where $R_{DS(ON)}$ is on-state resistance. Off state losses are the losses incurred when the power transistor is OFF and is largely dependent on the off-state leakage currents $I_{GSS}$, $I_{DSS}$ as defined in *Table 1* respectively. For higher operational efficiency of the switch, static losses should be minimal requiring smaller $R_{DS(ON)}$, $I_{GSS}$, $I_{DSS}$. Off state losses are generally negligible compared to the on-state losses. The critical parameters which control the static losses are defined in *Table 1* [12]. These parameters are extracted from the static characteristics such as Transfer characteristic measurement and output characteristic measurement.

*Table 1: Key parameters from the Static characteristics of lateral power MOSFET*

| **Characteristic** | **Symbol** | **Unit** | **Description** |
|---|---|---|---|
| Gate leakage current | $I_{GSS}$ | uA | The leakage current that occurs at a specified voltage across gate and source with drain and source short circuited |
| Drain cut-off current | $I_{DSS}$ | uA | The leakage current that occurs when a voltage is applied across drain and source with gate and source short-circuited |
| Drain source breakdown voltage | $V_{DSS}$ | V | The maximum voltage that the device will block between drain and source when the device is in OFF state |
| Gate threshold voltage | $V_{TH}$ | V | Threshold voltage is the voltage across the gate at which channel is formed and current flows between source and drain to a certain specified level |
| Drain source on resistance | $R_{DS(ON)}$ | Ω | The resistance across drain and source when the MOSFET is in the ON state |
| Transconductance | Gm | S | Ratio of the drain current variation at the output to the gate voltage variation at the input and is defined as Gm=$\Delta ID / \Delta VG$. It indicates the sensitivity or the amplification factor of power MOSFET |

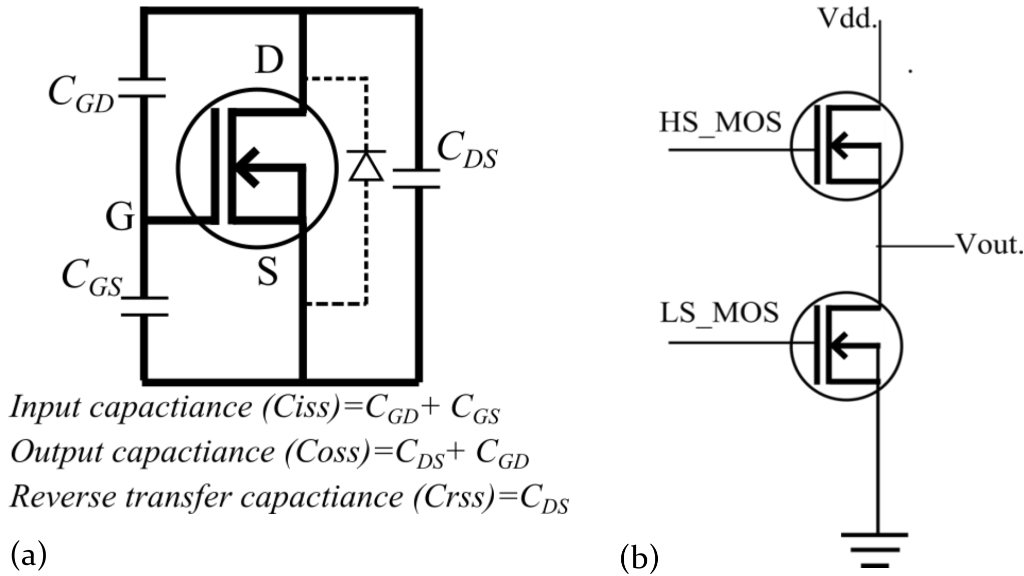



*Figure 1.4: (a) Equivalent circuit of a lateral 3 terminal (Source – S, Drain – D, Gate – G) power MOSFET showing the internal integral body diode (not present in GaN HEMT) and the capacitances. (b) A half bridge converter showing a high side power MOS and a low side MOS with an input voltage Vdd and output voltage Vout*

Switching losses are governed by the dynamic transient characteristics of the power device. The dynamic behaviour depends on the intrinsic resistance, capacitance which could be segmented as gate to source capacitance ($C_{GS}$), gate to drain capacitance ($C_{GD}$) and drain to source capacitance ($C_{DS}$) as shown in equivalent circuit *Figure* 1.4 *a).* Switching losses depends on the input capacitances ($C_{iss}$ = $C_{GS}$ + $C_{GD}$), output capacitances ($C_{oss}$ = $C_{DS}$ + $C_{GD}$), reverse transfer capacitances ($C_{rss}$ =$C_{DS}$)., its associated delay ($T_d$), rise ($T_r$), fall ($T_f$) times during the turning on and turning off the switch. Based on the charged based model [13] $C_{iss}$, $C_{oss}$, $C_{rss}$ is given by $\frac{\delta Qg}{\delta V_{GS}}$ , $\frac{\delta Qd}{\delta V_{DS}}$ , $\frac{\delta Qg}{\delta V_{DS}}$ respectively where $Q_g$ is the gate charge and $Q_d$ is the drain charge.

To understand the switching losses and the correlation to the capacitances, the turn on and turn off transition of a GaN HEMT, while being used in a half bridge application (Figure 1.4 (b)) is examined. The turn on switching period typically has 4 intervals P1 – delay period ($t_0$-$t_1$), P2 - $\frac{di}{dt}$ period ($t_1$-$t_2$), P3 - $\frac{dv}{dt}$ period ($t_2$-$t_3$), P4 - remaining switching period ($t_3$-$t_4$) as shown in Figure 1.5. At '$t_o$' gate current ($I_G$) starts to charge $C_{iss}$ exponentially and $V_{GS}$ reaches threshold $V_{G(TH)}$ at $t_1$. In the delay period (P1) when

$V_{GS} < V_{G(TH)}$ the channel (2-DEG) is not formed and $C_{iss}$ is low resulting in lower delay time (P1).

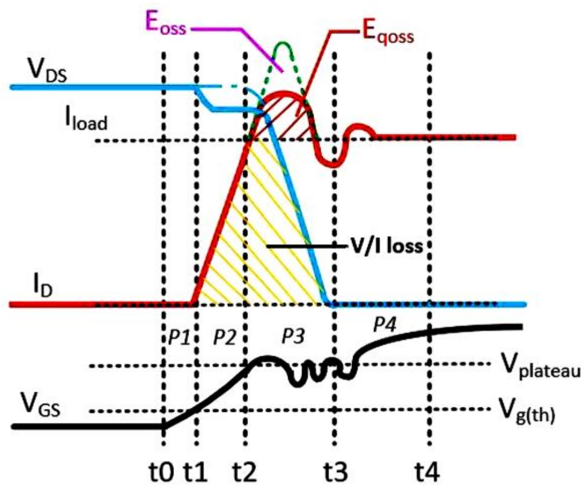



*Figure 1.5: Turn on transition of a GaN HEMT while hard switching in a half bridge [14]*

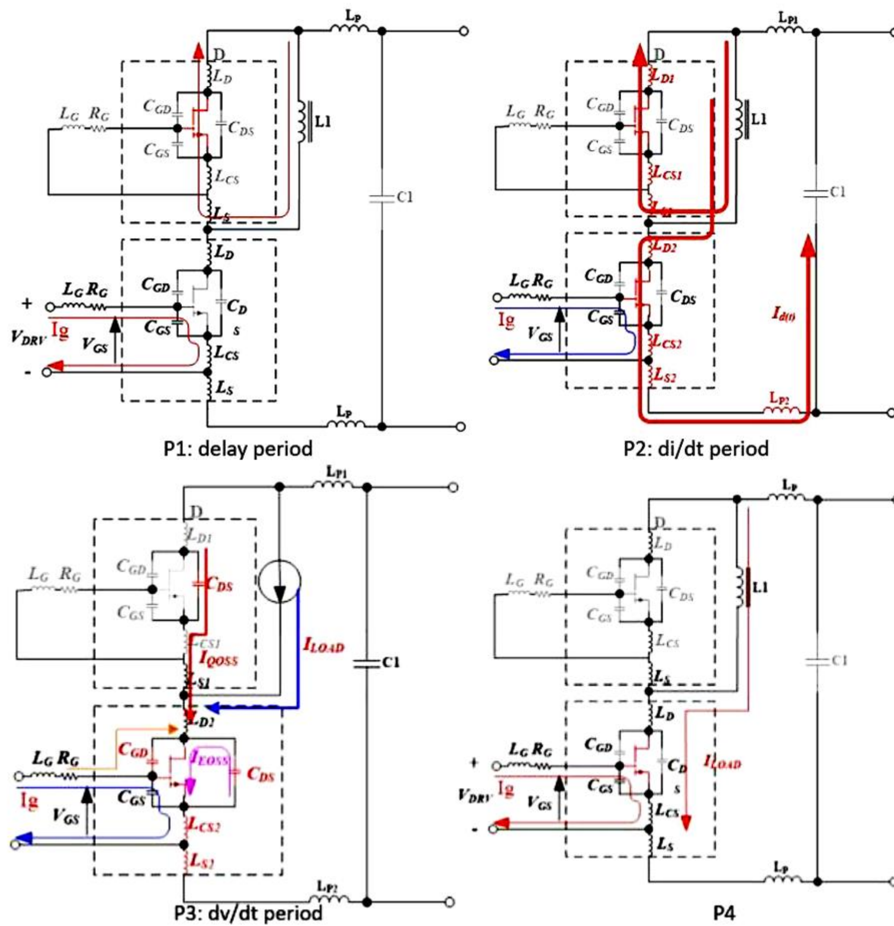



*Figure 1.6: Detailed turn on process of a GaN HEMT through 4 periods P1 to P4 while hard switching in half bridge [14]*

In the P2 period($t_1$-$t_2$) when $V_{GS} > V_{G(TH)}$ as channel is formed, $I_D$ quickly reaches load current, during this period the device operates in saturation region generating V/I overlapping switching loss ($E_{VION}$) as shown in Figure 1.5. The miller plateau voltage ($V_{plat}$) is given by $V_{plat} = V_{G(TH)} + I_D/g_m$, where gm is the transconductance and $V_{G(TH)}$ is the threshold voltage. $V_{plat}$ should be lower so that it takes lower time to reach $V_{plat}$ thereby reducing the overlapping switching loss in P2, this could be achieved by increasing the transconductance. In the P3 period (t2-t3) the output capacitance $C_{oss}$ of the low side GaN HEMT begins to discharge through channel ($E_{oss}$ loss), meanwhile $I_D$ charges the $C_{oss}$ ($E_{Qoss}$ loss) of the high side GaN HEMT (Figure 1.6) and $V_{DS}$ starts to fall. This region also generates V/I overlapping switching losses ($E_{VION}$). The period of the miller plateau voltage given by $t_{plat} = Q_{GD}/I_G$ predominantly controls the overlapping switching loss in P3. To minimise this the gate to drain charge ($Q_{GD}$) should be small and the gate drive current (Ig) should be high. Thus the total turn on switching loss is given by equation 1.2

$$Eon = E_{VION} + E_{Qoss} + E_{oss} \quad 1.2$$

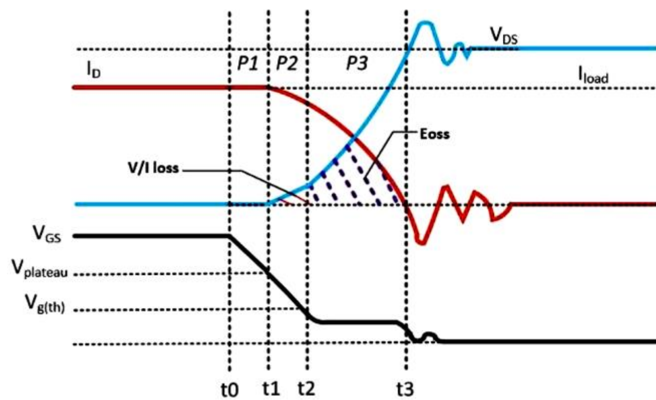



*Figure 1.7: Turn off transient of a GaN HEMT while switching in a half bridge [14]*

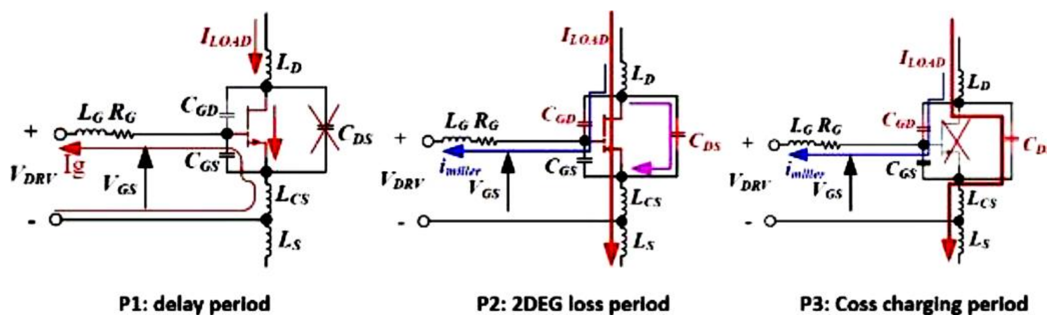



*Figure 1.8: Detailed turn on process of GaN HEMT through 3 periods P1 to P3 while hard switching in half bridge [14]*

Where $E_{VION}$ is the energy lost due to the V/I overlapping, $E_{Qoss}$ is the energy lost due to the charging of the output capacitance $C_{oss}$ and $E_{oss}$ is the energy lost due to the discharging of the output capacitance $C_{oss.}$ In a similar way the turn-off process includes 3 intervals P1- delay period, P2- 2-DEG loss period and P3-$C_{oss}$ charging period as shown in Figure 1.7. In the delay period (P1) the $I_G$ starts to discharge the input capacitance $C_{iss}$ exponentially, the load current flows through the channel (2-DEG) and there is no current flowing into output capacitance Coss as shown in Figure 1.8. At 't2', $V_{GS}$ drops to threshold voltage $V_{GS(TH)},$ and channel of GaN-HEMT turns off. In this period, with increasing impedance of channel, drain current $I_D$ starts to redirect into Coss. Most loss in this P2 region is V/I overlapping switching loss $E_{VIoff}$. From t2 gate-to-source voltage $V_{GS}$ drops below threshold voltage $V_{GS(TH)}$, the 2-DEG is turned off completely, and all the load current is charging $C_{oss}$ as shown in Figure 1.8. The turn off slew rate dv/dt is defined by the load current and the energy lost during the charging of $C_{oss,}$ $E_{oss}$ is only dissipated at the next turn on process. Thus, the total turn off switching loss is given by

$$E_{off} = E_{VIoff} + E_{oss} \qquad 1.3$$

From the turn on and turn off switching loss analysis it is evident how capacitances play a crucial role in switching losses. For higher operational efficiency of the switch, switching losses should be minimal requiring nominally smaller $C_{iss,}$ $C_{oss,}$ $C_{rss.}$ These parameters are extracted from the dynamic or switching characteristics of the MOSFET and are defined in *Table 2*. These metrics extracted from the dynamic characteristics of the lateral power MOSFET are generally provided by the manufacturer in the data sheet of a discrete power device switch enabling the circuit designer to carefully co- design circuits to develop a robust high-performance design.

*Table 2: Dynamic characteristics of lateral power MOSFET*

| Characteristic | Symbol | Unit | Description and system benefit |
|---|---|---|---|
| Capacitance | Ciss<br>Crss<br>Coss | pF | Ciss is the input capacitance, Crss is the reverse transfer capacitance and Coss is the output capacitance and affect the switching performance of a POWER MOSFET |
| Effective output capacitance | Coss | pF | Effective output capacitance is calculated from the $E_{oss}$, which is needed to charge $C_{oss}$ |
| Gate resistance | $R_G$ | Ω | The internal gate resistance of the MOSFET |

The desirable characteristics of a power switch for building efficient, high power density systems are

a) Lower on resistance ($R_{DS(ON)}$) – ON state conduction losses are minimal.
b) Lower leakage currents ($I_{DSS}$ & $I_{GSS}$) – OFF state losses are minimal.
c) Lower gate charge for faster switching enabling high frequency operation and lower switching losses
d) Lower capacitances (Ciss, Coss, Crss) enable faster switching, lower losses associated with charging and discharging of the power FETs which translates to a lower power requirement from the driving circuit.
e) Faster (larger dv/dt, di/dt) switching – switching losses are minimal
f) Larger transconductance is desirable to get a high current handling capability at a lower gate drive voltage and for achieving higher frequency response.

The principal design trade – off in lateral power device is between the $R_{DS(ON)}$ and blocking voltage (BV). The on-state resistance $R_{DS(ON)}$ of the lateral power device is the resistance for the flow of unipolar carriers between the drain and source terminals after the conducting channel is established. The blocking voltage or the breakdown voltage of the lateral power device is the maximum voltage that the device could block across the drain and the source terminals. Beyond the breakdown voltage, the peak electric field across the P-i-N junction (drift region) supporting the high voltage reaches the critical value of the material limit, leading to impact ionisation followed by avalanche breakdown as shown in Figure 1.9.

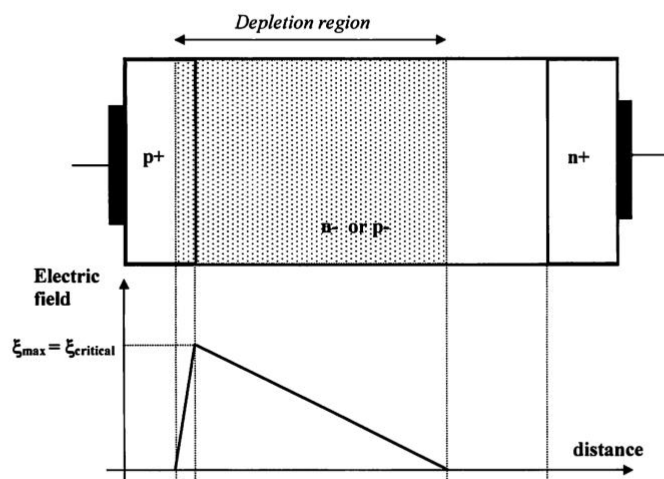



*Figure 1.9: Electric field profile in a PIN junction to demonstrate blocking mode action[15]*

The on-state resistance is comprised of two main components: the channel resistance and the drift resistance. The channel resistance is less significant relative to the drift resistance for high voltage devices (> 600 V). Therefore, with increasing voltage rating the drift resistance tends to dominate the on-state resistance. The specific drift resistance is given by the drift of electrons through the n- drift layer and is given by

$$R_{specific\text{-}drift} = \frac{W_d}{q*\mu*N_d} \qquad 1.4$$

Where $W_d$ is the width of the depletion region, q is the charge of the electron, μ is the mobility of electron, $N_d$ is the doping density of the n- drift region. The power MOSFET typically employs a non-punch through design as in Figure 1.9 where the electric field at breakdown potential ($V_{BR}$) should just touch the n+ drain contact region. Therefore, the drift width $W_d$ should equate to $W_{critical.}$ Applying Poisons equation in the p-i-n junction

$$V_{BR} = \frac{\varepsilon_r\,\varepsilon_0\xi^2_{critical}}{2qN_d};\;\; W_{critical} = \frac{2V_{BR}}{\xi_{critical}} \qquad 1.5$$

From equation 1.5 it is evident that to increase breakdown the drift region width has to be increased and from equation 1.4 it is evident that the $R_{DS(ON)}$ will increase with increase in the drift region. In addition to that with the larger drift region, the area of the associated input and output capacitances increase causing an increase in corresponding switching losses. For a higher blocking voltage, the lightly doped drift region must be extended so that the PIN junction across the source and the drain terminal could withstand higher blocking voltage however this would lead to an increased $R_{DS(ON)}$ and hence an increased conduction loss which is a key design trade off. The critical electric field is the intrinsic property of the material when increases reduces the on-state resistance quadratically. This leads to the quest for materials with higher critical electric field and wide band gap semiconductors by virtue of fitting intrinsic properties can have thinner drift regions.

### 1.5 Wide bandgap semiconductors and GaN's potential as power device

Wide band gap semiconductors possess intrinsic properties like

a) Larger bandgap energy
b) Larger critical electric field.

c) Higher thermal conductivity

d) Good saturation velocity

which make them a promising candidate for high power and high frequency applications. The energy required by an electron to jump from the highest part of the valence band to the lowest part of the conduction band is the energy bandgap of a semiconductor. While the Silicon has an energy bandgap of 1.1 electron volt (eV), materials with more than 2 eV of energy are known as Wide Bandgap (WBG) materials. The high critical electrical field of wide bandgap (WBG) semiconductor enables thinner and heavily doped drift region which leads to a much lower on-resistance than that of equivalent Si devices rated for the same voltage [16]. With larger band gap the intrinsic carrier concentration is lower leading to low levels of leakage current. Another advantage of wide bandgap material is the thermal expansion coefficient (CTE) which is better matched to the ceramics used today in the power device packaging technology [17] which results in higher reliability in the thermal cycles. During operation the channel can reach several hundred degrees above ambient temperature causing self-heating and degradation, high thermal conductivity of WBG materials enable the transfer of heat generated in the channel through the substrate hence needing lower cooling [18]. Formation of 2-dimensional electron gas by GaN heterostructures lead to a higher mobility channel which allow higher switching frequency which in turn lead to smaller passive components and hence smaller overall form factor. By virtue of these superior properties, the power systems built with wide band gap semiconductor-based devices will be efficient, smaller, and lighter with low cooling demands. For e.g., PN junctions based on WBG can operate at higher temperatures requiring low cooling requirements and the high electron mobility in the channel leads to the lower on resistance and higher frequency of operation. Lower intrinsic carrier concentration leads to lower off state leakage currents. Thus, the static losses driven by ON state and OFF state losses are significantly smaller. For the given voltage rating the area of the wide band gap-based device is much smaller than the Si counterpart causing the associated Ciss, Coss, Crss to be smaller. Smaller source, drain and gate capacitances alongside higher channel mobility enable smaller gate charge, larger dv/dt switching, larger transconductance, those features required for an ideal power switch as detailed

in *chapter 1.4*. B-FOM, Baliga figure of merit ($\varepsilon * \mu * \xi c^3$) given by product of the permittivity, electron mobility, cube of critical electric field is a useful parameter to compare different materials. BFOM [19] assumes that in a power device the losses are solely arising due to the on-state conduction losses and hence applies best for low frequency operation. The properties of the wide bandgap semiconductors [20][21] commonly considered for power devices is bench marked with silicon as summarised in *Table 3*.

*Table 3: Intrinsic properties of wide bandgap semiconductors in comparison with silicon [5]*

| Parameter | Symbol / unit | Si | GaN | 4H-SiC | Diamond |
|---|---|---|---|---|---|
| Bandgap | Eg (eV) | 1.1 | 3.4 | 3.26 | 5.47 |
| Critical electric field | $\xi c$ ($10^6$ V/cm) | 0.3 | 3.3 | 3 | 5.6 |
| Electron Mobility | $\mu_n$ ($cm^2$/Vs) | 1400 | $800^B$/1700 | 950 | 1800 |
| Intrinsic career concentration | $n_i$ ($cm^{-3}$) | $1*10^{10}$ | $2*10^{-10}$ | $8*10^{-9}$ | $1*10^{-20}$ |
| Saturation velocity | ($10^7$ cm/s) | 1 | 2.5 | 2 | 2.7 |
| Thermal conductivity | (W/cmK) | 1.5 | 1.3 | 4.5 | 20 |
| BFOM relative to Si | - | 1 | $1300^B$/2700 | 500 | 9000 |

B - Significant differences exist between bulk(B) and 2-DEG in GaN heterostructures

As observed in *Table 3*, GaN, SiC have bandgap energy 3 times higher than that of the Si and diamond have bandgap 5 times higher than that of Si. Critical electric field follows a similar trend as band gap and intrinsic carrier concentration follows an inverse trend as band gap as expected. GaN, Diamond based devices have higher electron mobility in channel relative to silicon making it suitable for high frequency applications. Whereas the mobility of SiC based devices is lowest making it less suitable for high frequency applications. It is to be noted that in GaN, bulk mobility is almost half that of the 2-dimensional electron gas (2-DEG) mobility due to defects arising during the epitaxial growth of GaN, on the other hand 2-DEG is in quantum confined space with no defects. The formation of this 2-DEG has been a principal differentiating value proposition for GaN devices, the physics behind its formation will be discussed in detail in Chapter 2. GaN has a better BFOM relative to Si, SiC and diamond has the best BFOM in the table. Thermal conductivity of GaN is the least and diamond is the best among all. Though diamond theoretically has the best parameters, there has been difficulties in doping

diamond layers consistently due to the lack of shallow dopant species [22] causing bottlenecks in realising commercial grade manufacturable devices. Among these listed wide bandgap semiconductors GaN and SiC are the front runners which has the potential to displace silicon given its mature manufacturing processes and cost parity. Among the silicon carbide (SiC) devices, the Schottky diodes, the Junction FETs (JFETs) and the MOS- FET are seen as candidates for higher voltages and higher power levels. Devices such as High Electron Mobility Transistors (HEMTs) and variants of these devices are the most likely contenders in gallium nitride (GaN). Gallium Nitride by virtue of its intrinsic properties, by its ability to form heterojunctions (AlGaN/GaN) and by its ability to form a high mobility channel at AlGaN/GaN interface without doping makes it apt for making a power device with higher switching frequencies and better figure of merit than SiC for 100-600 V applications.

### 1.6 Gallium Nitride power device and potential applications

Lateral GaN HEMT devices are being explored to cater low voltage (< 200V), medium voltage (200-600V), high voltage (600 – 1000V) application segments and vertical configuration of GaN power devices are explored [23]to cater > 1 kV application segments. Though vertical GaN power devices provide an opportunity to increase the break down voltage and current handling capability by increasing the depth of the device without increasing the area of the device, due to the defects on the material the technology is not yet mature. Lateral GaN HEMT devices on the other hand are widely adopted with mature proven processes. Lateral GaN HEMT's 2-DEG high mobility channel at the AlGaN/GaN hetero interface enables lower Ron and its much smaller junction capacitances provide better figure of merit making it viable for high frequency applications. Unlike a MOSFET there is no p-n junction within the lateral structure of a GaN HEMT, the depletion of the 2-DEG supports the blocking mode and hence there is no body diode and associated reverse recovery charge (Qrr). Thus, absence of body diode in GaN HEMT eliminates the reverse recovery losses enabling high frequency switching[24]. The reverse conduction voltage of GaN HEMT is high as compared to Si MOSFET's body diode leading to slightly higher dead time loss due to the third quadrant freewheeling current. GaN HEMT as a power device have

a) Low hard switching losses

b) Low turn off losses (Good choice for high frequency soft switching topologies)

c) Higher dead time losses or a poor third quadrant operation

GaN HEMT devices can typically enhance system efficiency by 3% to 10%. According to Yole development report [25]. Replacing silicon devices by GaN devices can improve the DC-to-DC conversion efficiency from 85% to 95%, AC to DC conversion efficiency from 85% to 90%, DC to AC conversion efficiency from 96% to 99%. Improvement in efficiency decreases the energy wasted as heat resulting in lower cooling requirements. Power devices are typically used in the applications having voltage ranges of operation from 30V to 1.2 KV, GaN HEMTs are found to be a viable replacement of their silicon counterparts in the 100-200V and 600V application segments [26] with current capabilities generally below 60A. 100-200V application segment typically include the point of load applications i.e. DC – DC converters for the consumer electronic applications. 600V application segment include power factor correctors (PFC), uninterrupted power supplies (UPS), AC/DC converters, motor drives, photovoltaic system inverters, lighting applications. chargers, inverters, and converters to mention a few. With the significant interest in the hybrid electric vehicles and electrical vehicles and GaN HEMTs offering a fitting value proposition, the application scenario is investigated specifically. *Figure* 1.10 depicts the various power electronic converters where GaN HEMTs could offer value by high efficiency, high density, and lower weight by which the vehicle running mileage can be increased.

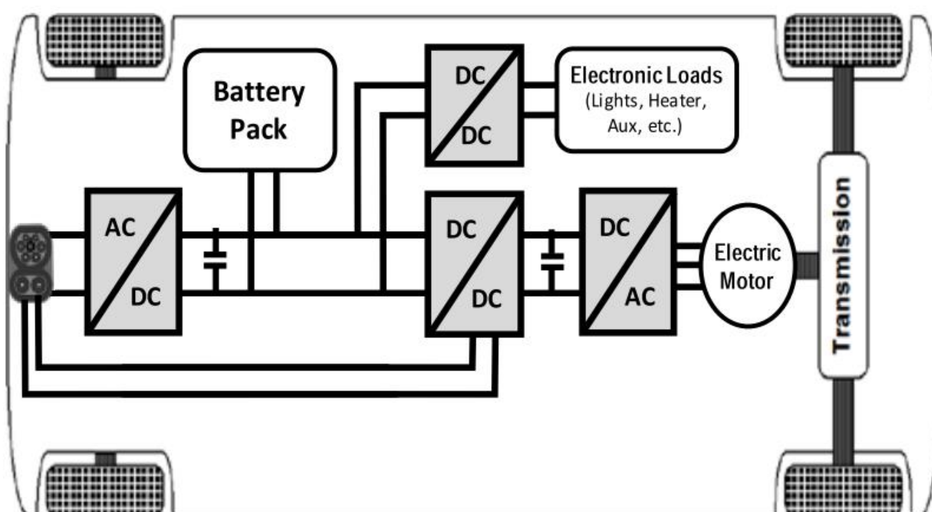



*Figure 1.10: Typical power electronic converters in electric vehicles where GaN can be employed [27]*

AC/DC stage  in *Figure* 1.10 is an onboard charger and for powering the propulsion subsystem including the electric motor  a three - phase traction inverter is needed for DC/AC conversion, a DC/DC boost converter is applied between on board charger and traction inverter to provide a controllable DC input voltage for the traction inverter. There is an additional isolated DC/DC converter to step down voltage for the low voltage electronic loads which is typically called the auxiliary power module. With the continuous efforts to improve the breakdown voltages and the current handling capabilities of GaN HEMTs by novel device architectures and parallelling GaN HETMs soon they will be able to penetrate the high voltage segment applications (1.2kV to 2kV) and high-power applications (sub 100 kW).

### 1.7 Challenges in GaN power devices

Despite the advantages of devices based on GaN, silicon devices have been dominating the industry due to its manufacturability, low cost, reliable high voltage operation and decades of design expertise enabling high density, high efficiency designs. Lateral HEMTs based on GaN on Si CMOS technology platform solved the manufacturability issue largely and provided the much-needed traction for industrial adoption. Currently the GaN on Si HEMTs are manufactured on 6 inch and 8-inch wafers with good yields. The key challenges of GaN power devices due under investigation are its

a) Normally OFF operation
b) Lower threshold voltage
c) Reliable high voltage operation
d) Reliable switching behaviour.

With the p-GaN gate normally OFF operation is enabled and with the continuous improvement of the controlled Mg doping, p-GaN gate is the leading normally OFF gate architecture. The other normally off architectures are discussed in 2.5. High threshold voltages typically > 2V is required to avoid parasitic turn on of the switch at higher temperatures. Despite multiple attempts [28][29][30] most of the monolithic devices available have threshold voltage in the range of 1.2 to 1.8V, though recent novel integrated commercial solutions claim higher threshold voltages. The nominal high voltage and switching operation induced reliability concerns in the AlGaN/GaN on Si HEMT switching circuits can be classified into

1) OFF state (Drain stress) induced reliability concerns
2) ON state (Gate stress) induced reliability concerns

Typically power integrated circuits operate in 10kHz causing an on time of 100µs. In the practical switching circuits, the drain has to endure long term OFF state voltages. The OFF-state blocking voltage across the Drain and source leads to dynamic on resistance which has been a serious reliability concern as the increase in $R_{DS(ON)}$ leads to lower drive currents at the given voltage leading to faulty operation of the power systems or increased losses leading to reduced efficiency. Dynamic $R_{DS(ON)}$ has been investigated in detail and understood to be caused by trapping of the channel 2 DEG electrons in the access region between gate and drain at the device surface[31] or/and by the bulk traps in the buffer/transition region [32] [33]. Improved passivation layers in the gate access region, continuous improvement of the buffer and transition regions over the past decade has kept the Dynamic $R_{DS(ON)}$ under control. By introducing a hole injection layer Dynamic $R_{DS(ON)}$ has been eliminated as reported in [34]. On the other hand, threshold voltage ($V_{TH}$) instability is a reliability issue which is of great interest in the recent times. It can lead to faulty turn on, power device breakdown, increased dead time losses, larger reverse conduction voltages explained in detail in chapter 2.7.1. Positive and negative $V_{TH}$ shifts have been reported by the gate stress during ON state operation. However, Threshold voltage instability arising during measurements, OFF state and for different gate contacts has not been investigated in detail which is the focus of this work and thesis.

### 1.8 Overview of the thesis

This thesis investigates the nominal operation induced threshold voltage instability in normally of p-GaN gate AlGaN/GaN on Si HEMT. Discussion spans on various topics ranging from novel measurements, physics of threshold voltage instability and advanced TCAD modelling.

Chapter 1 describes the overview of the field of power microelectronics, the history of power device development, their ideal characteristics, and the potential of the wide bandgap semiconductors. The chapter also summarises the characteristics of an

ideal power switch and why GaN HEMT would make an ideal power switch. GaN HEMTs application scenario and present industry penetration is also presented.

Chapter 2 describes the basics of the heterojunction physics observed in the heterostructures and explains the principle of 2-dimensional electron gas formation in the AlGaN/GaN heterostructure. The various normally off architectures of the AlGaN/GaN on Si HEMTs are reviewed and p-GaN architecture is reviewed in detail. The various reliability and operational challenges of p-GaN/AlGaN/GaN on Si HEMT and the implications of threshold voltage instability at the device and circuit level are reviewed.

Chapter 3 describes the sentaurus simulation work bench, the respective integrated models used in this thesis for simulating the normally off p-GaN AlGaN/GaN on Si HEMTs. Traps constitute a centric role in the reliability studies of HEMTs and the basics of traps, their physical understanding, and their means of modelling is also summarised.

Chapter 4 analyses the gate stack of the normally off p-GaN HEMT for a physical understanding of the underlying dynamic charge balance at various interfaces and henceforth the normally OFF operation. The analytical expression for the potential at which the channel turns on for p-GaN HEMTs is reviewed. The significance of the trapping mechanisms in the gate stack which causes charge conditions altering the threshold voltage is discussed.

Chapter 5 describes the challenges of the threshold voltage measurement in the normally off p-GaN HEMTs. The measurement procedure by itself induces an instability in the threshold voltage making the measurement of threshold voltage challenging. This measurement induced threshold voltage instability for two different measurement methodologies a) Pulsed transfer characteristic measurement b) DC step transfer characteristic measurement is investigated and a methodology to mitigate this effect has been proposed. It is further observed that Schottky gate has a more pronounced measurement induced threshold instability relative to an ohmic gate which has a stable threshold voltage throughout measurement. A detailed TCAD analysis validating the proposed physical mechanisms and the effect of ohmic and Schottky contact are also demonstrated in this chapter

Chapter 6 investigates the instability arising in the threshold voltage due to nominal ON state and OFF - state operations. The $V_{TH}$ instability arising due to the gate voltage stresses (ON state) and the drain voltage stresses (OFF state) are studied by developing novel measurement setup. The physical mechanisms hypothesized are further validated using the TCAD simulations.

Chapter 7 introduces a novel measurement technique to measure the time required to recover from the threshold voltage instability post stress eliminating the measurement induced effects often present in the nominal techniques. The effect of the stress voltage, effect of stress time on the recovery time is also summarised.

Chapter 8 summarises and provides conclusions for the work done as well as provide a discussion on the possible continuation of this work.

# 2. AlGaN/GaN hetero junction physics and normally off HEMT

*This chapter describes the basics of the heterojunction physics observed in the heterostructures and explains the principle of 2-dimensional electron gas formation in the AlGaN/GaN heterostructure. The various normally off architectures of the AlGaN/GaN on Si HEMTs are reviewed and p-GaN gate architecture is reviewed in detail. The various reliability and operational challenges of p-GaN/AlGaN/GaN on Si HEMT and the implications of threshold voltage instability at the device and circuit level is reviewed.*

## 2.1 Gallium Nitride crystal and its polarisation potential

Depending upon the nature of the bond and its ionicity between the atoms semiconductors are classified as non-polar, semi polar, polar. Ionicity depends on the electro-negativity (EN) difference. The non-polar semiconductor, e.g. diamond, Si, Ge, has a covalent bond with EN difference, say, $< 0.5$. Elemental semiconductors (C, Si, Ge) consist of one atom; hence, are necessarily covalent and non-polar. III-V compound semiconductors (GaAs, InP, GaN) have EN difference between the anions and the cations hence have necessarily partly ionic bond (EN = 0.4-0.9) and at times are moderately (EN = 1-1.3) polar or strongly polar (EN= 1.4 to 1.8). GaN (Ga-1.8, N-0.75) with EN difference of 1.05 is characterised as a polar covalent bonding crystal. GaN by virtue this polar nature have a net built in electric field as shown in *Figure 2.1.* The internal electric field is in the direction from positively charged N anion to negatively charged Ga cation and the polarisation potential is in the opposite direction to the electric field. This polarisation potential is called the spontaneous polarisation potential.

The most stable crystal structure for Gallium Nitride (GaN) is wurtzite. Wurtzite is based on a hexagonal crystal lattice system (*Figure* 2.2*)* and miller Bravais system is used to define the planes as derived in *Figure* 2.3. Not all the planes are polar in a hexagonal wurtzite-based crystal lattice, there exists polar 'C' plane (0001), semipolar planes (10-10) and non-polar 'M' planes (11-21) as shown in *Figure* 2.3. The reduced polarisation effects in non-polar planes may be suitable for realising certain optoelectronic devices. And semipolar planes offer a balance between polarisation and crystalline quality useful for certain use cases of optoelectronic devices. By virtue of the

strong non centro symmetrical crystal structure, GaN based material show strong spontaneous polarization potential. To have an inherent polarisation potential GaN need to be grown along the positive C axis orthogonal to C plane (0001). The GaN material epitaxially grown can be with Ga atoms facing the surface (Ga-polar) or Nitrogen atoms facing the surface (n- polar) as shown in *Figure* 2.2, this is critical as the direction of the polarization potentials is dependent on the atoms at the surface. Heterostructures grown on Ga- polar GaN tend to have lower defect densities, enhanced mobility than the ones grown on n-polar GaN, thus Ga- polar GaN is widely adopted for HEMTs. Ga faced GaN material system based on wurtzite crystal lattice consist of 2 closely spaced hexagonal layers, one based out of Ga cations and the other based on N anions.

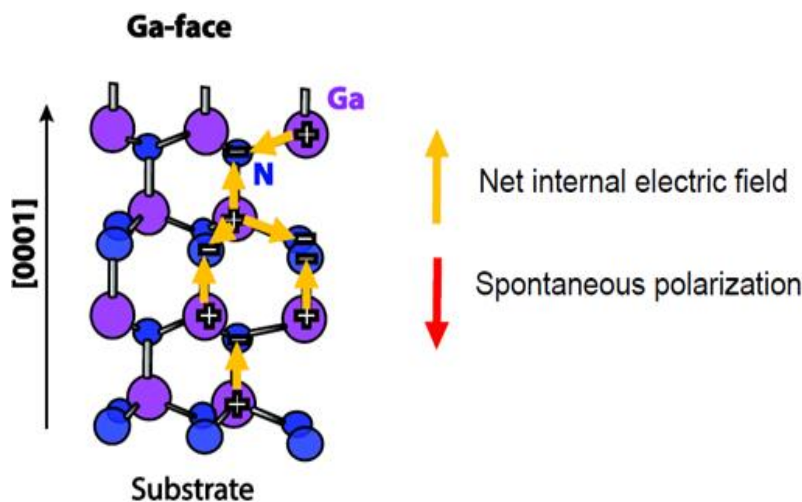



*Figure 2.1: Illustration showing the inherent spontaneous polarisation in Ga face GaN*

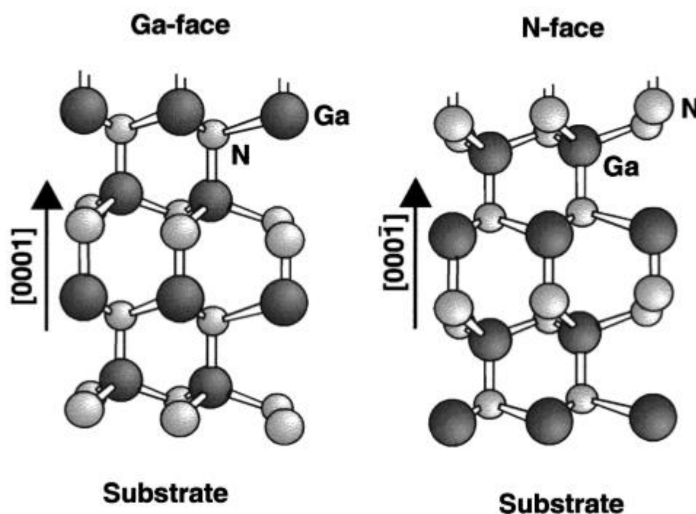



*Figure 2.2: Schematic of the wurtzite crystal structure of GaN with a Ga- face and N-face [35]*

In addition to the spontaneous polarisation potential there exists piezoelectric polarisation potential which is instrumental in the formation of the 2-dimensional electron gas. When wurtzite lattice-based material like AlGaN is pseudo morphically grown on wurtzite lattice based GaN, AlGaN is elastically deformed due to the lattice mismatch which causes a shift in the atoms and in turn an electric field is induced leading to a potential called piezoelectric polarisation potential.

*Polar 'C' plane*

Intercepts: $a_1 = a_2 = a_3 =$ § ; c =1

Indices calculation : $1/a_1 = 1/a_2 = 1/a_3 = 0$; $1/c = 1$

Miller Indices: (hkil) → (0001)

*Semi Polar plane*

Intercepts: $a_1 = 1$, $a_2 = 1$, $a_3 = -1/2$; c =1

Indices calculation : $1/a_1 = 1/a_2 = 1$, $1/a_3 = -2$; $1/c = 1$

Miller Indices: (hkil) → (11-21)

*Non Polar plane 'M'*

Intercepts: $a_1 = 1$, $a_2 =$ §, $a_3 = -1$; c = §

Indices calculation : $1/a_1 = 1$, $1/a_2 = 0$, $1/a_3 = -1$; $1/c = 0$

Miller Indices: (hkil) → (10-10)

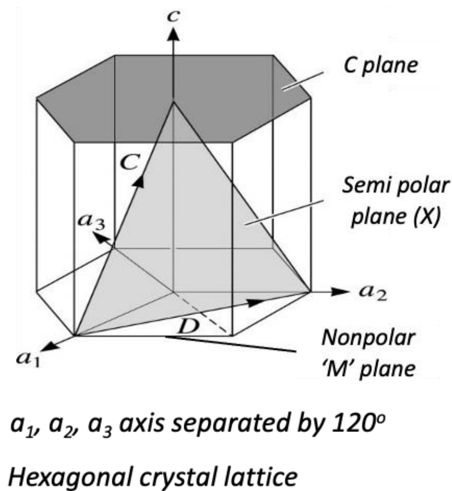



*Figure 2.3: Illustration showing the Miller Bravais indices to represent the hexagonal wurtzite crystal lattice*

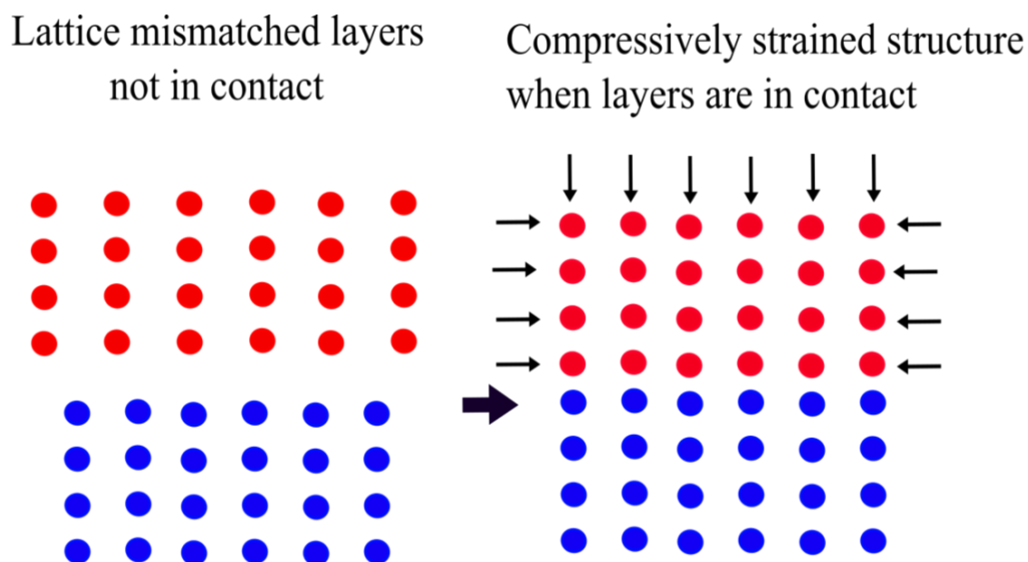



*Figure 2.4: illustration depicting the elastic deformation and a compressive strain caused by a lattice mismatched layers*

During growth of such pseudo morphic lattice mismatched structures, atoms can experience a compressive strain or a tensile strain depending upon the nature of the lattice mismatch. *Figure* 2.4 depicts a lattice mismatch where the material is elastically deformed due to the compressive strain.

### 2.2 Heterojunction physics of AlGaN/GaN heterostructure

Hetero junction is the interface between two different semiconductor materials with a different bandgap and a closely matched lattice rather than a largely mismatched lattice to avoid dislocations at the interface altering the electrical behaviour of the junction. With this in view a semiconductor with a closely matched lattice constant as that of GaN and a large bandgap difference is chosen to form a good heterojunction.

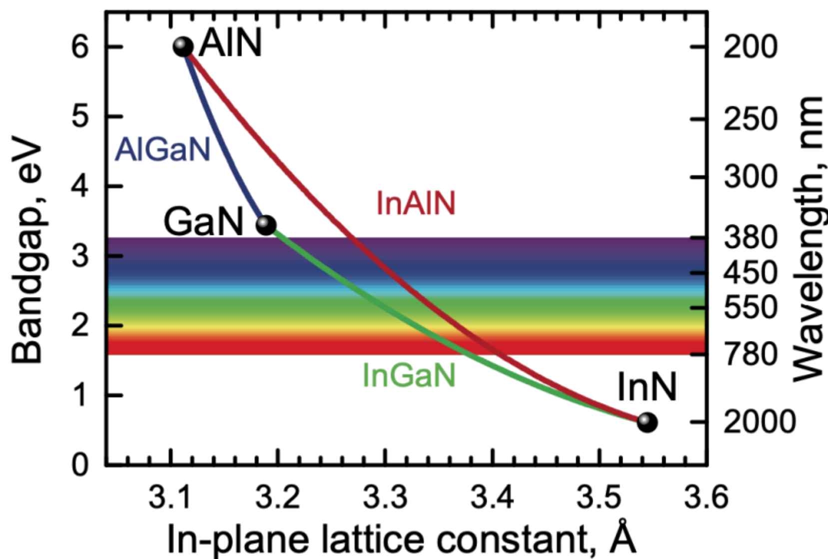



*Figure 2.5: Illustration showing the in plane lattice constant and the bandgap difference of various III-V semiconductors including AlN and GaN [36]*

AlN is chosen to form the heterojunction with the GaN as AlN bandgap and lattice constant match our requirement as shown in *Figure* 2.5. By controlling the mole fraction of the Aluminium in the GaN during the epitaxial growth we could tune the band gap and other metrics of the material as shown in *Table 4*. By varying the aluminium concentration (x) of the GaN layer between x = 0 and x = 1, a ternary compound ($Al_xGa_{1-x}N$) with electrical and mechanical properties between GaN (x = 0) and AlN (x = 1) is obtained as given by

$P_{AlGaN\,(x)} = P_{AlN} * x + P\text{-}GaN * (1 - x)$

Where P corresponds to the properties such as bandgap, electron affinity, elastic constants, and permittivity.

*Table 4: Table showing the parameters of the AlGaN which forms the heterojunction with the GaN*

| Parameter | Symbol / unit | GaN | $Al_{0.2}Ga_{0.8}N$ | AlN |
|---|---|---|---|---|
| Bandgap | Eg (eV) | 3.4 | 3.74 | 6.2 |
| Breakdown field | $\xi c$ ($10^6$ V/cm) | 3.3 | 4.32 | 8.4 |
| Relative permittivity | $\varepsilon r$ | 9.5 | 9.3 | 8.5 |

In the case of AlGaN/GaN heterojunction the band alignment across the interface is typically such that the bandgap of the lower bandgap material (GaN) is positioned energetically within the wider bandgap of the second semiconductor (*Figure* 2.6) forming the so-called Type I or straddling heterojunction. When the two layers are in contact the bandgap discontinuity forms a quantum well, as it will be shown later in this section 2.3

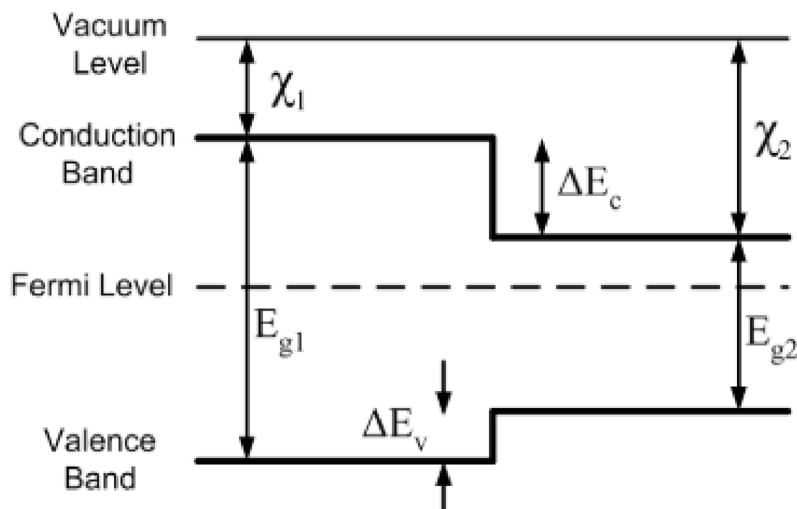



*Figure 2.6 Illustrative band diagram of a straddling heterojunction*

### 2.3 2-DEG formation in AlGaN/GaN heterostructure

The hetero junction AlGaN on GaN will have different direction of the spontaneous polarisation potential and induced piezoelectric potential depending upon the Ga face or N face of the GaN. Ga- face GaN is the commonly adopted epitaxial material over which heterostructure is made for HEMT realisation. If the strain built in

such heterostructure is compressive the piezoelectric polarisation charge (coulombs/ $cm^2$) is negative whereas if the strain induced is tensile the piezoelectric polarisation is positive as in *Figure* 2.7. The heterojunction structure in the highlighted red box is the structure of interest for high electron mobility transistors in this thesis.

When the AlGaN is placed on Ga face GaN, with lattice constant of AlGaN slightly smaller than GaN due to the lattice mismatch a tensile strain is induced as in *Figure* 2.8. The tensile strain can happen along the in-plane axis as well as the growth axis C leading to the piezoelectric polarisation potential ($P_{PE}$). The Piezoelectric polarisation potential is given by *Equation 2.1*

$$P_{PE} = e_{33}\epsilon_z + e_{31}(\epsilon_x + \epsilon_y) \quad 2.1$$

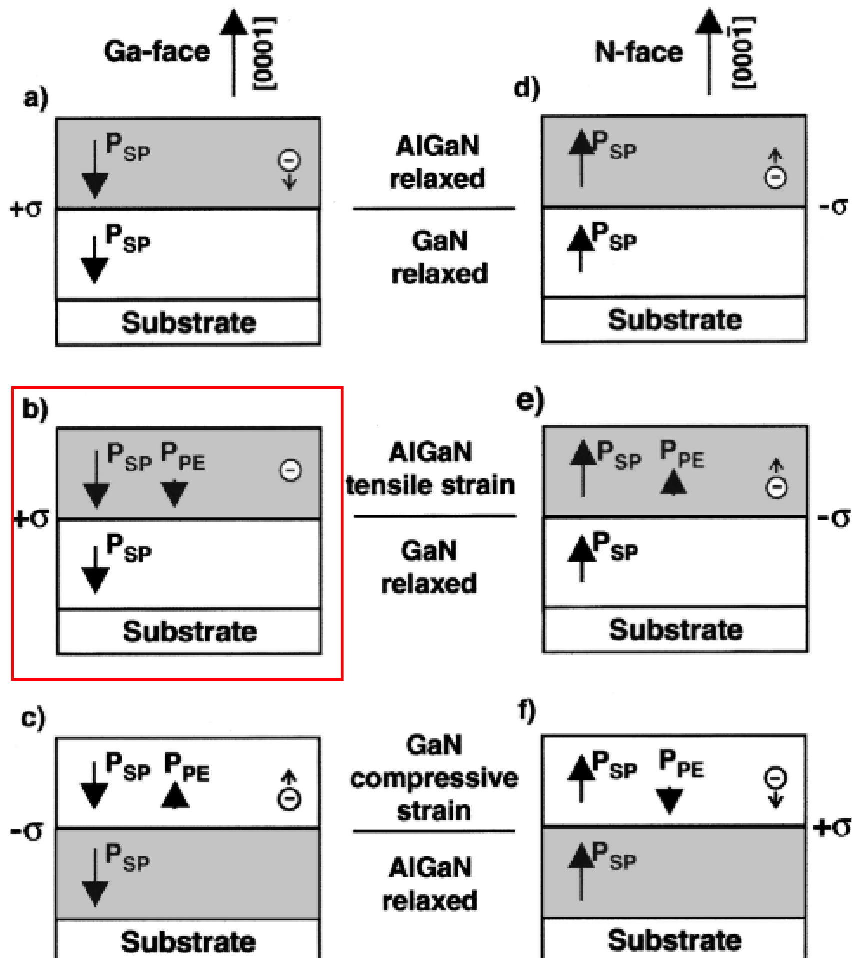



*Figure 2.7: Illustration depicting the direction of the polarisation potentials and their polarity dependence on the nature of the strain and the face (Ga-face or N- face) of the material [35]*

Where $e_{33}$ and $e_{31}$ are piezoelectric coefficients, $\epsilon_z$ is the strain along the C axis and $\epsilon_x = \epsilon_y$ is the in-plane strain given by *Eqn. 2.2*

$$\epsilon_z = \frac{\mathrm{C} - C_0}{C_0}; \quad \epsilon_x = \epsilon_y = \frac{\mathrm{a} - a_0}{a_0}; \tag{2.2}$$

Where $a_0$ , $C_0$ are equilibrium values of the lattice parameters. The relation between the lattice constants of the hexagonal GaN is given by *Eqn. 2.3*

$$\frac{\mathrm{C} - C_0}{C_0} = -2\frac{C_{13}}{C_{33}}\frac{\mathrm{a} - a_0}{a_0}; \tag{2.3}$$

Where C13 and C33 are the elastic constants of the material. From equation 2.2 and 2.3 and 2.1 the $P_{PE}$ is given as

$$P_{PE} = 2\frac{\mathrm{a} - a_0}{a_0}\left(e_{31-}e_{33}\frac{C_{13}}{C_{33}}\right) \tag{2.4}$$

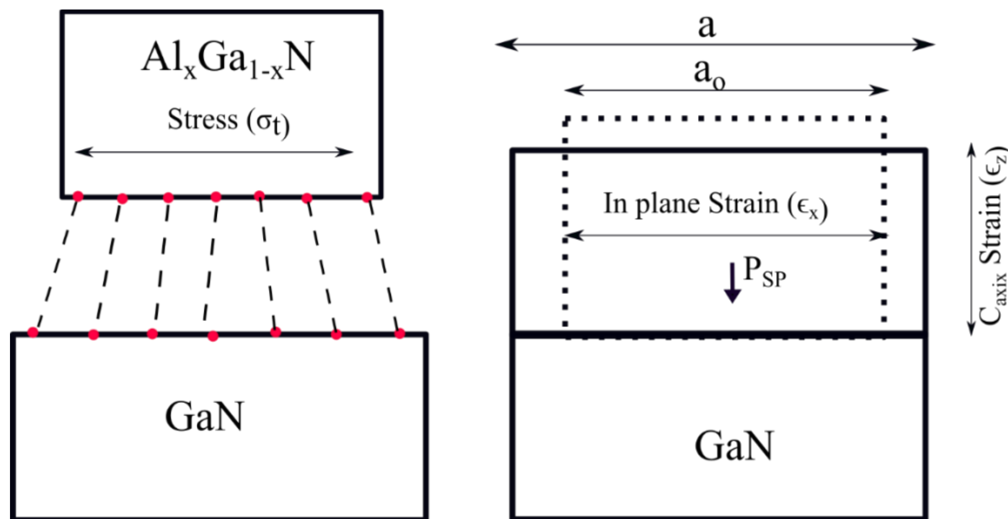



*Figure 2.8: Illustration showing the tensile strain in plane and in C axis at AlGaN/GaN interface*

It is to be noted that $\left(e_{31-}e_{33}\frac{C_{13}}{C_{33}}\right)$ is <0 for AlGaN over all the compositions and hence the $P_{PE}$ is negative for tensile and positive for compressive strained barriers as in *Figure* 2.7, *2.8*. The net polarisation charge developed at the interface is the actual difference in the polarisation potentials (Spontaneous polarisation potential $P_{SP}$ + Piezoelectric polarisation potential $P_{PE}$) across the 2 different semiconductor materials forming the hetero junction when they are in contact as in *Figure* 2.9. For the AlGaN/GaN

heterostructure with a Ga face, $P_{PE}$ is negative, $P_{SP}$ is negative, and the polarisation induced charge density due to the gradient of the polarisation potential is given by *Eqn.2.5*. The strain induced piezoelectric polarisation potential developed when AlGaN is grown on GaN (Ga face) buffer is more pronounced at the thinner AlGaN rather than the GaN buffer layer which is relatively thick ($(P_{PE})_{GaN}$ is negligible).

$$\sigma = (P_{PE} + P_{SP})_{AlGaN} - (P_{PE} + P_{SP})_{GaN} \qquad 2.5$$

$$|\sigma(x)| = |(P_{PE} + P_{SP})_{AlGaN} - (P_{SP})_{GaN}|$$

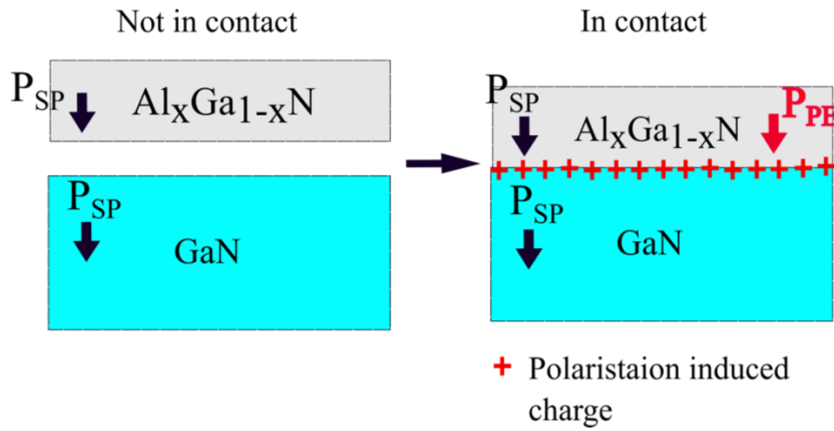



*Figure 2.9: Illustration depicting the formation of the positive polarization charge at the interface of the AlGaN/GaN heterojunction*

*Table 5 : Elastic constants of GaN, AlN and the lattice constants from* [35]

| Parameter | Type | unit | AlN | GaN |
|---|---|---|---|---|
| C11 | Elastic constant | GPa | 396 | 367 |
| C12 | Elastic constant | GPa | 137 | 135 |
| C13 | Elastic constant | GPa | 108 | 103 |
| C33 | Elastic constant | GPa | 373 | 405 |
| C44 | Elastic constant | GPa | 116 | 95 |
| ao | Lattice constant (in plane) | Angstrom | 3.112 | 3.189 |
| Co | Lattice constant (C axis) | Angstrom | 4.982 | 5.185 |

$$|\sigma(x)| = \left|2\frac{\mathrm{a}(0) - \mathrm{a}(x)}{a_0}\left(e_{31-}e_{33}\frac{C_{13}}{C_{33}}\right) + P_{SP}(x) - P_{SP}(0)\right| \qquad 2.6$$

The net polarisation induced charge density at the hetero interfaces could be evaluated by the *Eqn.2.6* substituting the lattice constants and elastic constants as listed in *Table*

5 , where x is the mole fraction of the Aluminium content in heterojunction $Al_xGa_{1-x}N$/GaN. These equations are extensively used to calculate the polarisation charges at the heterointerfaces present in the p-GaN/AlGaN/ GaN on Si HEMT for the TCAD models used in Chapter 4, 5 and 6.

The polarisation induced positive charge at the interface induces the formation of a thin sheet of conducting free electrons called the 2-dimensional electron gas without

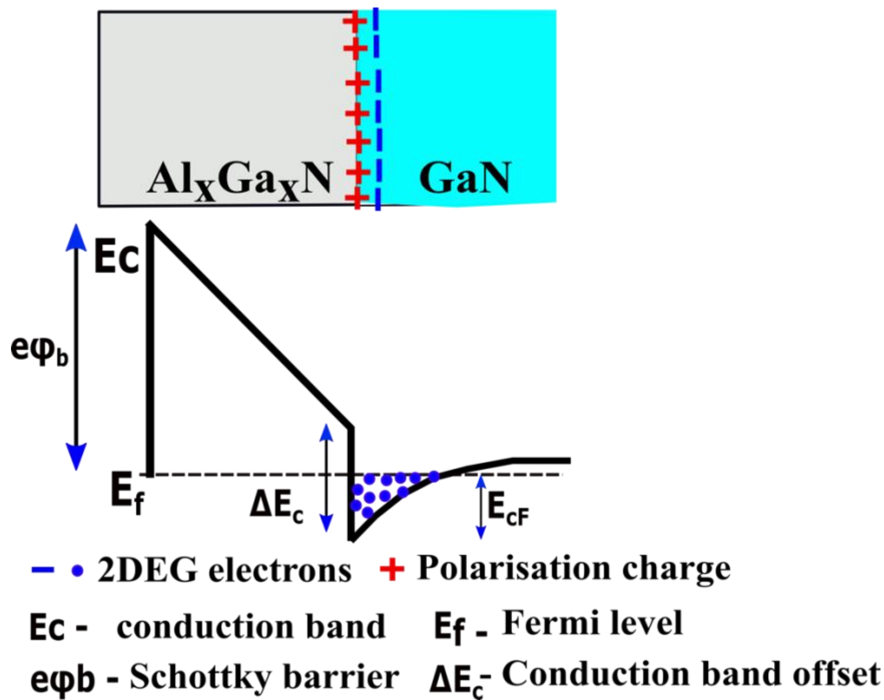



*Figure 2.10: Illustration of the positive polarisation charge inducing the formation of a confined conducting sheet of electrons called 2-dimensional electron gas*

the application of any external electrostatic potential. The band gap discontinuity and the polarisation induced sheet charge create a triangular quantum well at the heterointerface where electrons are confined as a high density of charge (of the order of $10^{13}$ $cm^{-2}$) with a high carrier mobility (up to 2000 $cm^2/Vs$). The 2-DEG channel is formed at the AlGaN/GaN interface where the (quasi-) Fermi level lies well below the conduction band as in *Figure* 2.10.

The Schrodinger and Poisson equations are solved simultaneously and the sheet electron density at the nominally undoped AlGaN/GaN interface is given by [37]

$$n_{2DEG} = \frac{\sigma(x)}{e} - \left(\frac{\epsilon_0\,\epsilon(x)}{d_{AlGaN}e^2}\right)[e\phi_b(x) + E_{CF}(x) - \Delta E_c(x)] \qquad 2.7$$

Where $d_{AlGaN}$ is the thickness of the $Al_xGaN_{1-x}$ barrier, $e\emptyset_b$ is the Schottky barrier of the gate contact, $E_{CF}$ is the penetration of the conduction band edge below the fermi level at the AlGaN/GaN interface, $\Delta E_c$ is the conduction band offset at the AlGaN/GaN interface as in *Figure* 2.10. $\Delta E_c$ is evaluated by *eqn*.2.8 *and* $E_{CF}$ (x) is evaluated by *eqn*.2.9

$$\Delta E_c(x) = 0.7\left[E_g(x) - E_g(0)\right] \quad 2.8$$

$$E_{CF}(x) = E_0(x) + \frac{\pi\hbar^2}{m^*(x)}\, n_{2DEG}(x) \quad 2.9$$

Where $E_0$ is the lowest sub band level of the 2-DEG and it is given by *Eqn*.2.10

$$E_0(x) = \left\{\frac{9\pi\hbar^2 e^2 n_{2DEG}(x)}{8\epsilon_0\sqrt{8\,m^*_{GaN}}}\right\} + \frac{\pi\hbar^2}{m^*(x)}\, n_{2DEG}(x) \quad 2.10$$

Where $\hbar$ is the reduced Planck constant and $m^*(x)$ and $m^*_{GaN}$ are the effective mass of the AlGaN and GaN respectively. The carrier density at the 2-dimensional electron gas is dependent on the difference between the polarisation charges in the GaN layer and those in the AlGaN layer, which in turn are dependent on the mole fraction of Aluminium in AlGaN layer and on the thickness of the AlGaN layer. The underlying physics behind the heterojunctions and the equations discussed are reviewed and detailed from [38].

## 2.4 HEMT based on AlGaN/GaN on silicon substrate

For large scale manufacturability, CMOS platform compatibility and to enable monolithic integration AlGaN/GaN heterojunction is preferentially grown on a 6/8 inch silicon substrates. Despite the large relative mismatch of lattice constant and the thermal expansion coefficient of silicon and GaN as in *Table 6*, GaN has been grown on Si to mitigate the issues of high cost of manufacturing associated with the more suitable SiC and GaN substrates. And lateral devices based on GaN on Si enable monolithic integration of mixed signal, analog, MEMS devices utilising the CMOS platform offering added functional value for the given area on chip. With the relative maturity of the epitaxial growth techniques and the successful demonstration of the GaN on 200mm (8 inch) Si substrates [39] silicon is the substrate of choice for commercialisation of GaN power devices. However GaN on SiC is the substrate of choice for commercialisation of

GaN RF HEMTs used in radar and defence applications owing to their improved device/thermal performance metrics and low cost sensitivity.

*Table 6: Lattice mismatch of GaN on various substrates* [40]

| Parameter | GaN-on-Si | GaN-on-SiC | GaN-on-sapphire | GaN-on-GaN |
|---|---|---|---|---|
| Defect density | $\sim 10^9/cm^2$ | $\sim 5 \times 10^8/cm^2$ | $\sim 10^9/cm^2$ | $\sim 10^4$–$10^6/cm^2$ |
| Lattice mismatch (%) | 17 | 3.5 | 16 | 0 |
| CTE mismatch (%) | 54 | 25 | 34 | 0 |

*CTE – Thermal expansion coefficient*

GaN and Si's lattice mismatch and thermal expansion coefficient mismatch lead to GaN – Si alloy formation causing cracking of the GaN epi layers leading to higher threading dislocations [40]. To mitigate the lattice mismatch of GaN on Si, significant work has been carried out in the past decade and 100 to 200 nm thick AlN transition layers are commonly used to avoid the formation of the GaN- Si alloy. AlN transition layers form a sharp interface nucleation layer with Si (111) thereby yielding smooth surface morphologies with roughness < 5nm and GaN buffer layer grown on top of this AlN transition layer has lower thread dislocation densities (TDD). AlN transition layer thickness is critical as cooling of thicker AlN layers post high temperature epitaxial growth led to tensile strain and subsequent cracking, thus cooling induced strain kinetics play a role in controlling the TDD. Sometimes AlGaN buffer layer or superlattices of AlGaN layer is grown on top of AlN nucleation layer before GaN buffer layer growth. In summary transition layer is a semiconductor system consisting of AlN nucleation layer, AlGaN layer, AlGaN superlattice layers grown epitaxially to mitigate the large lattice mismatch. Nucleation layer is the first layer which is grown on top of the silicon substrate and superlattice layers consists of a series of alternating layers with different mole fractions. The transition layer ensures high quality 2-DEG formation at the AlGaN/GaN heterostructure grown on top of it. These transition layers are doped intentionally and unintentionally with carbon to minimise the vertical leakage and to increase vertical breakdown [41]. Carbon acts as an amphoteric dopant in GaN, C replacing Ga in GaN lattice makes it a N type dopant and C replacing N in GaN lattice makes it a P type dopant. The growth conditions govern the possibility of C acting as a N type or P type dopant and can be controlled. Intentional controlled incorporation of carbon is often done during the growth of the transitional layers for effective

management of leakage and trapping. However, due to the organic precursors (E.g. Trimethyl gallium) used in the epitaxial growth processes unintended carbon incorporation is often observed in the transitional, buffer and barrier layers referred to as unintentional doping.

The Buffer layer which is grown on top of the smooth crack free transition layer sustains the high electric field built up during the OFF state high voltage blocking conditions of HEMTs. GaN buffer thickness is critical in determining the voltage handling capability of the HEMT made for 200V, 600V applications, thus a crack free, high quality GaN buffer of 3.2 µm to 5.2 µm is nominally used [42]. Buffer layers typically are unintentionally doped with carbon during the epitaxial growth. The reproducibility and repeatability of the epi stack is largely dependent on the transition layer, buffer layer growth.

The Barrier layer is often a thin AlGaN layer which forms the hetero structure with the GaN buffer. The thickness and the % Al doping has a significant influence on the 2-DEG formation and its sheet charge density.

To realise a switching device which utilises and controls the 2-DEG formed by the AlGaN/GaN heterojunction, source/drain and gate terminals are needed as in *Figure* 2.11 which forms a normally ON HEMT.

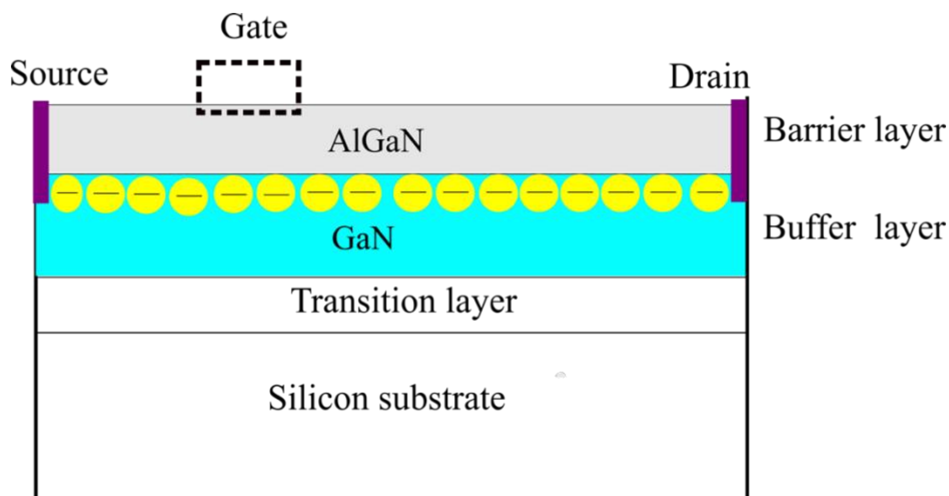



*Figure 2.11: High electron mobility transistor basic structure utilising the AlGaN/GaN heterojunction*

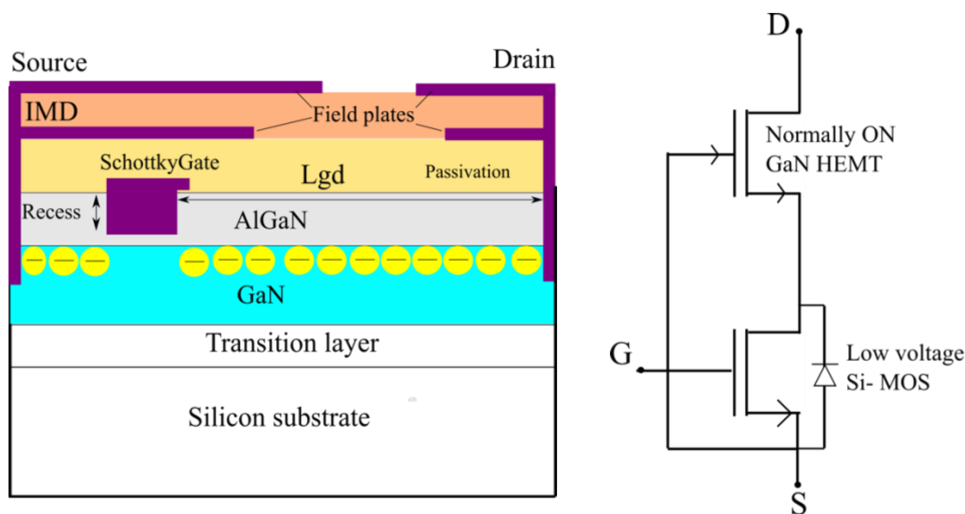
## 2.5 Normally off AlGaN/GaN on Si HEMT and its operation

The Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT) is a 4-terminal device comprising of source, drain, gate and the substrate. Normally off GaN HEMT comprises of a AlN transition layer (100-200nm), GaN buffer layer (2-6 μm). A thin AlGaN layer (10-60 nm) is epitaxially grown over GaN buffer layer. By the spontaneous and piezoelectric polarisation potential differences between AlGaN and GaN layers a conducting channel at the hetero interface AlGaN/GaN is formed naturally without the application of any potential. The conducting channel is called the 2-dimensional electron gas (2-DEG), 2-DEG is a collection of electrons in a triangular quantum well confined by the conduction band of the AlGaN, GaN and the fermi level which have high mobility and higher carrier concentration. Utilising this 2-DEG a normally-on transistor could be engineered by the addition of ohmic source, drain terminals and Schottky gate terminals to control the carrier concentrations in the 2-DEG. However, for safety and lower static power dissipation normally off GaN HEMT power switching devices are commonly preferred [43] except few selected applications like start-up circuits where normally on HEMTs are preferred. There have been many techniques proposed to deplete the channel of its conductive properties to make the HEMT normally off, listed as below

A) Gate Recess Technique
B) Fluorine implantation Technique
C) Cascode configuration normally off HEMT
D) MOS channel transistor normally off HEMT
E) MESFET – Metal Schottky field effect transistor (described in chapter 2.4)
F) p-GaN gate normally off HEMT [44]

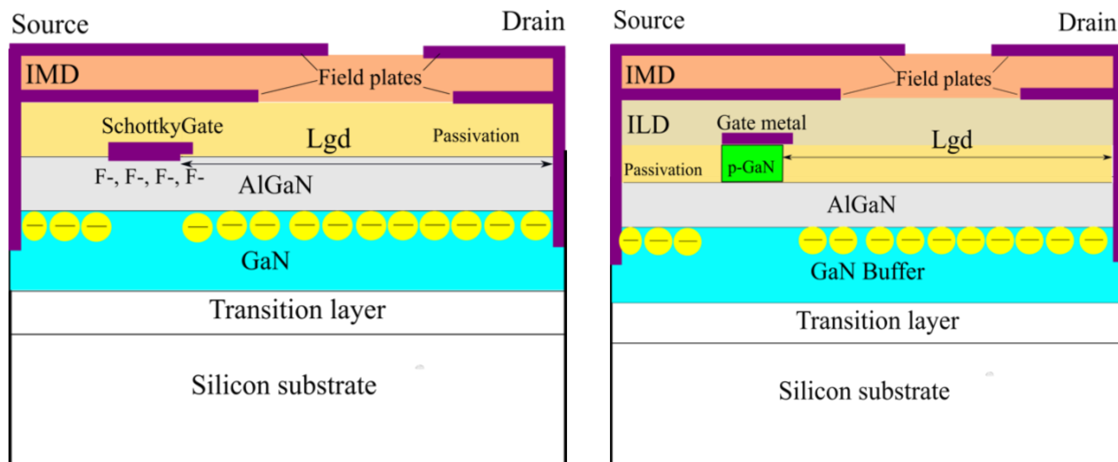
The approach to thin AlGaN layer below the gate by etching techniques is referred to as the gate recess technique. By selectively etching back AlGaN layer below the gate region as shown in *Figure* 2.12 *a)* the net positive charge built up at the AlGaN/GaN interface causing the 2-DEG formation is reduced, thereby causing normally off operation. In fluorine implantation technique, by incorporation of fluorine below gate in AlGaN barrier, 2-DEG is depleted below gate making it normally off as shown in *Figure* 2.12 *c)*. In the Gate recess approach and the fluorine incorporation approach low threshold

voltage < 1V could only be achieved. For power electronic applications it is desired to have a larger $V_{TH}$ and larger gate swing hence these 2 approaches are less preferred. Cascode configuration is another commonly proposed normally off approach where the low voltage Si MOSFET is connected in series with the normally ON GaN HEMT such that drain of the Si FET is connected to the source of the GaN HEMT and the gate of the GaN HEMT is shorted with the source of the Si FET. In the Cascode configuration the gate terminal of the Si MOSFET acts as the control gate of the Cascode device to turn on the normally ON GaN HEMT, the drain terminal of the normally ON HEMT acts as the drain of the Cascode device and the source terminal of the Si MOSFET acts as the source terminal of the Cascode device as shown in *Figure* 2.12 *b).* This Cascode device enables higher threshold voltage, reliable operation, however it introduces additional $R_{DS(ON)}$ and reverse recovery charge (Qrr) due to the Si MOSFET. The most common and industrially widely adopted normally off GaN HEMT architecture is the HEMT with p-GaN gate proposed by Y.Umeto et.al [44] from Panasonic in 2007 called gate injection transistor (GIT). p-GaN gate normally OFF architecture as seen in *Figure* 2.12 *d)* is widely adopted which will be discussed in more detail.




*a) Gate recess technique – normally off HEMT*

b) *Cascode – normally off HEMT*




c) *F implant technique – normally off HEMT*  d) *P doped GaN gate – normally off HEMT*

*Figure 2.12: Various normally off architectures of the GaN HEMT*

The p - GaN layer in the gate region raises the potential at the channel region such that the conduction band is above the quasi-fermi energy level as seen in *Figure 2.13 leaving* no electrons at the triangular quantum well at the interface of the AlGaN/GaN layer which means the HEMT is normally OFF. The normally off p GaN HEMT operation at various bias conditions and the output characteristics are shown in *Figure* 2.14 as follows

(a) At zero bias, the channel formed by the 2-DEG present at the AlGaN/GaN interface is depleted below the gate region due to the p doped GaN cap layer. The HEMT which is normally ON is now normally OFF, no current flows in the device until a positive gate voltage is applied (*Figure* 2.14 *(a)*). For $V_{GS} < V_{TH}$, the device is in off-state since the channel beneath the gate is still OFF and the drain current is negligible.

(b) In on-state, when $V_{GS}>V_{TH}$, the electrostatic charge conditions across the p-GaN/AlGaN/GaN gate stack (explained in detail in Chapter 4) is such that the 2-DEG is accumulated below the gate region completing the channel between the source and drain terminal enabling normally ON operation (*Figure* 2.14 *(b)*)

(c) In off-state also known as blocking mode (*Figure* 2.14 *(c)*), at high $V_{DS}$, the channel starts depleting from the gate towards the drain and the 2-DEG depletion holds the drain voltage in the blocking mode. *Figure* 2.14 *(d)* shows the typical output characteristics of the normally OFF p-GaN HEMT. The transition form the ON state to

OFF state or the OFF state to ON state is called switching. Switching involves charging and discharging of the input, output, transfer capacitances and the time taken to switch depends upon the capacitances. Due to the absence of the body diode, smaller form factor, lower capacitance per unit area (smaller input and output capacitances) GaN HEMTs can switch from OFF state to ON state or from ON state to OFF state much faster consuming less energy translating to lower switching losses relative to the silicon MOSFETs.

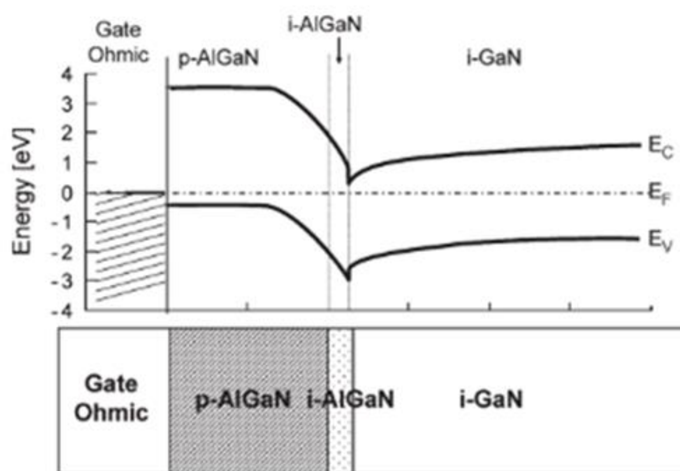
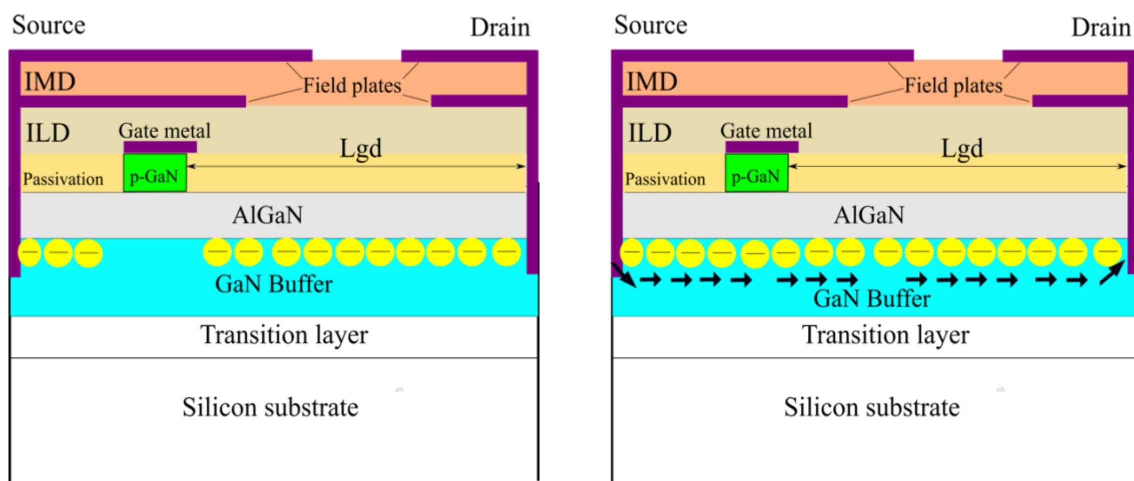
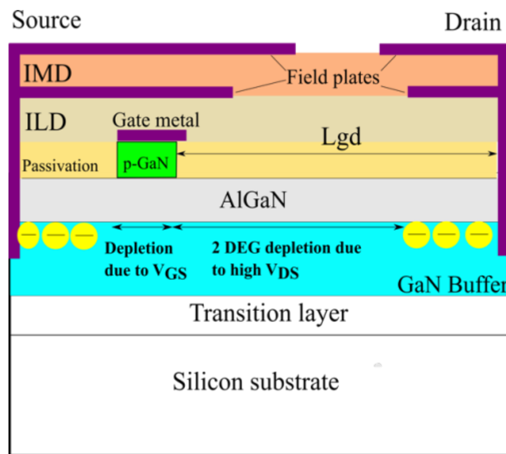
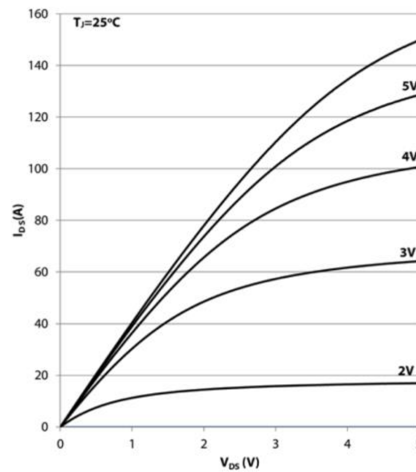



*Figure 2.13 : Illustration showing band diagram of the p-gate normally OFF GaN HEMT by Umeto* [44]




*OFF condition $V_{GS}$=0V, $V_{DS}$= 0V (a)* *ON condition $V_{GS}$>$V_{TH}$, $V_{DS}$= 50mV (b)*




*OFF state blocking $V_{DS}$ = High V, $V_{GS}$ = 0V (c)*

*Output characteristics (d)*

*Figure 2.14: Modes of operation of normally OFF p-GaN gate HEMT a) OFF state b) ON state c) OFF state blocking state d) Output characteristics Id-Vd*

## 2.6 p-GaN gate AlGaN/GaN on Si HEMT fabrication and design

The generic process by which normally off p-GaN gate AlGaN/GaN on Si HEMT is realised is presented. The devices investigated in this thesis are based on TSMC, p gate technology and are detailed before each chapter. Epitaxial III-nitride layers are grown on a Si (111) wafer by metal – organic chemical vapor deposition. The III-nitride layers over silicon wafer are composed of a 150-nm AlN nucleation layer, a 3-4µm semi-insulating GaN layer, a 100 to 200-nm GaN channel, a 10 to 30 nm $Al_{0.29}Ga_{0.21}N$ layer and a 100-nm p-GaN layer. The typical density of holes in p-GaN is $2*10^{17}cm^{-3}$ and could be varied by varying the Magnesium doping. After isolating the adjacent devices by Ar implantation or MESA etching [45], the p-GaN layer is selectively etched by Inductive Coupled Plasma Reactive Ion Etching. The source and drain contacts were formed by the lift off process of e-beam evaporated Ti/Al/Ni/Au metal layers and rapid thermal annealing at 800°C for 30s in $N_2$ ambience to form ohmic contacts. After the SiN surface passivation by chemical vapor deposition technique, the gate was defined by the Inductively Coupled Plasma Reactive Ion Etching (ICPRIE) based on Cl2/BCl3 reactants. For the gate metal Ni, W, Mo, Ti are the commonly used interface metals depending upon the Threshold voltage and gate leakage current requirement. The device could be custom designed to get desired characteristics by varying control parameters in terms of epitaxial layer and device design. The doping, thickness and mole fraction of the

AlGaN barrier layers and other III-V nitride layers have significant effect on the device characteristics such as the breakdown voltage, threshold voltage and reliability. The work function of the metal stack used for the source drain and gate contacts [46] can have impact on the on-state resistance, saturation current. In addition to that passivation layers, interlayer dielectric, intermetal dielectric constitute an important role in terms of the protection and device reliability during high temperature, high field operations. Field plates also play an important role in regulating the breakdown voltage of GaN HEMTs, field plates can be suitably designed to change the position where the field peaks and breakdown happens as shown in Figure 2.15. Typically, at the blocking mode the electric field peaks at the drain/gate edges, by effective gate/drain field plate design the field peaks can be lowered henceforth enabling full depletion of the drift region before the material critical electric field is reached. Many different schemes have been reported in literature, including multiple drain, source, or gate field plates with different shapes, such as stepped, slanted or grating [47] [48][49][50]. Field plate design has also been shown to have an impact on the dynamic characteristics of the device and in particular on parasitic charge trapping, which is often an issue with GaN HEMTs [51] [52][53] [54][55]. Passivation provides electrical and chemical protection for the surface of the device [56] [57], but also modifies the surface states [58][59] and changes the surface electric field distribution [60].

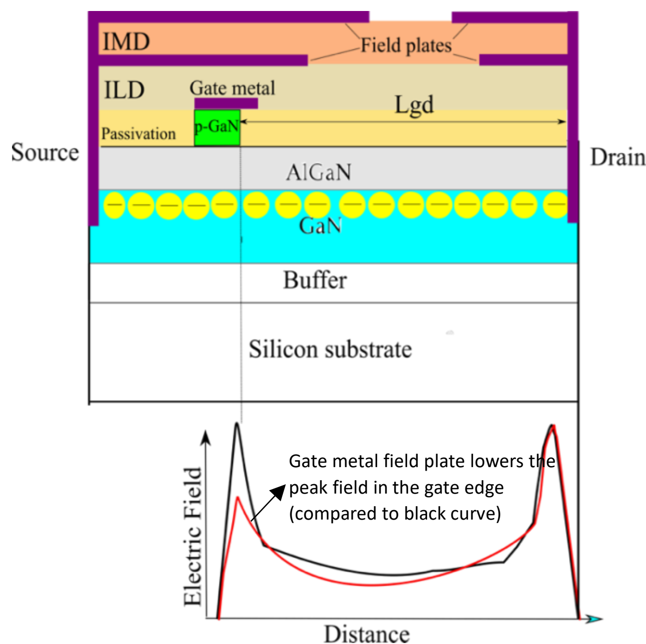



*Figure 2.15: Effect of field plate and impact of efield distribution in the normally OFF p-GaN HEMT*

## 2.7 Review of the reliability challenges of the p-GaN gate HEMT

p-GaN gate AlGaN/GaN based High Electron Mobility transistors often face reliability challenges due to the presence or generation of the traps in their bulk material, interfaces during the nominal operation [61]. These traps are dynamic and can trap electrons/holes altering the static, dynamic characteristics of the devices causing reliability concerns such as

a) Dynamic $R_{DS(ON)}$
b) Threshold voltage instabilities
c) Kink effect

Dynamic $R_{DS(ON)}$ is a phenomenon by which the on resistance of the HEMT increases post high voltage blocking mode operation. In blocking mode, the drain terminal is subjected to high $V_{DS}$ and at such instances the electric field across the semi insulating GaN buffer layers increases leading to the activation of traps which trap the 2 DEG electrons from the channel. This causes reduction in ON current (equivalently an increase in $R_{DSON}$) thereby shifting the knee voltage, saturation regime in the output characteristics making the conduction losses increase. Increase in the dynamic on resistances after the drain is subjected to a stress voltage during switching has been a major technical snag in the adoption of GaN HEMTs. By continuous improvement in epitaxy and by the introduction of the additional p GaN region beside the drain region [30] the issue of the current collapse is addressed. Injected holes from the p GaN in drain region in the off state effectively release the trapped electrons so that the current collapse is effectively eliminated as illustrated in *Figure 2.16*

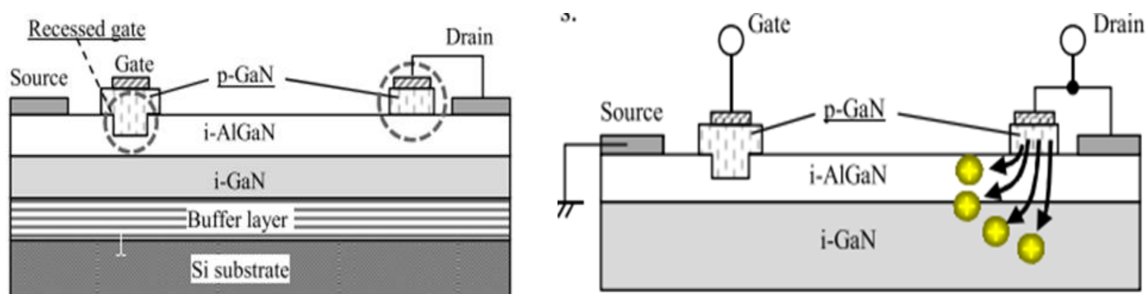



*Figure 2.16: Schematic showing the architecture of current collapse free Gate Injection Transistor with a p-GaN recessed gate in addition to the p-GaN drain*[34]

Threshold voltage instabilities refer to the change in threshold voltage due to the nominal operational gate terminal stress and drain terminal stress. They can shift in positive and negative directions leading to uncontrolled power device turn off and turn on respectively leading to power system failure discussed in detail in the next section.

Kink effect refers to the sudden abnormal increase in the drain current at a certain drain source voltage $V_{DS}$ in the saturation regime of the output characteristics of the device. Various models for this effect have been reported, the most prominent being electrons gaining kinetic energy at high electric field causing inter band impact ionisation, hole pile up and hole trapping.

The associated charge trapping and detrapping processes causing the above reliability concerns have a strong voltage dependence, electric field dependence, time dependence linked with trap metrics. The kinetics of trapping, detrapping and their modelling is detailed in *Chapter 3.* To understand the reliability failure mechanisms, it is essential to know the trap energy level location of the defects. Traps can be arising due to the a) native defects b) impurity related defects. The common native defects found in the GaN and AlGaN are Nitrogen vacancies ($N_V$), Nitrogen interstitials ($N_I$), Nitrogen antisite, Gallium interstitials ($Ga_I$), Gallium vacancies ($Ga_V$), these defects add energy levels in the band gap as listed in Table 7. Of these Nitrogen vacancies are quite commonly reported with various energy levels $E_C$ – 0.19eV, $E_C$ – 0.23eV, $E_C$ – 0.25eV. Impurities are nominally those atomic species which are new elements other than that of the GaN lattice which can be intentionally or unintentionally introduced. Silicon, Magnesium, Iron and Carbon are the common contributors for the impurity related defects. GaN intrinsically has a n – type conductivity and at times these impurities are introduced to compensate the intrinsic n type doping. In addition to that oxygen due to its high electronegativity and hydrogen due to its unpaired valence electron, bond with other impurities or native defects to form complexes which introduce trap energy levels. The database of the traps presented in Table 7 helps to physically understand various trapping mechanisms associated.

A) **Negative $V_{TH}$** shift causes a faulty turn on of the transistor during the turn off transient and lead to device breakdown and subsequently power system breakdown.

*Table 7: Database of traps detected in GaN and AlGaN devices* [62]

| Type of defect or impurity | Physical origin | Reported $E_a$ (eV) | Detected as |
|---|---|---|---|
| | | Native defects | |
| Nitrogen interstitial | $N_I$-related | 1–0.76 | $E_C-$ |
| | | 2.42 | $E_V+$ |
| Nitrogen antisite | $N_{Ga}$-related | 0.66–0.5 | $E_C-$ |
| | | 2.48 | $E_V+$ |
| Nitrogen vacancy | $V_N$-related | 0.27–0.089 | $E_C-$ |
| | | 0.4 | $E_C-$ |
| | | 3.28 | $E_V+$ |
| | $V_N$ or $Mg_{Ga}–V_N$ | 3.18 | $E_V+$ |
| | $V_N$ complexes | 0.35 | $E_C-$ |
| | $(V_N)^{3+}$ | 0.53 | $E_C-$ |
| | $V_N$ clusters | 0.613 | $E_C-$ |
| Gallium interstitial | $Ga_I$ complexes | 0.91 | $E_C-$ |
| | $Ga_I$-related | 0.8 | $E_C-$ |
| Gallium vacancy | $V_{Ga}$ or unspecified complexes (main band) | 2.85–2.47<br>1.02, 0.83 and 0.89, 0.9, and 0.86 | $E_C-$<br>$E_V+$ |
| | $V_{Ga}$–O | 1.12, 0.64, and 0.6 | $E_C-$ |
| | $V_{Ga}$-related | 0.62 | $E_C-$ |
| | | 1.8 | $E_V+$ |
| | | 0.25 | $E_V+$ |
| | $V_N–V_{Ga}$ complexes | 0.24 | $E_C-$ |
| Extended defects | Many | 1.118–0.24 | $E_C-$ |
| | | Impurities-related defects | |
| Silicon | Si-related | 0.59 | $E_C-$ |
| | | 0.4 | $E_C-$ |
| | | 0.37 | $E_C-$ |
| Magnesium | Shallow acceptor level | 0.16–0.24 | $E_V+$ |
| | Mg–H complexes | 0.08 | $E_V+$ |
| | | 0.62 | $E_C-$ |
| | Mg-related | 0.355 and 0.597 | $E_C-$ |
| | $Mg–V_N$ complexes | 0.44 | $E_C-$ |
| Hydrogen | $H–V_{Ga}$ complexes | 2.62–2.47 | $E_C-$ |
| | C- or H-related | 0.578 and 0.49 | $E_C-$ |
| Oxygen | $O–V_{Ga}$ complexes or dislocations | 1.118, 0.642, and 0.599 | $E_C-$ |
| | $O_N$ | 0.44 and 0.01 | $E_C-$ |
| Iron | Fe-related | 0.397, 0.5, 0.57, 0.66, 0.68, and 0.72 | $E_C-$ |
| | | 2.5 | $E_V+$ |
| | $Fe^{2+}$ or $Fe^{3+}$ related | 0.34 | $E_C-$ |
| | | 3 | $E_V+$ |
| Carbon | $(C_N)^0$ | 3.31–3.22 | $E_C-$ |
| | | 0.29 | $E_V+$ |
| | $(C_N)^{-1}$ | 0.8–0.95 | $E_V+$ |

B) **Positive $V_{TH}$** shift mandates a relatively large gate drive voltage to turn on the device fully & suppress the effect of dynamic ON – resistance. It leads to increased turn on losses at instances when the gate resistance is high and can lead to 20% higher turn on losses [63]

C) **Positive $V_{TH}$** shift also leads to larger reverse turn on voltage in the reverse conduction mode and lead to higher reverse conduction energy loss during the dead time increasing the losses.

To understand the impact of $V_{TH}$ instability at the application level a half bridge unit along with a high voltage driver integrated circuit (HVIC) as in *Figure* 2.17 is considered. When the high output (HO) terminal of the HVIC drives ON the high side MOSFET (HSMOS) and the low output terminal of the HVIC simultaneously drives OFF the low side MOSFET (LSMOS) the drain terminal voltage of the LSMOS ramps to ~ $V_{dd}$ (~ 600V) in few nano seconds. This swift voltage transient causes a miller current = $C_{GD}$ * ($dV_{dd}/dt$) through the miller capacitor $C_{GD}$ of LSMOS and can lead to voltage spike causing parasitic turn ON of the LSMOS, which need a careful design. In addition to the fact that p-GaN gate normally off HEMTs generally have a small $V_{TH}$ (<2V), if there is a $-\Delta V_{TH}$ shift the above explained circumstances can cause power device failure.

Dead time losses in GaN HEMTs are larger in general compared to Si MOSFETs and with the threshold voltage instability, reverse conduction voltage increases causing a further increase in the deadtime losses. In the third quadrant operation of a GaN HEMT the potential at the drain terminal is negative with respect to source ($-V_{DS}$) and the channel is typically off in a E- mode HEMT (with $V_{GS}$ =0V or $V_{GS} < V_{TH}$) and there exists a net positive voltage across the gate and the drain given by $V_{GD} = V_{GS} - V_{DS}$ causing the channel to be ON and providing a reverse conduction path equivalent to that of the freewheeling anti parallel diode as in Si MOSFET. This reverse conduction path often called quasi freewheeling action [64] is established when

$V_{GS} - V_{DS} > V_{TH}$

$V_{DS} > -(V_{GS} - V_{TH})$ as depicted in *Figure* 2.18

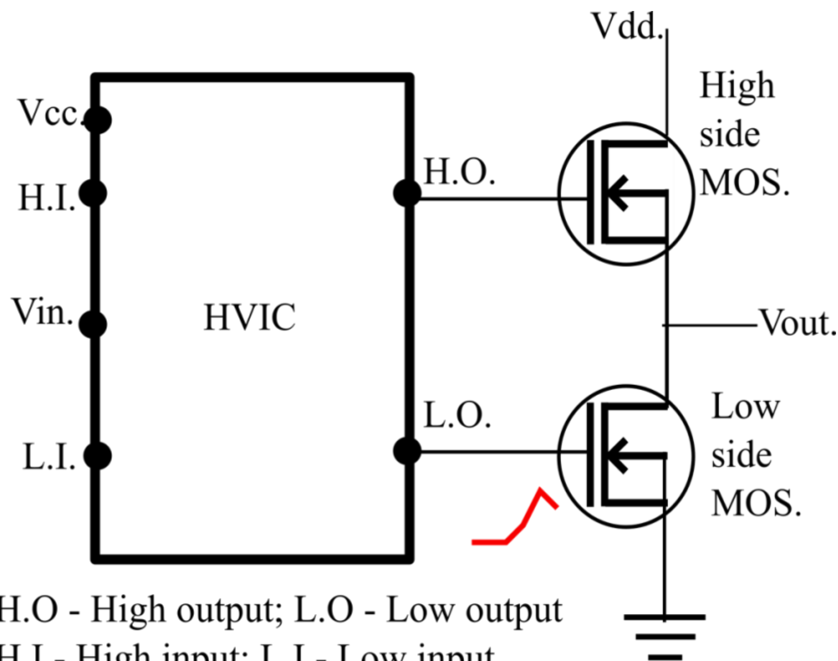



*Figure 2.17: Half bridge circuit driven by the Gate driver High Voltage integrated circuit*

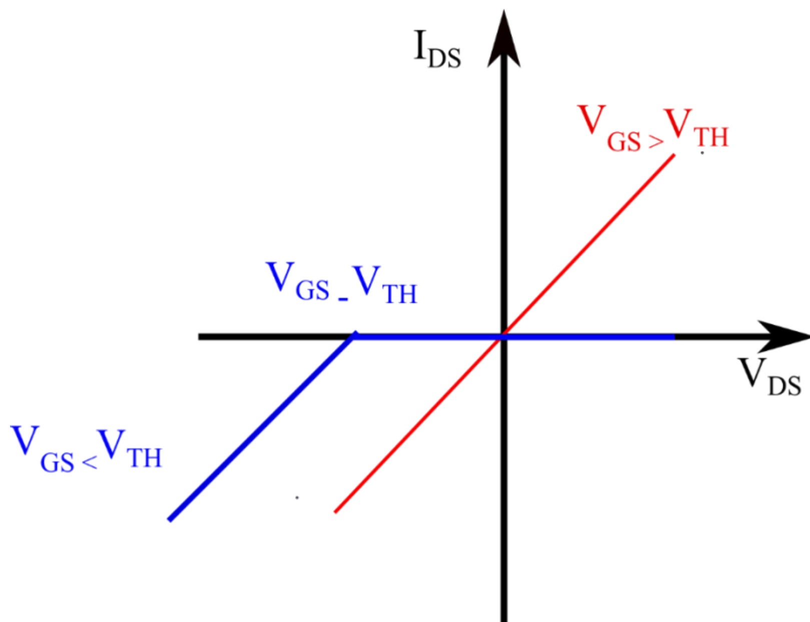



*Figure 2.18: Output characteristics of E- Mode HEMT showing reverse conduction characteristics*

When there is a positive threshold voltage shift the voltage at which the reverse conduction happens given by $V_{GS}$ - $V_{TH}$ increases, and this increase leads to higher dead time losses. To understand the impact of reverse conduction voltage on the dead time losses a hard switching topology-based buck converter with a resistive load as in *Figure* 2.19 is considered. The buck converter has MOSFETs in high side and low side switching

alternatively, the time period during which both the MOSFETs are intentionally OFF in the switching waveform to ensure safe operation is called the dead time. Dead time helps to avoid a situation where both the HSMOS and LSMOS are simultaneously ON causing a shoot through current causing device breakdown. There are 2 instances of dead time during each switching cycle, the first dead time instance (DT1) happens after the HSMOS is ON and before the LSMOS is ON, the second dead time (DT2) instance happens before the HSMOS is ON and after the LSMOS is ON as in *Figure* 2.20.

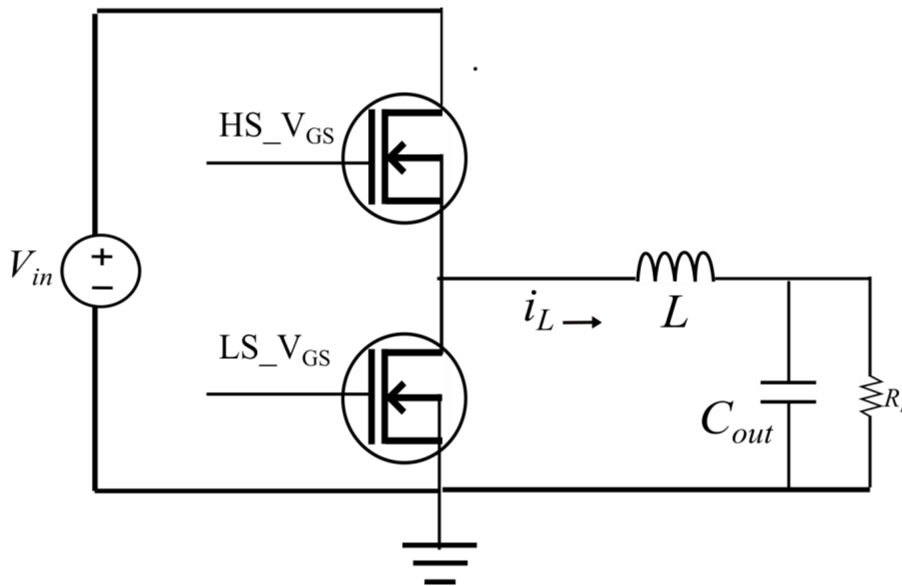



*Figure 2.19: Hard switching topology based buck converter with the half bridge circuit*

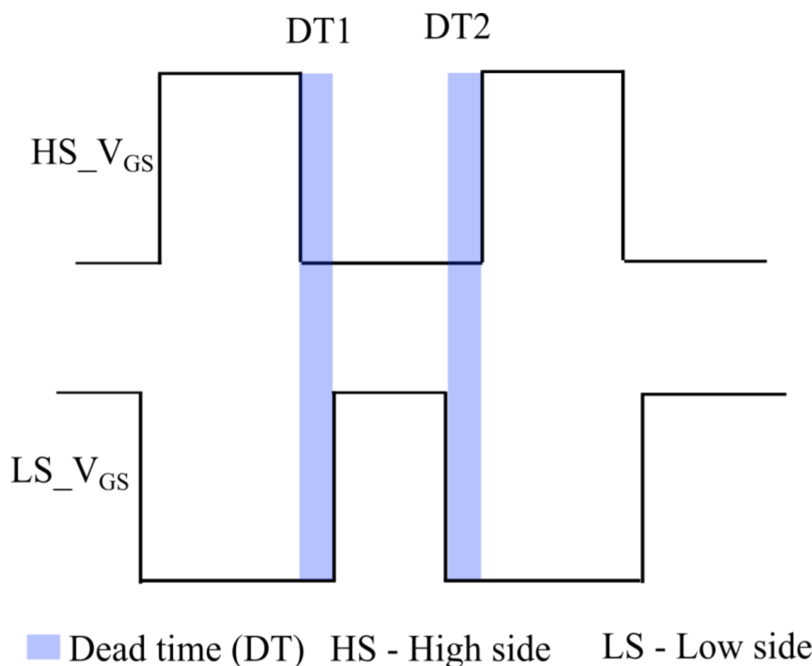



*Figure 2.20: Schematic showing two dead time instances per switching cycle of the buck converter*

During DT1 and DT2 the LSMOS reverse conducts as in *Figure* 2.21 and the power loss during the dead time is given by *eqn.* 2.11 *and eqn.* 2.12 *respectively*

$$P_{DT1} = V_{SD} * I_L * (T_{DT1} - T_f) * f_{sw} \tag{2.11}$$

$$P_{DT2} = V_{SD} * I_L * T_{DT2} * f_{sw} \tag{2.12}$$

Where $V_{SD}$ – voltage drop during the reverse conduction of GaN HEMT

$I_L$ - inductor current during the dead time

$T_f$ - rising time for the HSMOS $V_{DS}$

$f_{sw}$ – switching frequency

It takes some time for the LSMOS output capacitance which has been charged by Vin during the preceding HSMOS on pulse to discharge. This time ($T_f$) is being subtracted from the dead time as in *eqn.* 2.11. Total dead time loss is given by $P_{DT1} + P_{DT2}$ which shows the direct correlation of the reverse conduction voltage ($V_{SD}$) to the dead time losses.

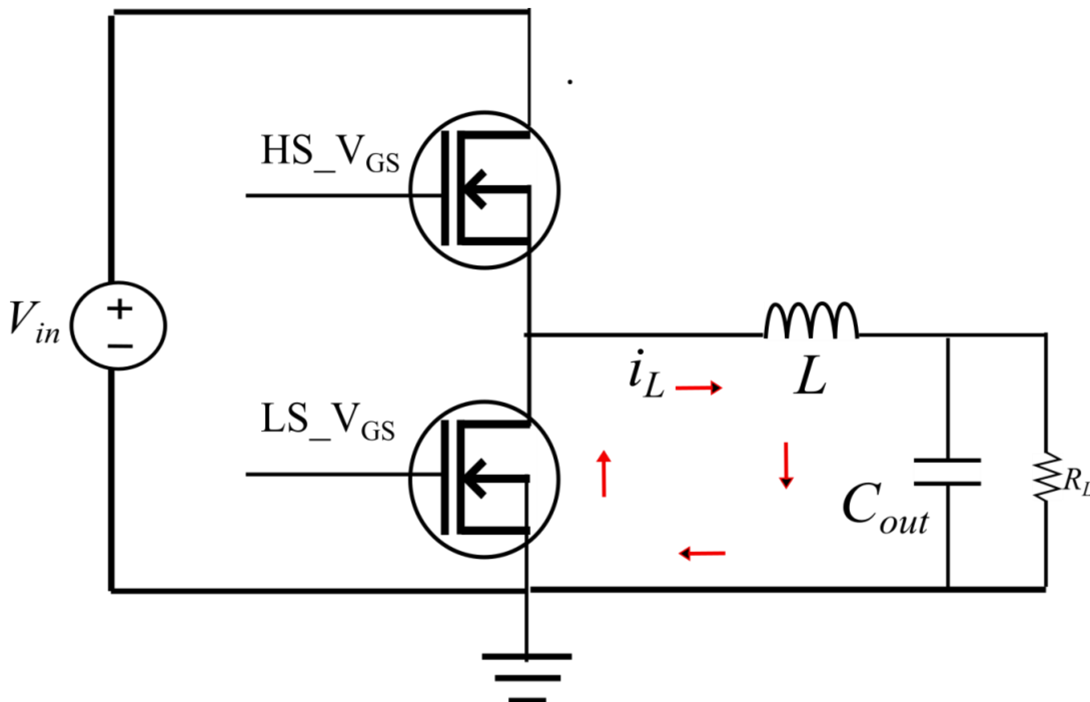



*Figure 2.21 Dead time reverse conduction path of L.S. MOS in the Buck converter causing conduction losses*

The dead time conduction mechanisms can change based upon the synchronous, asynchrous, soft switching and hard switching topologies. The above example illustrates the increased dead time losses due to the increased reverse conduction voltage.

## 2.8 Conclusion

- Gallium Nitride is based on a non-centrosymmetric wurtzite crystal lattice having a polarisation potential and can form high quality heterostructures. $Al_xGa_{1-x}N/GaN$ heterostructure due to its lattice mismatch, band discontinuity and polarisation induced interface charges forms a channel of electrons with high density (of the order of $10^{13}$ $cm^{-2}$) and high mobility (up to 2000 $cm^2/Vs$) at the heterointerface called a 2-dimensional electron gas (2-DEG).
- The 2-DEG channel formed at the AlGaN/GaN interface can be used to realise a _normally ON high electron mobility transistor with an ohmic source, drain and Schottky/Ohmic gate. Normally OFF transistors are preferred in power electronics for fail safe, reliable operations.
- Normally off transistors are realised by various device architectures, where the 2-DEG below the gate region is depleted and can be controlled by a gate potential. Magnesium doped GaN cap layer on top of the $Al_xGa_{1-x}N/GaN$ heterostructure depletes the 2-DEG formation and is the most adopted normally off HEMT architecture.
- Owing to traps, reliability of GaN based HEMT devices is challenging. Dynamic threshold voltage ($V_{TH}$) is a one such reliability concern where due to the nominal operational ON and OFF state bias stresses the $V_{TH}$ shifts positively or negatively.
- Positive $V_{TH}$ shift in normally off p-GaN/AlGaN/GaN on Si HEMTs lead to increased reverse conduction voltage, hence increased dead time losses, and mandates a relatively large gate drive voltage to turn on the device fully & suppress the effect of dynamic ON – resistance. Negative $V_{TH}$ shift in normally off p-GaN/AlGaN/GaN on Si HEMTs lead to faulty turn on during the turn off transient.

# 3. TCAD simulations and trap modelling

*Sentaurus TCAD solves the device equations self consistently on the discrete mesh in an iterative fashion. For each iteration an error is calculated, and the software attempts to converge at a solution numerically. This chapter describes the sentaurus simulation work bench, the respective integrated models used in this thesis for simulating the normally off p-GaN AlGaN/GaN on Si HEMTs. Traps constitute a centric role in the reliability studies of HEMTs and the basics of traps, their physical understanding, and their means of modelling is also summarised.*

## 3.1 TCAD simulations

It is a common practice in the field of semiconductor devices to use simulations to understand device operations, predict device behaviour for continuous improvement, development, and optimisation of semiconductor technology & devices. Synopsys, Technology Computer Aided Design (TCAD) is a simulation software based on finite element technique used to model process (process TCAD) and devices (device TCAD). In this thesis we have used sentaurus device simulations to model normally off p GaN gate AlGaN/GaN on Si HEMTs to understand the underlying physical mechanisms associated with the threshold voltage instability. TCAD sentaurus solves a set of physical partial differential device equations self – consistently in an iterative fashion at each point in the grid of the discrete mesh created on the device. For each iteration an error is calculated and sentaurus device attempts to converge at a solution. TCAD solvers typically solve on each grid point for a) electrostatic potential via Poisson's equation *Eqn.* 3.15 b) electron concentration c) hole concentration via the electron *(Eqn.* 3.3) and hole continuity equations (*Eqn.* 3.4). On a physical device, electrostatic potential translates to voltage and the net charge flux (holes – electrons) translates to electric current and the electric field could be estimated from the distribution of the mobile charges in the device and can be calculated by the gradient of the electrostatic potential given by $-\nabla * \psi$

$$\epsilon * \nabla^2 * \psi = -Q \qquad 3.1$$

$$Q = q(n - p + N_d^+ - N_a^-) \quad 3.2$$

In equation 3.1, 3.2, $\epsilon$ is the material dependent permittivity, $\psi$ is the electrostatic potential, Q is the net charge, q is the electronic charge, n/p are concentration of electron and hole respectively, $N_d^+$ / $N_a^-$ are the concentration of the ionised acceptor and donor impurity atoms.

$$\frac{dn}{dt} = \frac{1}{q}\nabla * \left(q\mu_n n\varepsilon + qD_n\frac{dn}{dx}\right) \quad 3.3$$

$$\frac{dp}{dt} = \frac{1}{q}\nabla * \left(q\mu_p p\varepsilon + qD_n\frac{dp}{dx}\right) \quad 3.4$$

The continuity equations 3.3 3.4 has two components contributing to the carrier transport, a drift component arising due to the electric field ($q\mu_{p/n}p\varepsilon$) and the diffusion component ($D_{n/p}\frac{dn}{dx}$) arising from the concentration gradient of the carriers; where $\mu_n$ , $\mu_h$ corresponds to the mobility of electron and holes respectively, $\varepsilon$ is the electric field and $D_n, D_p$ corresponds to the diffusivity of the electrons and holes. The numerical simulation starts with predicting the solution by solving the Poisson equation at equilibrium conditions or conditions defined in prior and then apply the respective bias conditions as the simulation proceeds. If the error is large, then the solution is increased/decreased by a factor. This deep physical approach gives TCAD a predictive approach. Device simulations can be transient or quasi stationary. Transient simulations are based on time, where the device simulated is being solved at each time instance under stationary conditions and while the device is ramped with respect to time, the device equations are resolved with the previous state being taken as the new stationary condition. Whereas quasi stationary simulations are steady state simulations where each parameter, property of the system and its partial derivative with respect to time is zero. During a quasi-stationary simulation when the device is ramped from one point to other, the boundary conditions (typically voltage, current or temperature) change with previous state having less significance compared to the next. Choice of the type of simulation depends upon the predominant physical mechanism which we try to investigate or happens in the device. As we analyse the physical mechanisms involving the trapping and de-trapping of the 2-DEG electrons in GaN HEMT we use transient

simulations in this thesis. GaN based heterojunction device simulations are complex [65] and challenging (poor convergence) in comparison to the silicon devices due to a) Piezo polarisation effects b) wide band gaps c) abrupt hetero interfaces d) non-linear distribution of traps and their properties. However, TCAD simulations still constitute a key part of research to validate the physical mechanisms behind the anomalous behaviour observed. The next few sections detail the key models used in the simulations in this thesis.

### 3.1.1 p-GaN doping and AlGaN/ GaN on Si heterostructure modelling

Magnesium doped GaN cap layer (p-GaN) on AlGaN/GaN on Si heterostructure in gate stack enables depletion of 2-DEG at AlGaN/GaN interface making the HEMT normally OFF. Mg in the GaN cap layer out diffuses into the AlGaN/GaN layers in the gate stack [66] and introduces an energy level 170-250meV [66] from the valence band in p-GaN/AlGaN/GaN layers. At room temperature Mg is not fully ionized as Mg dopant energy level is > 3*KT ~ 75meV from valence band. In addition to that, Mg atoms may be passivated by Hydrogen (H) atoms[67] or it could be self-compensated due to deep donor states attributed to Nitrogen vacancies [68]further reducing the net activation of Mg dopants. A doping efficiency of ~ 70% with a net acceptor concentration of $1.8x10^{19}$ $cm^{-3}$ is reported for a Mg incorporation of $3x10^{19}$ $cm^{-3}$ by [65],constant efforts are undertaken to improve the Mg activation ratio[70], [71]. To consider partial ionisation of Mg and to take into account the changes in activation due to electric field, Mg doping is introduced as a single acceptor trap energy level 170meV from valence band. Trap density equivalent to the total Mg incorporated is introduced as detailed in chapter 5.7. This acceptor trap energy level on ionisation become negatively charged contributing a hole to the valence band equivalent to that of an activated Mg dopant. The out-diffusion effect in the AlGaN/GaN layers in gate stack is created by physical model interface introducing a gaussian distribution of acceptor traps as detailed in chapter 6.6. Gate metal contacting the p-GaN cap layer can be Ohmic or Schottky type. Schottky contact in comparison to ohmic contact provides a higher threshold voltage and relatively larger gate turn on (~8V) which allows a wider range of gate bias operation [102]. Nonetheless both type of contacts are adopted by different manufacturers for different use cases. Schottky contact is modelled by a Schottky barrier with suitable carrier tunnelling mass and ohmic contact is modelled by having no barrier in contact. Fixed charges were

included in the TCAD simulation deck according to Ambacher et. al. [18] to consider the piezo-polarisation effect observed at the heterojunction interfaces p-GaN/AlGaN/GaN. A buffer layer is used to allow a high quality GaN layer to be grown despite the significant lattice mismatch between GaN and Si. Buffer layer is modelled with a little effort put into achieving an accurate representation of this buffer layer.

### 3.1.2 Contacts and 2-DEG modelling

Sentaurus TCAD permits users to specify contacts as either Ohmic or Schottky. Additionally, when a Schottky electrode is chosen, users can further specify the metal work function. The calculation of electrode charge varies based on the contact surface i.e., whether it made on an insulator or a semiconductor. When the electrode makes contact only with an insulator region, the simulator calculates the charge from Gauss's law and it represents the charge that would sit on the surface of a real contact to the device. When an electrode makes contact with a semi-conductor region, though the charge is calculated from Gauss's law, the Gaussian surface used for integration includes the doping well associated with the electrode. Here, the electrode charge includes the space charge in the doping well in addition to the charge that sists on the electrode [82]. Addition of lump or distributed contact resistance to the contacts as required is also possible. The polarisation induced charges at the hetero interfaces which cause the formation of the 2-DEG in the AlGaN/GaN heterostructure are modelled based on equations 2.6, 2.7. Fixed charges were included in the TCAD simulation deck. The polarisation charges in the transition layer, back barrier layers are suitably changed to match the experimental characteristics as the details of the multiple layers are not known in off the shelf devices used in this work. Sentaurus device manual [72] is referred for the inclusion of the listed models in the sentaurus work bench.

### 3.1.3 Transport models

The transport model in the GaN heterostructures define the transport of the carriers across the abrupt interfaces and discontinuous conduction and valence bands that are prevalent in hetero junctions. The following are the principal models used in semiconductor devices

**a) Drift diffusion model**

The default carrier transport model in Sentaurus is the drift-diffusion model. The current densities for electrons and holes, in this model, are given by

$$\vec{J}_n = \mu_n(n\,\nabla E_c - 1.5nkT\nabla\ln(m_n)) - D_n(\nabla_n - n\nabla\ln\gamma_n) \quad 3.5$$

$$\vec{J}_p = \mu_p(p\,\nabla E_v - 1.5nkT\nabla\ln(m_p)) - D_p(\nabla_p - p\nabla\ln\gamma_p) \quad 3.6$$

where $\mu$ = carrier mobility ($cm^2/Vs$), n, p = electron, hole carrier density ($cm^{-3}$), k = Boltzmann constant (J/K), $E_c$, $E_v$ = conduction, valence band energy level (J), T = temperature (K). Note that for Boltzmann statistics $\gamma_n = \gamma_p = 1$. Further, the Einstein relation, D = kT*μ provides the mobilities which define the diffusivities ($D_n$, $D_p$). The contribution due to the spatial variations of the electrostatic potential, the electron affinity, and the band gap are duly considered in the first term. The contribution due to the gradient of concentration, and the spatial variation of the effective masses $m_n$ and $m_p$ are accounted for by the remaining terms.

**b) Tunnelling model**

Tunnelling is defined as the phenomenon in quantum mechanics, where carriers tunnel through a potential barrier that is theoretically unsurmountable. Sentaurus offers three tunnelling models. The non-local tunnelling model is employed in this thesis not only because it is the most versatile but also due to its suitability when describing tunnelling at Schottky contacts and tunnelling in heterostructures [72]. These are scenarios of interest and will be discussed in more detail in the chapters that follow. Tunnelling conduction mechanism at a simple Schottky junction is illustrated in Fig. 3.2. The product of the carriers available to cross the barrier (n), the Richardson velocity ($v^R$) and the probability of tunnelling ($\Theta$) gives the tunnelling current density, according to the following equations [73].

$$\vec{J}_n = e\,v^R n\Theta \quad 3.7$$

$$\Theta = \exp\left(\frac{-4\sqrt{2em_n^*}\,\varphi_b^{3/2}}{3h\xi}\right) \quad 3.8$$

where $\phi_b$ is the barrier height, $m*$ is the effective electron mass and $\xi$ is the electric field within the potential barrier.

#### c) Thermionic emission model

The carrier transport model through which charge carriers (electrons or holes) are transported across a potential-energy barrier, that arises due to the conduction band or valence band discontinuity or built in electric fields, by the thermal energy gained, is referred to as the thermionic emission model. The thermal energy gained should be sufficient for the carriers to cross the barrier, that is equivalent to the work function of the material. The thermionic current density can be expressed as [73]

$$\vec{J}_n = e v^R N_c \exp\left(-\frac{e\Phi_b}{kT}\right)\left[\exp\left(\frac{eV_a}{kT}\right) - 1\right] \quad 3.9$$

where $\Phi_b$ is the barrier height and $V_a$ is the external voltage applied to the barrier. Richardson velocity, the average velocity with which the electrons reach the barrier, is denoted by $(v^R)$ and is equal to $\sqrt{kT/_{2\pi m_n}}$, with $m_n$ is the electron mass. It can be observed from *Eqn.* 3.9 that thermionic emission probability of an electron across a barrier exponentially increases with rise in temperature, as the barrier height reduces with increase in applied potential.

### 3.1.4 Mobility models

The speed with which an electron or hole can move through a metal or semiconductor, when pulled by an electric field is defined as carrier mobility. Saturation velocity is the maximum velocity that carriers can attain in the presence of high electric fields. Mobility field dependence can be modelled in several ways in Sentaurus. *Eqn 3.11* describes one such model, the Extended Canali high field saturation model [84]. This model the default choice in Sentaurus and one that is commonly used in Silicon device simulations.

$$\mu = \frac{\mu_0}{\left[1 + (\frac{\mu_0 F}{v_{sat}})^{\beta}\right]^{1/\beta}} \quad 3.10$$

where $\mu_0$ = mobility at low fields, F = driving field, $v_{sat}$ = electron saturation velocity. According to Monte Carlo calculations [74], GaN should exhibit velocity

overshoot and therefore a negative differential mobility. Sentaurus TCAD provides a model for III-nitride materials called as Transferred Electron Model 2 which describes this effect. This model was used in the HEMT TCAD model described in Chapter 4. A constant mobility model is a simple mobility model that has no field dependence, and accounts only for phonon scattering effects[72] This model is available when the field effects are not a subject of investigation. Here mobility is only dependent on the lattice temperature which is a valid assumption provided 2-DEG channel is in a region of low doping and the electric fields present under on-state conditions are not too high in the operation of a Schottky diode. The following equation describes the constant mobility model:

$$\mu = \mu_L \left(\frac{T}{300K}\right)^{\zeta} \tag{3.11}$$

where T is temperature in K, μL = mobility at room temperature and ζ = mobility exponent.

### 3.1.5 Mesh

In order to ensure reliability of TCAD simulation results, a proper mesh definition is necessary. If the mesh is not refined to the required extent, results may be less reliable, or it may give rise to convergence issues. Whereas, if the mesh is refined in excess, the time taken to complete the simulations might increase by a large extent. The key is to define a very refined mesh at important points such as the hetero-junction, Schottky contacts and regions of high electric field and a coarser mesh at bulk regions. This is illustrated in *Figure* 3.1 which shows a sample mesh definition in a TCAD model and the increased refinement at significant regions of the structure. The location highlighted shows the region below the gate stack where the interest of simulation was present

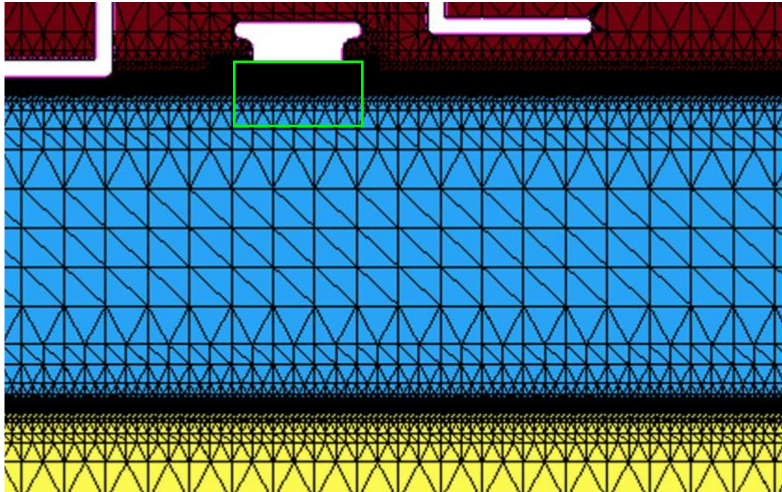


*Figure 3.1: Meshing of the p-GaN gate device during the TCAD simulation*

## 3.2 Physical understanding of traps and its types

To comprehend the device failure mechanisms and improve the reliability of the normally off p GaN gate AlGaN/GaN on Si HEMTs it is essential to understand the location, type, source, and physicality of the traps in the device. During material growth or device processing, due to the chemical, physical and temperature effects, defects are prone to happen. Defects can be interpreted as a perturbation to the periodic potential of the crystal lattice which translates into an electronic energy level in the bandgap of the semiconductor. For example, GaN growth on lattice matched sapphire leads to dislocation densities of $10^8$ to $10^{10}$ $cm^{-2}$. Such defects in the device act as trapping centres which can in turn capture electrons or holes and after some dwell time have the possibility to emit/detrap the carriers. This trapping and detrapping of the carriers can alter the electrical characteristics of the device and if it happens in an uncontrolled manner, it can be detrimental to the performance and the reliability. There are 2 types of traps

a) Donor like traps
b) Acceptor like traps

Donor like traps are neutral when fully occupied and become positively charged after donating an electron (*Figure* 3.2*)*. Donor like traps can trap or emit an electron or hole correspondingly identified as 'donor like electron trap', 'donor like hole trap' respectively. Acceptor like traps are neutral when empty and become negatively charged after accepting an electron as shown in *Figure* 3.2.

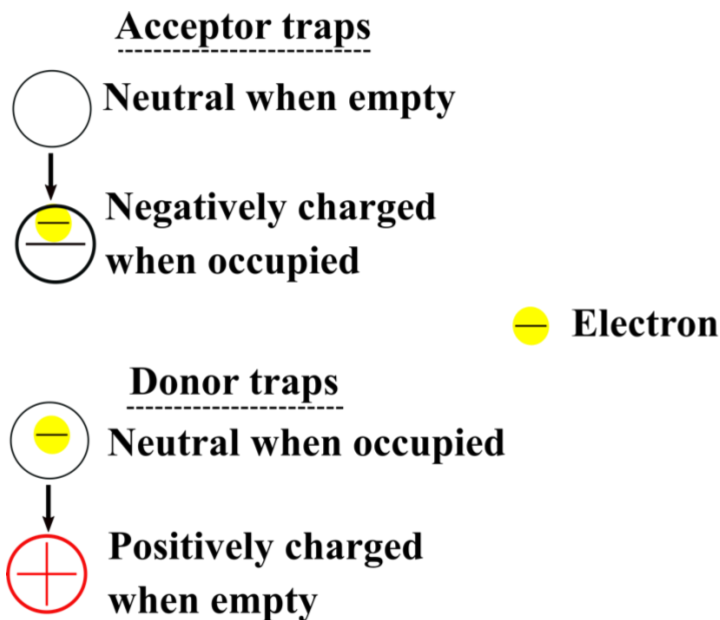



*Figure 3.2: Illustration of the donor and acceptor traps and their state of charge*

A trap is classified as acceptor like or donor like based on its charging state post trapping and de-trapping.

### 3.3 Trap dynamics - its capture and emission metrics

The trapping of the carriers can be described as a sequence of below processes

a) Charge injection
b) Trapping
c) Detrapping

Electron trapping/detrapping appears in the conduction band whereas hole trapping/detrapping appears with the valence band. Capturing a hole means that trap delivers an electron to valence band and emitting a hole means that a trap captures an electron from the valence band. The probability of a trap center trapping/capturing an electron or hole depends upon the capture coefficient of electrons ($\boldsymbol{c_n}$) and holes ($\boldsymbol{c_p}$) respectively. And a trap center detrapping/emitting an electron or hole depends upon the emission coefficient of electrons ($e_n$) and holes ($e_p$) respectively. Those traps that emit or capture electrons are electron traps and ones that emit, or capture holes are hole traps as in *Figure* 3.3.

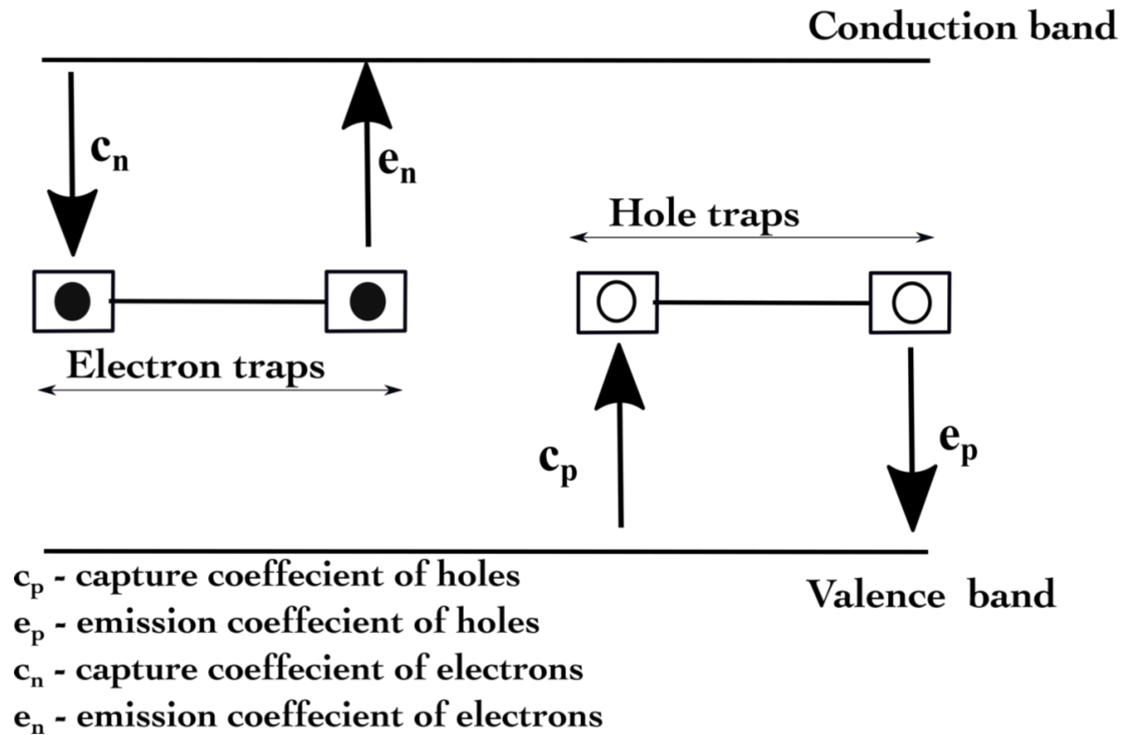



*Figure 3.3 Illustration of the electron traps and hole traps emitting and capturing carriers*

The capture coefficient has the unit $cm^3/s$ and the emission coefficient has the unit 1/seconds. The electron capture coefficient ($c_n$) is given by the product of the electron capture cross section ($\sigma_n$) of the trap center and the electron thermal velocity ($v_{th}$) as in *eqn.* 3.12. Thermal velocity ($v_{th}$) is inversely proportional to the electron density of states effective mass as in *Eqn.* 3.13. On the other hand, the emission coefficient ($e_n$) is inverse of the emission time ($\tau_e$) as in *Eqn.* 3.14. It is to be noted that the capture cross section of the trap center measured in $cm^2$ varies depending upon whether it is neutral, negative or positively charged. If the trap center is charged such that it is coulombic repulsive for the carrier to be captured, then the capture cross section would be small. if the trap center is charged such that it is coulombic attractive for the carrier to be captured then the capture cross section is large implying that capture cross section is a dynamic parameter

$$c_n = \sigma_n * v_{th} \tag{3.12}$$

$$v_{th} = \sqrt{\frac{3KT}{m_n}} \tag{3.13}$$

$$e_n = \frac{1}{\tau_e}; \quad e_p = \frac{1}{\tau_p} \tag{3.14}$$

The mathematical analysis of the kinetics of the traps is predominantly based on the Shockley - Read - hall defect model [75]. To understand the dynamics further it is essential to quantify the processes in terms of the time taken to capture the carriers and the time taken to emit the trapped carriers and the parameters that influence them. A semiconductor as in *Figure* 3.4 where donor energy level ($E_D$) close to the conduction band, acceptor energy level ($E_A$) close to the valence band is assumed thereby causing a complete ionisation with $N_D = N_D^+$ and $N_A = N_A^-$ . '$N_T$' is the total trap density which is partially filled and partially empty where $n_T$ denotes the fraction of $N_T$ that is filled and $p_T$ denotes the remaining empty trap canters. The electron capture probability is directly proportional to the electron density in the conduction band, (n) density of holes ( $p_T$) on trap energy level ($E_T$) and the capture rate of electrons is given by *Eqn.*3.9

$$R_c^e = C_n n p_T \quad 3.9$$

where $c_n$ as constant of proportionality factor is the electron capture coefficient ($cm^3/s$). On the other hand, the electron emission rate as given by *Eqn.* 3.10 depends on the trapped electron density and is independent of the electron density with $e_n$ being the emission coefficient with unit 1/s.

$$R_e^e = e_n n_T \quad 3.10$$

Similarly, the hole emission rate and the capture rate is given by *Eqn.3.11*

$$R_c^p = C_p p n_T; \quad R_e^p = e_p p_T \quad 3.11$$

The electron time rate of change in the conduction band due to trapping is given by the difference of emission rate and capture rate of electrons, in a similar way hole time rate of change in the valence band is given by the difference of emission rate and the capture rate of the holes as in *Eqn. 3.12, 3.13* respectively

$$\frac{dn}{dt} = R_e^n - R_c^n = e_n n_T - C_n n p_T \quad 3.12$$

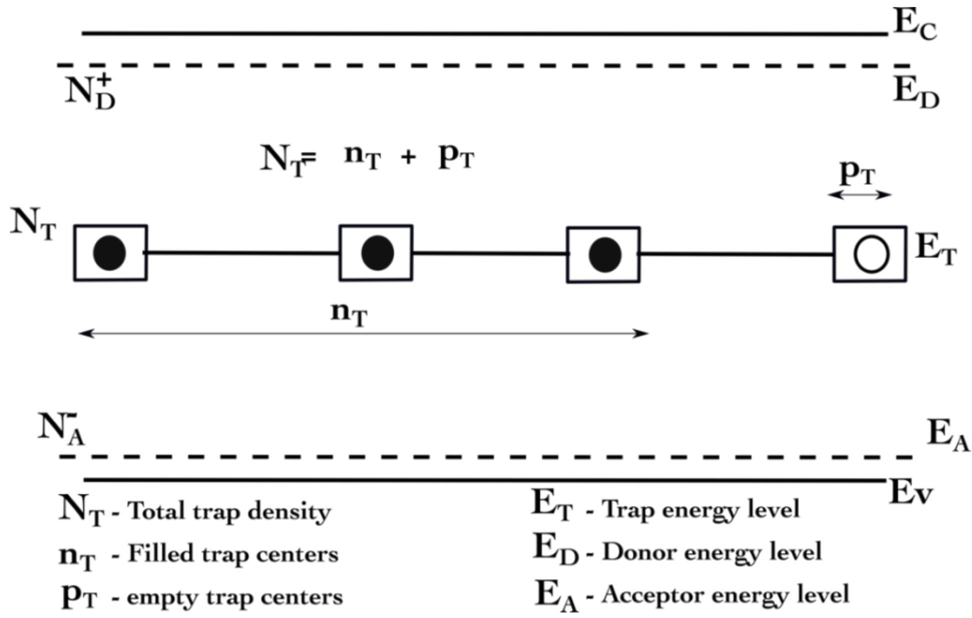



*Figure 3.4: Trap dynamics, capture and emission of electrons and holes*

$$\frac{dp}{dt} = R_e^p - R_c^p = e_p p_T - C_p p n_T \quad (3.13)$$

$$\frac{dn_T}{dt} = \frac{dp}{dt} - \frac{dn}{dt} = (C_n n + e_p)(N_T - n_T) - (C_p p + e_n)n_T \quad (3.14)$$

Trapping and detrapping leads to change in the trap occupancy, the net change in the trapped electron density is given by the rate of change of the filled trap energy levels as in *Eqn. 3.14*. This non-linear equation has 4 variables of which capture, and emission coefficients are unknown and n, p are the electron/ hole concentration which vary with time, electric field. Depending upon the field conditions (quasi-neutral region, space charge region) suitable boundary conditions assuming steady state conditions or equilibrium conditions are applied, and the above equation is numerically solved to calculate the emission and capture coefficients. Using these emission time could be back calculated. Assuming an equilibrium condition where principle of detailed balance is assumed the emission time and capture time is given by *Eqn.3.15* [76]

$$\tau_{e,n} = \frac{\exp(E_C - E_T)/\text{KT}}{\sigma_n * v_{th} * N_c}; \qquad \tau_{e,p} = \frac{\exp(E_T - E_v)/\text{KT}}{\sigma_p * v_{th} * N_v} \quad (3.15)$$

$$\tau_{c,e} = \frac{1}{\sigma_n * v_{th} * n}; \qquad \tau_{c,p} = \frac{1}{\sigma_n * v_{th} * p}$$

Where $\tau_{e,e}$ is the emission time of the electron, $\tau_{e,p}$ is the emission time of the hole, $\tau_{c,e}$ is the capture time of the electron, $\tau_{c,p}$ is the capture time of the hole, $N_c$ is the effective density of states in the conduction band, $N_v$ is the effective density of states in the valence band, $E_T$ is the trap energy level, K is the Boltzmann constant and T is the temperature, $\sigma_n$ is the electron capture cross section of the trap center and $v_{th}$ is the electron thermal velocity. 'n' is the concentration of electron in the conduction band and 'p' is the concentration of the hole in the valence band. It is to be noted that the capture time is inversely proportional to the capture cross section, thermal velocity and the number of carriers available for capture. And the emission time has an exponential dependence on the relative position of the trap energy level with respect to the conduction band or valence band and inversely proportional to the capture cross section, thermal velocity and the effective density of states available to emit. If the trap energy level is close to the conduction band it can easily emit an electron yielding smaller emission time. These transition processes can take time ranging from nanoseconds to seconds to days. Trapping and detrapping are closely related to

a) Spatial distribution of the traps
b) Trap distribution in terms of energy depths.
c) Trap density

Spatial distribution of traps denotes the trap distribution profile in the case of multiple or quasi continuous traps. These traps can be uniformly distributed in a range of energy levels (Eg: 0.25eV to 0.45eV from the conduction band edge) or can have a gaussian distribution profile or a listed non uniform profile at various energy levels. At times based on the diffusion gradient of the impurities which contribute to the trap energy levels the traps can be described matching the diffusion gradient spatially

Trap distribution by energy depth denotes the position of the trap energy level/s with respect to the conduction band edge or the valence band edge or the intrinsic energy level. It varies in a semiconductor depending upon the physical, thermal, chemical processes causing the defects and the position of these defect complexes in the crystal lattice. For instance, defects at the surface mostly cause donor like or acceptor like shallow trap energy levels (exceptions do exist). Surface atoms in general have fewer bonding partners than bulk atoms giving rise to electronic energy levels close

to that of the free atoms which is either more conduction band/acceptor like (at the *Figure* 3.5 bottom edge of the conduction band) or valence band/donor like (at the top edge of the valence band), the charging state of these surface energy levels is donor or acceptor like depending on proximity to the valence band or conduction band respectively. Certain impurities like Gold in silicon cause a deep level trap with the trap energy level almost in the midgap. Trap density denotes the density of traps at each energy level and will vary depending upon the energy depths [77]. The capture time is usually much shorter than the emission time and using CV measurements, combined with the capture pulse, the capture cross section is calculated in each device, for a respective condition.

There are three common mechanisms as in by which emission of trapped electrons happen, these emission mechanisms are strongly influenced by the electric field. Poole Frenkel (PF) is a mechanism where the electron surmounts a barrier lowered by the presence of the electric field; Direct tunnelling (DT) is a mechanism by which the electrons tunnels through the barrier and crosses the barrier which is likely to happen only at high electric fields of the order $10^7$ V/cm; Phonon assisted tunnelling (PAT) is a mechanism where the electron absorbs thermal energy from the lattice and then tunnels through the barrier at a higher energy. Electric field significantly increases the probability of these mechanisms happening and thus increase the emission coefficient and thereby reduce the emission time.

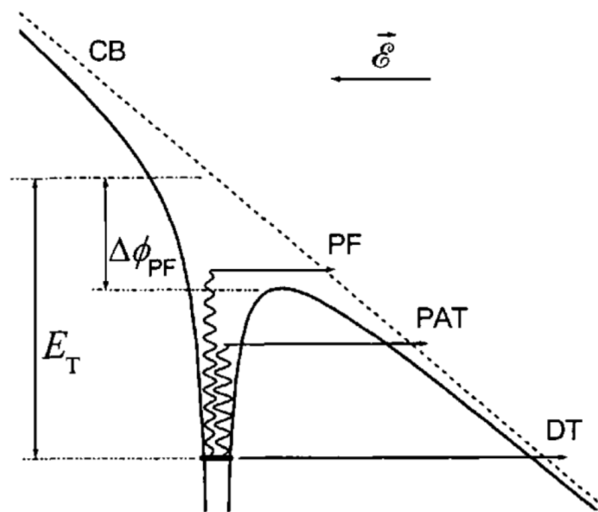



*Figure 3.5: Common electron emission mechanisms post trapping event at an electric field [78]*

With this detailed introduction of traps, trapping and detrapping how these processes contribute to threshold voltage instability and their recovery is covered in chapter 5, 6, and 7.

## 3.4 Trap TCAD modelling - Statistical and energetic distribution of traps

Using sentaurus device we can add traps as the following type a) electron traps b) hole traps c) fixed charges with different energetic distribution like a) level b) uniform c) exponential d) gaussian and e) table. The various distribution of traps and the parameters are shown in *Figure* 3.6. The keywords Level, Uniform, Exponential, Gaussian, and Table determine the energetic distribution of traps. The keywords select a single-energy level, a uniform distribution, an exponential distribution, a Gaussian distribution, and a user-defined table as given by equations

$$N_0 \quad \text{for } E = E_0 \ \text{ for level} \tag{3.15}$$

$$N_0 \ \text{ for } E_0 - 0.5E_0 < E < E_0 + 0.5E_s \ \text{ for uniform}$$

$$N_0 \exp\left(-\left|\frac{E-E_0}{E_s}\right|\right). \quad \text{For exponential}$$

$$N_0 \exp\left(-\frac{(E-E_0)^2}{2{E_s}^2}\right). \quad \text{For gaussian}$$

$$\{N_1 \ldots\ldots N_m \ for\ E = E_1 \ldots\ldots for\ E = E_m \ \text{ for table list of traps}$$

Where $N_0$ is the concentration in $cm^{-3}$ for level distribution and for other distributions it is $eV^{-1}cm^{-3}$ or $eV^{-1}cm^{-3}$. If the traps are defined in the bulk region it is $eV^{-1}cm^{-3}$ on the other hand if these traps are defined in the interfaces they have a unit $eV^{-1}cm^{-2}$

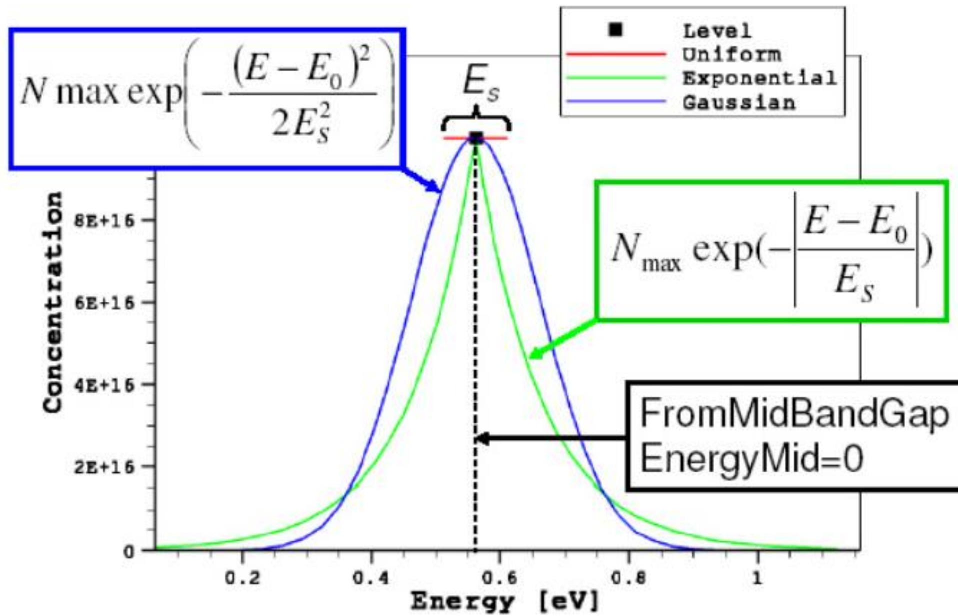



*Figure 3.6: Various Trap distribution schemes in the TCAD.*

*In this* way the traps can be energetically distributed. Physically they can be distributed to any profile by the physical model interface. In the case of normally OFF p-GaN gate HEMTs traps are often introduced in the surface of the access region between the gate and drain, in the buffer, in the gate stack surfaces to investigate various reliability mechanisms. The TCAD device structure and model for normally-off HEMT once built is validated by comparing the measured electrical parameters with the TCAD parameters.

## 3.5 Conclusion

- Technology Computer Aided Device (TCAD) simulations are finite element simulations which solve physical partial differential equations at each discretised mesh of semiconductor device to extract the electrostatic potential, electric field, electron, and hole concentration.
- Traps are physical defects in a semiconductor arising during processing which translate into electronic energy levels in the midgap of the semiconductor. Traps can be donor like, or acceptor like with varied spatial distribution, energy depth, trap density and capture cross section.

- The kinetics of trapping and detrapping is given by the Shockley - Read - Hall model and the time taken for the traps to capture the carriers (trapping) is called capture time and the time taken to emit the carriers (detrapping) is called the emission time.
- The capture time is inversely proportional to the capture cross section, thermal velocity and the number of carriers available for capture. And the emission time has an exponential dependence on the relative position of the trap energy level with respect to the conduction band or valence band, and inversely proportional to the capture cross section, thermal velocity, and the effective density of states available to emit.
- Traps can be simulated by TCAD simulation, and the physical distribution of the traps can be simulated by the physical model interface in TCAD, by which Gaussian distribution of traps is defined for the subsequent Mg out diffusion analysis.

# 4. Physical understanding of Threshold voltage and p-GaN/AlGaN/GaN gate stack

*This chapter analyses the gate stack of the normally off p-GaN HEMT for a physical understanding of the underlying dynamic charge balance at various interfaces and henceforth the normally OFF operation. The analytical expression for the potential at which the channel turns on for p-GaN HEMTs is reviewed. The significance of the trapping mechanisms in the gate stack which causes charge conditions altering the threshold voltage is discussed, paving foundations to understand Threshold voltage instability discussed in chapters 5,6.*

## 4.1 p-GaN gate stack charge balance and 2-DEG formation

The region below the gate comprising of metal, p-GaN, AlGaN barrier, GaN buffer, transitional layers and the silicon substrate influence the ON/OFF control of the gate. The p-GaN/AlGaN/GaN gate stack's charge dynamics significantly control the channel formation, channel sheet charge density, ON/OFF state control and hence the threshold voltage. p-GaN/AlGaN/GaN gate stack, as highlighted in *Figure* 4.1 is analysed further. To understand the build-up of the polarisation charge at the interfaces and subsequent charge balance in gate stack, GaN (undoped - U)/AlGaN/GaN $_{\text{buffer}}$ is reviewed first and later the effect of Mg doping forming p-GaN/AlGaN/GaN is reviewed.

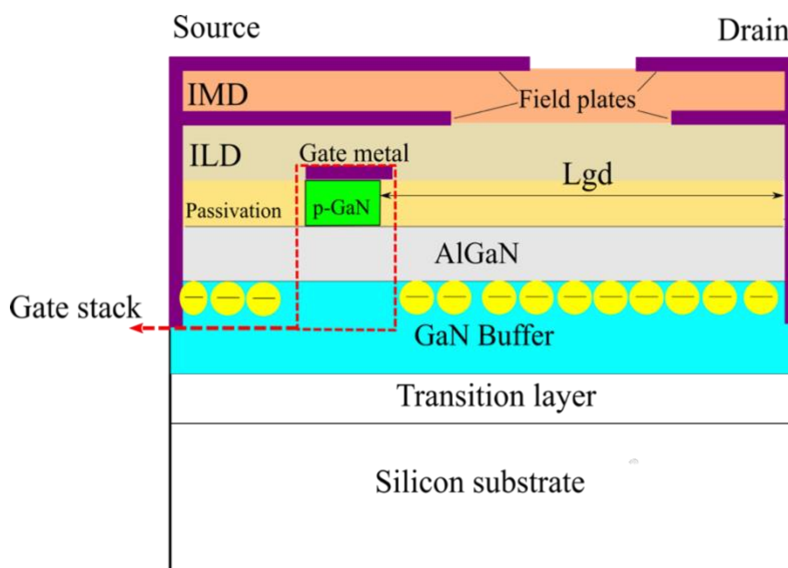



*Figure 4.1: Schematic of the normally off p-GaN/AlGaN/GaN on Si HEMT highlighting the gate stack*

The GaN/AlGaN/GaN stack is pictured with no bias under thermal equilibrium in *Figure* 4.2. Instead of polarisation charge dipoles the spontaneous and piezoelectric charge are segregated and represented for better understanding.

For sake of simplicity, charges in the buffer and AlGaN back barrier are ignored in this pictorial understanding. GaN/ $Al_xGa_{1-x}N$ /GaN $_{buffer}$ hetero structure will have spontaneous and piezoelectric polarisation charges formed during the process of epitaxial growth and cooling. The bound polarisation charges lead to spontaneous polarisation potential and the direction of the potential is same for Ga – face GaN, $Al_xGa_{1-X}N$, GaN – buffer layers as seen in (a) of *Figure* 4.2. The lattice mismatch causes a tensile strain in the $Al_xGa_{1-x}N$ layer and compressive strain in the GaN layer causing a piezoelectric charge built up. The polarity of the piezoelectric charge changes depending upon the type of strain as seen in (b) of *Figure* 4.2. The GaN buffer is assumed to be relatively thick as in real HEMTs, hence the strain effects and associated piezoelectric charge built up are negligibly small.

For further analysis it is essential to understand the charge dynamics at 3 interfaces

a) Interface 1 – GaN top surface (Metal/p-GaN interface after doping GaN cap layer)
b) Interface 2 - p-GaN/ AlGaN interface
c) Interface 3 - AlGaN/GaN interfaces

A disaggregated illustrative pictorial representation of the polarization charge build up and translation of these charges to free carriers in the gate stack is shown in Fig. 4.2 and 4.3. The suffix indices 'S' refers to spontaneous, 'P' refers to piezoelectric, 'pg' refer to p GaN, 'a' refer to AlGaN. 2-DHG or 2DHG = 2-dimensional hole gas, 2-DEG or 2DEG = 2-dimensional electron gas. Thus, the notations used in Figure 4.2, Figure 4.3 are interpreted as below

$\delta_{Sg}$ = **S**pontaneous polarisation charges/unit area in **G**aN

$\delta_{Spg}$ = **S**pontaneous polarisation charges/unit area in **p**-**G**aN

$\delta_{Sa}$ = **S**pontaneous polarisation charges/unit area in **A**lGaN

$\delta_{Pg}$ = **P**iezoelectric polarisation charges/unit area in **G**aN

$\delta_{Ppg}$ = **P**iezoelectric polarisation charges/unit area in **p**-**G**aN

$\delta_{Pa}$ = **P**iezoelectric polarisation charges/unit area in **A**lGaN

$\delta_{iMg/pg}$ = Equivalent sheet charge due to the ionised out diffused Mg dopants **in p-GaN**

$\delta_{iMg/a}$ = Equivalent sheet charge due to the ionised out diffused Mg dopants **in AlGaN**

$\delta_{2DEG}$ = Charge due to the 2-dimensional electron gas

$\delta_{2DHG}$ = Charge due to the 2-dimensional hole gas

$\sigma_{p1} = \delta_{Sg}$= The spontaneous polarization charges/unit area in GaN

$\sigma_{p2} = \delta_{Sa} + \delta_{Pa}$ = The net polarization charge at the AlGaN barrier

$\sigma_{p3} = \delta_{Spg} - \delta_{Ppg}$ = The net polarization charge at the p-GaN cap layer (assumption $\delta_{Spg} > \delta_{Ppg}$).

Field induced ionization of the out diffused Mg at the AlGaN barrier $\sigma_b = \delta_{iMg/a}$;

The non ideality of the crystal structure from GaN to AlN increases in terms of the anion – cation bond length along the (0001) axis in units of *c* (vertical axis), corresponding to an increase in the spontaneous polarisation [79]. Hence the spontaneous polarization induced charge density of AlN alloy, $Al_xGa_{1-x}N$ is higher than that of GaN making $\delta_{Sa} > \delta_{Sg}$. In the gate stack at the GaN(U)/ $Al_xGa_{1-x}N$ interface, a net negative polarization charge is present due to the differences in the spontaneous and piezoelectric polarisations as seen in (c) of *Figure* 4.2 and is given by *Eqn.*4.1

$$\text{Net -ve polarisation charge at the GaN/AlGaN interface} = -(\delta_{Sa} + \delta_{Pa}) + (\delta_{Spg} - \delta_{Ppg}) \quad 4.1$$

This net negative polarisation charge at the GaN(U)/ $Al_xGa_{1-x}N$ interface leads to the accumulation of the holes to compensate the negative charge as depicted by (e)(f) in *Figure* 4.2. These holes are quantum confined at the interface and is called the 2-dimensional hole gas (2-DHG). Similarly in the gate stack at the $Al_xGa_{1-x}N$ /GaN interface a net positive polarisation charge is present due to the differences in the spontaneous and piezoelectric polarisations as seen in (c) of *Figure* 4.2 and charge is by *Eqn.*4.2

$$\text{Net +ve polarisation charge at the GaN/ } Al_xGa_{1-x}N \text{ interface} = (\delta_{Sa} + \delta_{Pa}) - (\delta_{Sg}) \quad 4.2$$

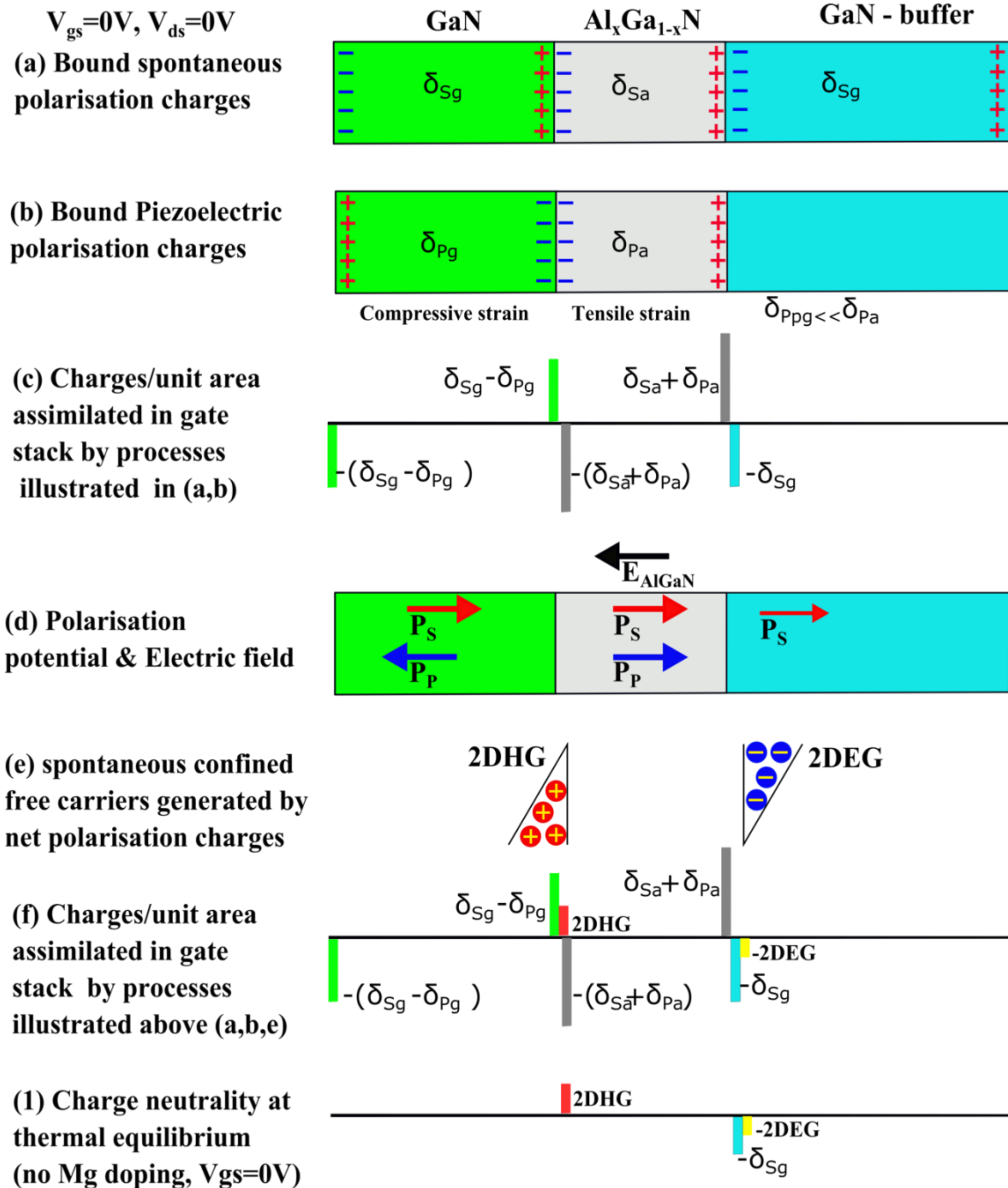



*Figure 4.2 : GaN/$Al_xGa_{1-x}N$/GaN heterostructure charge dynamics at zero bias*

This net positive polarisation charge at the $Al_xGa_{1-x}N$ /GaN interface leads to the accumulation of the electrons to compensate the positive charge. These electrons are quantum confined at the interface and is called the 2-dimensional electron gas (2-DEG).

Thus, 2-DHG density = - ($\delta_{Sa}$ + $\delta_{Pa}$) + ($\delta_{Spg}$ - $\delta_{Ppg}$) and 2-DEG density = ($\delta_{Sa}$ + $\delta_{Pa}$) - ($\delta_{Sg}$). The charge neutrality in the GaN/AlGaN/GaN $_{buffer}$ including both the interfaces is

always maintained under equilibrium. Thus, the net charge in the GaN surface, GaN (U)/ $Al_xGa_{1-x}N$ interface and $Al_xGa_{1-x}N$ /GaN interface sums to 0 as in *Eqn.*4.3.

$$-(\delta_{Spg} - \delta_{Ppg}) + \delta_{2\text{-}DHG} -(\delta_{Sa} + \delta_{Pa}) + (\delta_{Spg} - \delta_{Ppg}) - \delta_{2\text{-}DEG} + (\delta_{Sa} + \delta_{Pa}) - (\delta_{Sg}) = 0 \qquad 4.3$$

Thus, the 2-DEG built up is balanced by the 2-DHG and the small spontaneous polarisation as illustrated in (g) of *Figure* 4.2. This enables the Normally ON (2-DEG channel present) operation in AlGaN/GaN heterostructure. The source of the electrons and holes for the formation of 2-DHG and 2-DEG is not well established. Electrons that form 2-DEG are predominantly believed to be from the surface traps at the AlGaN surface and the source of the holes is not clearly known.

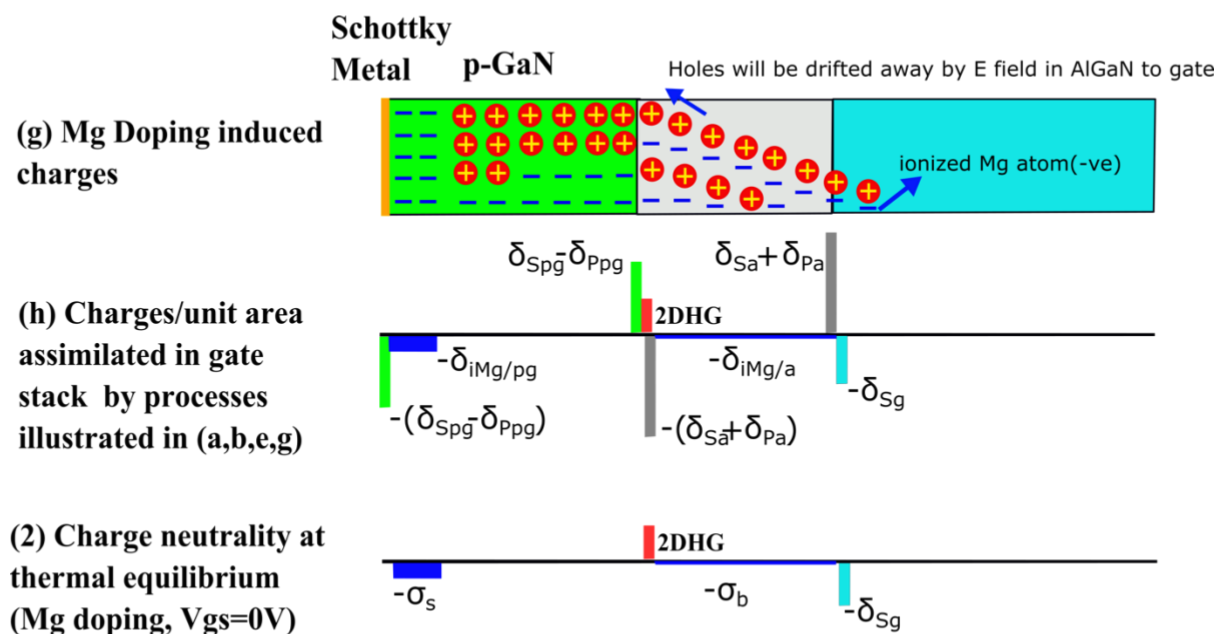



*Figure 4.3: p- GaN/AlGaN/GaN at zero bias depicting the charge balance in the gate stack*

To enable normally off operation (2-DEG channel absent without external gate potential) in GaN/ $Al_xGa_{1-x}N$ /GaN $_{buffer}$ heterostructure the GaN cap layer is doped with magnesium making it p type. The p – type magnesium doping at the metal/p-GaN interface, is completely ionized due to the Schottky barrier induced depletion region. Whereas in the middle of the p-GaN cap layer there is only partial Mg ionisation due to the lack of the electric field [80] being a quasi-neutral region. The charge dynamics for p-GaN/ $Al_xGa_{1-x}N$/GaN buffer at zero bias is pictorially illustrated in *Figure* 4.3. The magnesium atoms once ionised generate a net positive charge after the holes have been drifted by the field in the AlGaN region and in the Schottky barrier at the metal/p-GaN contact. This field induced ionisation of the out diffused Mg at the AlGaN barrier leads

to a negative charge - $\delta_{iMg/a}$ alias $-\sigma_b$. In a similar way the ionised Mg charge in the Schottky contact depletion region is given by $\delta_{iMg/pg}$ alias $-\sigma_s$. At equilibrium the charge neutrality is still maintained as shown in (2) of Figure 4.3 and is given by $-\sigma_b - \sigma_s + 2DHG - \delta Sg = 0$. It can be observed that due to Mg doping of GaN cap layer 2-DHG is compensated by ionized Mg $(-\sigma_b - \sigma_s)$ making it normally OFF. Whereas in the case undoped GaN cap layer (Fig. 4.2) the 2-DEG primarily compensates the 2-DHG which makes it normally ON. The transition from the normally ON operation to normally OFF operation in terms of band diagram is shown in *Figure* 4.4, where the p-GaN cap layer pulls up the AlGaN/GaN conduction band relative to the electron fermi level causing 2-DEG depletion.

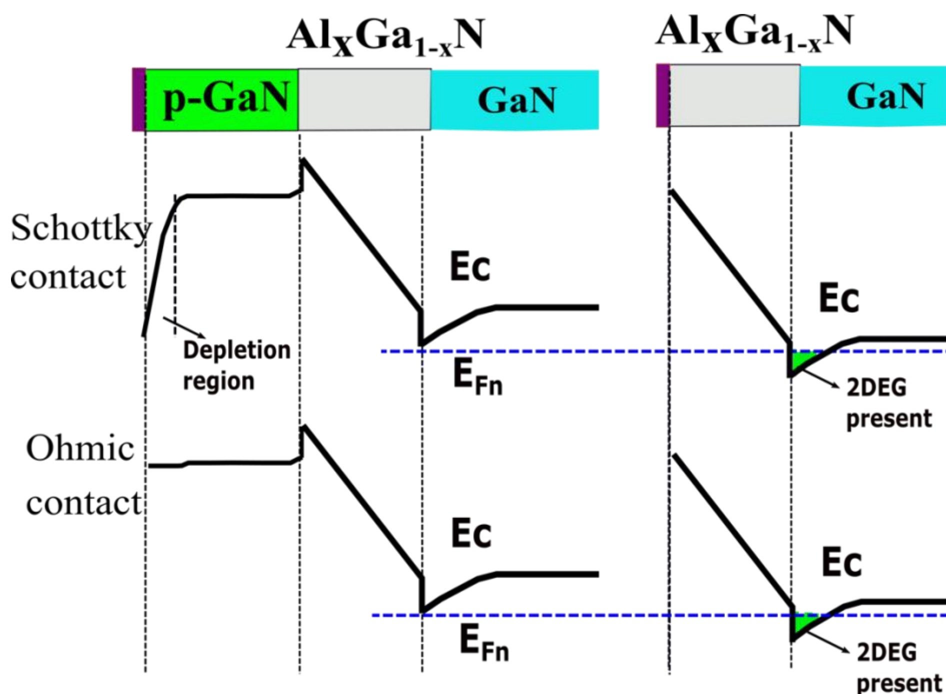



*Figure 4.4: Illustrative band diagram showing the effect of p-GaN cap layer causing normally off channel. without p-GaN cap layer (left) with p-GaN cap layer (right)*

### 4.2 Physical understanding of Threshold voltage

With this built in charge dynamics across the gate stack, to physically understand the threshold voltage analytical models in literature [81][82][83] are reviewed and the control parameters for the threshold voltage is presented based on the analysis. To begin with, gauss law in the metal/p-GaN, p-GaN/ AlGaN and AlGaN/GaN interfaces with boundary conditions, the electric field and the electrostatic potential is evaluated. The electrostatic potential when the electron quasi-Fermi energy level coincides with the

conduction band edge EC at the AlGaN/GaN interface is nominally defined as the threshold voltage. An additional back barrier charge of $-\sigma_4$ is included to make the analysis comprehensive. The derivation of the expression for the threshold voltage as adopted from [81]. The parameters used in the below equations could be better understood with the help of *Figure* 4.5

$$V_{TH} = \Phi_{\mathrm{bn}} + \psi_{bi} + V_R + \psi_{si} - (\Delta E_{c2} - \Delta E_{c1})/q - \Delta V_b \qquad 4.4$$

Where $\Phi_{\mathrm{bn}}$ is the Schottky barrier height of the metal toward the conduction band, $\psi_{bi}$ is the built in potential of the Schottky contact, $V_R$ is the reverse bias of the Schottky contact, $\psi_{si}$ is the surface potential of the p-GaN/AlGaN barrier and $\Delta V_b$ is the voltage drop across the barrier. Abstractly the threshold voltage has 2 main segments a) voltage dropped across the Schottky metal barrier b) voltage dropped across the AlGaN barrier. Solving Poisson equation in the barrier gives the expression for the voltage across the barrier

$$\Delta V_b = \frac{1}{C_b}\left(\sigma_{p1} - \sigma_{p2} + \sigma_e + \sigma_4\right) + \frac{\sigma_b}{2C_b} \qquad 4.5$$

Where $\sigma_e$ is the sheet charge density of the 2-DEG electrons, $C_b$ is the back barrier capacitance. A back barrier with a fermi energy level is $EF_{bb}$ and an activation energy Ea2 causing a back barrier polarisation charge -$\sigma_4$ is assumed. Substituting equation 4.5 in equation 4.4 give equation 4.6

$$V_{TH} = \frac{E_{gp} + \Delta E_{c1} - \Delta E_{c2}}{q} + \frac{\sigma_b}{2C_b} + \frac{C_{Ch}}{C_b}\frac{(E_g - E_{a2})}{q} - \frac{1}{C_b}(\sigma_{p2} - \sigma_{p1}) \qquad 4.6$$

In the first term, $E_{gp}$ is the bandgap of the p-type gate region, $\Delta E_{c1}$and $\Delta E_{c2}$ are the conduction band offsets at the p-region/barrier and barrier/channel regions respectively. The second term is dependent only on the properties of the barrier region, with $C_b$ being its capacitance and $\sigma_b$ being the ionized acceptors per unit area, associated with the out-diffusion of the p-dopant. The third term contains the dependence from the back barrier, with $C_{Ch}$ being the capacitance of the channel, sandwiched between the barrier and the back barrier, $E_g$ being the bandgap of the GaN channel and $E_{a2}$ the trap energy-pinning level of the back-barrier. In the last term $\sigma_{p2}$ is the piezoelectric polarization charges per unit area of the barrier and $\sigma_{p1}$ is the spontaneous polarization charges per unit area in GaN.

Thus, the threshold voltage depends on the conduction band discontinuity signifying the importance of the Al mole fraction. The above threshold voltage expression does not have a direct dependence on the p doping in the pGaN region. This is a consequence of the assumption that there is a neutral region in the p-GaN between equilibrium and the threshold voltage. As long as there is a neutral region in the p-GaN gate, it does not matter how high the Mg doping density exactly is, because the quasi-Fermi level of the holes will be pinned close to the Mg activation level in the neutral region and close to the valence band edge at the p-GaN/barrier interface. However, p-GaN doping had an indirect influence as it controls the depletion region near the gate contact and extent of out diffusion in AlGaN barrier which alters the gate charge neutrality by affecting $-\sigma_b$ and $-\sigma_s$ as in Figure *4.3 (2)*

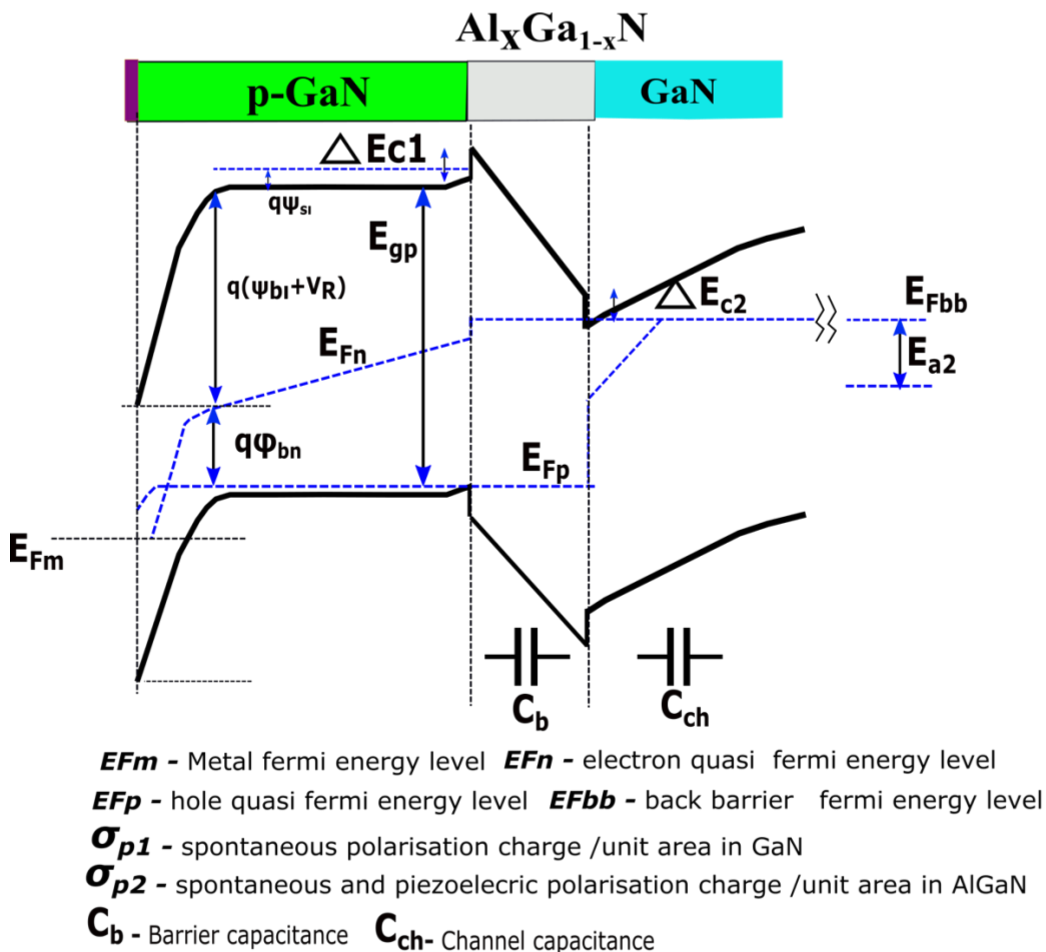



*Figure 4.5: Illustrative band diagram of the p-GaN/AlGaN/GaN gate stack highlighting the parameters that affect the threshold voltage as detailed in the threshold voltage expression*

Thus the p-GaN/AlGaN/GaN gate stack could be modelled as an equivalent circuit having a Schottky diode in series with PIN diode as in *Figure* 4.6. The metal semiconductor contact is modelled as the Schottky diode and the AlGaN barrier is modelled as the PIN diode. The metal semiconductor contact could be Ohmic or Schottky depending upon the manufacturer. At normal conditions the device is OFF. When the device is forward biased the fraction of the applied potential drops across a) Schottky barrier ($V_{Schottky}$) b) across PIN diode ($V_{AlGaN}$), beyond which the applied potential causes the change in the electrostatic conditions, causing conduction band to be pulled down relative to the electron quasi fermi energy level of GaN. 2-DEG density is formed when the conduction band minimum of GaN touches the quasi-fermi energy level, and its density increases with increasing forward bias. With increasing positive bias, the energy of the electrons at the AlGaN/GaN interface increases so that the conduction band moves closer to electron Fermi level forming the 2-DEG.

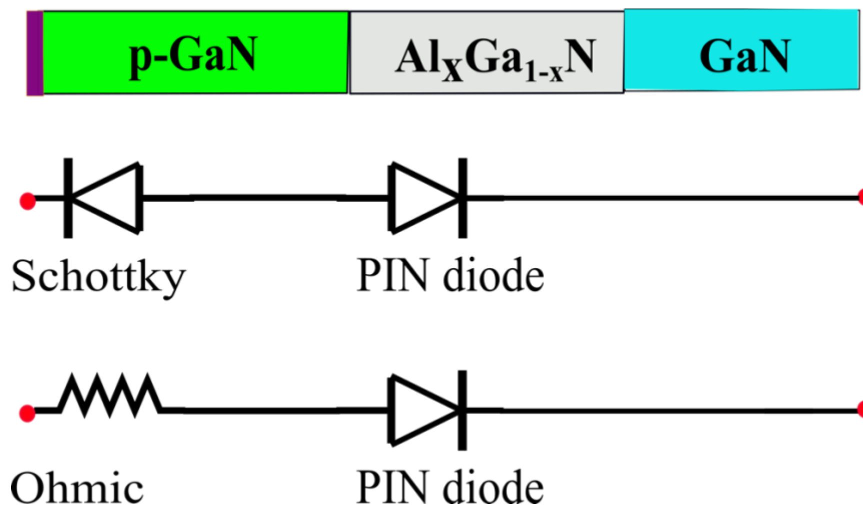



*Figure 4.6: Equivalent circuit of the p-GaN/AlGaN/GaN gate stack with Schottky gate and ohmic gate*

When a positive bias is applied to the p-GaN gate, the metal Schottky junction is reverse biased and causes a potential drop across the Schottky barrier ($V_{Schottky}$). In addition

a) It causes the depletion region to expand leading to increased Mg activation in the depletion region [79]
b) It causes the injection of holes into the p GaN region across Schottky barrier by thermionic emission or by tunnelling. The gate leakage current could be a good indication of this hole injection which is often negligibly small for gate bias <3V.

The gate leakage current at positive gate bias can be due to the leakage at Schottky barrier and PIN diode. If the Schottky barrier is leaky it translates to higher 2-DHG henceforth higher 2-DEG. However, a leaky PIN diode would cause lower 2-DHG henceforth lower 2-DEG. Thus, gate leakage current by controlling the 2-DHG has an effective control on 2-DEG[84]. The above effects alter the gate charge balance and thus increase or decrease the threshold voltage. In the case of the ohmic contact high hole injection across the gate terminal happens and adds to the 2-DHG creating electrostatic conditions which require lower threshold voltage to turn on the device.

In summary $V_{TH}$ of a normally off p-GaN HEMT as measured depends on

- Work function difference between the gate metal and the p-GaN cap layer, which in turn controls the leakage across the gate and the net voltage drop across the gate/p-GaN potential barrier
- AlGaN barrier's Al mole fraction and thickness, which in turn controls the voltage drop across the barrier and the leakage across the barrier.
- P-GaN's Mg doping, which controls the active hole concentration in p-GaN, extent of depletion region boundary in p-GaN, extent of out diffusion in the AlGaN barrier and thus the concentration of ionized negatively charged Mg ion in p-GaN & out diffused regions.
- Extent of 2-DEG electron trapping caused by the measurement condition and methodology.

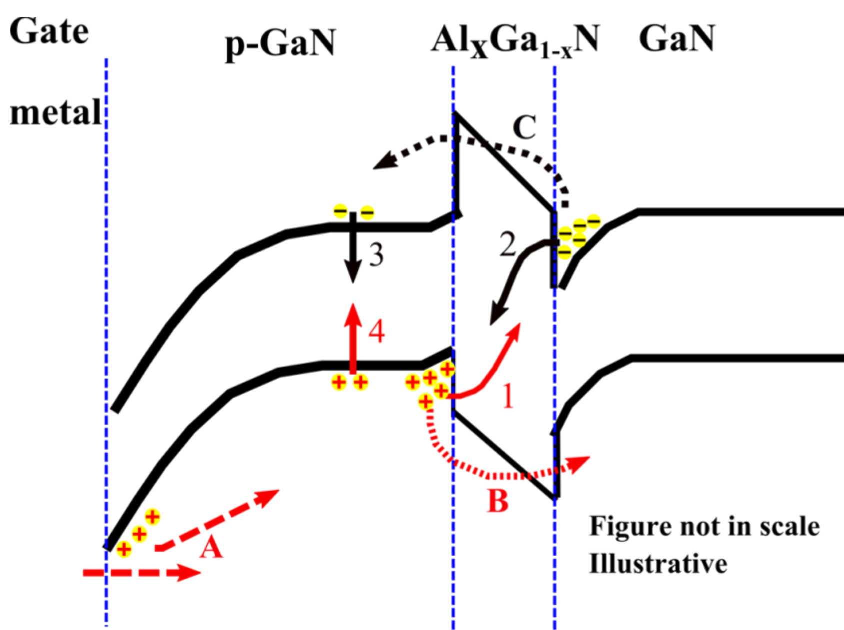
In the case of Normally off p GaN gate HEMTs 2-DHG and 2-DEG could be considered as surface charges and hence the electric field associated with these charges are associated only at the interface as evident from the band diagram. The presence of polarization charges at hetero interfaces/surface, partial ionization of deep level Mg acceptors in p-GaN cap layer and out diffusion of acceptors into the AlGaN barrier layer make the estimation of $V_{TH}$ complex compared to conventional normally ON AlGaN/GaN devices.

### 4.3 Significance of the trapping effects on gate stack charge balance

Reliability issues such as $V_{TH}$ instability in the GaN HEMTs are often associated with trapping. Such trapping processes in the gate stack cause dynamic charge conditions,

which alter the channel density and hence the ON/OFF state characteristics. Figure 4.7 represents such trapping mechanisms which could happen under various gate bias conditions. When the gate stack is positively biased a vertical electric field pull is established across the gate stack which can cause

*a)* Trapping of the 2-DEG electrons in the AlGaN barrier by tunnelling through the barrier (process 2 in Fig.4.7)
b) Thermionic emission of 2-DEG electrons across the AlGaN barrier into the p-GaN region (process C in Fig.4.7)
c) Hole injection from the gate contact which can accumulate at the p-GaN adding to the 2-DHG density (process A in Fig.4.7) causing increased 2-DEG.
d) Accumulated holes in 2-DHG to cross the barrier counter compensating the 2-DEG density (process B in Fig.4.7)




**A (Hole accumulation in p-GaN) --> -ve 'Vt'shift**
**4,B,1 (Hole depletion in p-GaN) --> +ve 'Vt'shift**
**2,1 (Electron depletion in 2DEG) --> +ve 'Vt'shift**
**1,2 - Trapping in AlGaN 3,4 - Trapping in p-GaN**
**A - Hole injection by tunneling/thermionic depending on barrier**
**B,C - At high gate biases (when Vgs>4V)**

*Figure 4.7: Illustrative band diagram of the p-GaN/AlGaN/GaN gate stack depicting the various potential trapping processes that could happen*

The number of holes that can be injected vary depends upon the nature of the gate contact. In the case of Schottky gate contact the leakage is negligibly small till 3-4V, whereas in the ohmic contact the hole injection levels can be higher. These trapping processes are shown for generic understanding, and the location of these traps can be in the bulk of AlGaN barrier or p-GaN/AlGaN interface or AlGaN/GaN interface. Trapped electrons and the holes can recombine by standard Shockley Read Hall processes represented by 3 and 4; 1 & 2 respectively. The potential at the drain terminal ($V_{DS}$) on the other hand establishes the lateral electric field with reference to the channel and with increasing bias can cause high electric field effects at the buffer and gate edge towards the drain side (discussed in detail in chapter 6).

The significance of all the above discussed trapping processes arises from the charging state of these traps post occupation event. These traps depending upon being an acceptor trap or donor trap have varied charging status post an occupation event, the data base of identified traps in GaN material system is detailed in chapter 2.7. The charging state with respect to its carrier occupation for different traps has been detailed in chapter 33.2. For instance, when an acceptor trap in the AlGaN barrier (initially empty) traps a 2-DEG electron it leads to the addition of a net negative charge. This negative charge alters the electric field conditions in the barrier and equivalently cause the conduction energy bands to be pulled up relative to the (electron quasi) fermi energy causing a reduction in the 2-DEG concentration. This drop in 2-DEG density can lead to a reduced channel current ($I_{DS}$) which manifests to an increased $R_{DSON}$ or more voltage requiring to turn on the channel equivalently interpreted as positive threshold voltage shift. In a similar way a donor like trap (D.T.) in AlGaN barrier after donating an electron leads to the addition of a net positive charge, causing a negative threshold voltage shift. In this way trapping mechanisms can cause threshold voltage instability discussed in detail in Chapter 5 and Chapter 6.

### 4.4 $V_{TH}$ targeting and TCAD model

To study and validate the physical mechanisms influencing the threshold voltage, a TCAD model is built and used for analysis in the subsequent chapters (5,6). The normally off p-GaN HEMT gate stack model is further calibrated to match the threshold voltage and gate leakage current of the devices investigated. The principal control

parameters which have been changed are the background doping of the p-GaN, AlGaN, GaN buffer, metal work function, thickness of p-GaN, AlGaN, GaN buffer and the hole tunnelling mass (for gate leakage calibration).

The gate metal work function and the background acceptor doping of p-GaN controls the depletion region width in p-GaN. Gate metal induced depletion width in p-GaN has significant influence on the gate leakage current and the threshold voltage as understood from the *Eqn.*4.4. A work function of 4.65eV, a p type doping of 2E19 $\#cm^{-3}$ and a hole tunnelling mass 0.22 is used to model the Schottky gate metal /p-GaN. An acceptor doping of 2E19 $\#cm^{-3}$ at 170 meV (Mg doping levels) from the valence band edge is used to model the out diffused Mg in the AlGaN/GaN region. A gaussian distribution of the acceptor traps below the gate region using TCAD physical model interfaces in the AlGaN/GaN unintentionally doped (UID) region is made as illustrated in *Figure* 4.8 (a green line below the gate region). The thickness of p-GaN often needs to be such that, there exists a quasi-neutral region to avoid punch through. A 80 nm thick p-GaN layer is used. P type background doping of 3.5 E16 # $cm^{3-}$ is used in the AlGaN and GaN buffer layer to simulate the carbon doping.

GaN buffer has a 50 to 60 nm of unintentionally doped (UID) layer at the AlGaN interface near the channel region. When the unintentional background p type carbon doping of the GaN buffer is higher, the depletion region in the GaN UID layer at the AlGaN interface is smaller and thus will contribute less immobile negative charges causing the 2-DEG density to be larger in the AlGaN/GaN interface. This correlates to the channel capacitance parameter in *Eqn.* 4.6. The mobility and the doping of this UID layer can be suitably changed to match the experimental characteristics. The Al mole fraction and the AlGaN barrier thickness significantly changes the 2-DEG density and higher Al content increases the 2-DEG density.

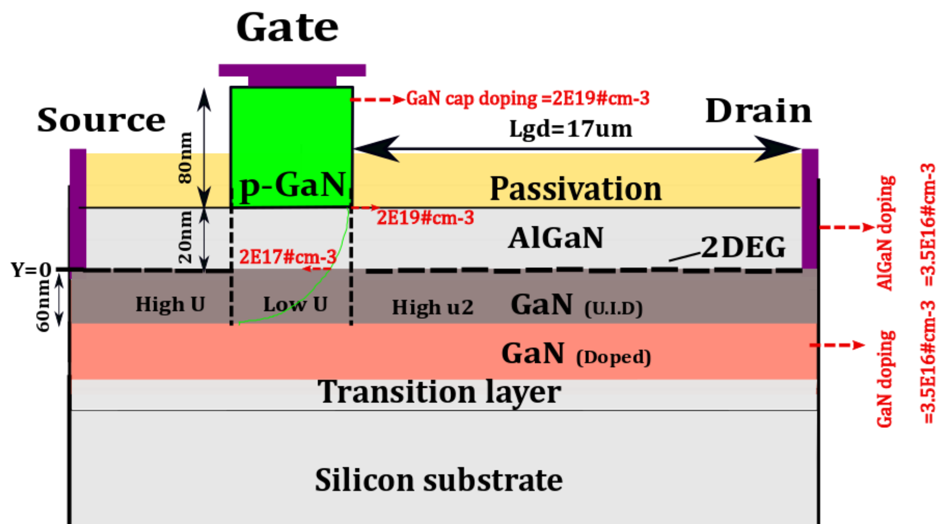



*Figure 4.8: TCAD model structure of the normally off p-GaN gate HEMT, depicting the various layers thickness and doping*

An Aluminium mole fraction of 0.19 and thickness of 20 nm is used for the AlGaN barrier layer in the model. The TCAD model of the normally off p-GaN/AlGaN/GaN HEMT built is used in the chapter 5 and 6 with customised changes as mentioned in the respective chapters.

### 4.5 Conclusion

- The gate control of the 2-DEG channel of electrons is strongly dependent on the charge dynamics across the gate stack at the metal/p-GaN interface, p-GaN/AlGaN interface, AlGaN/GaN buffer interface and the back barrier charges.
- The gate stack p-GaN/AlGaN/GaN could be modelled as a Schottky diode in series with the PIN diode where metal/p-GaN represents the Schottky diode and the AlGaN barrier represents the equivalent PIN diode. The electrostatic potential when the Fermi level at the AlGaN/GaN interface coincides with the conduction band edge $E_C$ is defined as the threshold voltage.
- Threshold voltage depends on the potential drop across the metal gate induced Schottky barrier, potential drop across the AlGaN barrier and the potential required to pull down the AlGaN/GaN conduction band minimum below the quasi-electron fermi energy level. The potential drop across the barrier is the key control metric which encompasses the various parameters such as the conduction band discontinuity, Al mole fraction and Al thickness. The potential required to pull the band is predominantly dependent on both AlGaN and p-GaN parameter

# 5. Measurement induced threshold instability and challenges of reliable threshold voltage measurement

*This chapter describes the challenges of the threshold voltage measurement in the normally off p-GaN HEMTs. The measurement procedure by itself induces an instability in the threshold voltage making the measurement of threshold voltage challenging. This measurement induced threshold voltage instability for two different measurement methodologies a) Pulsed transfer characteristic measurement b) DC step transfer characteristic measurement is investigated and a methodology to mitigate this effect has been proposed. It is further observed that Schottky gate has a more pronounced measurement induced threshold instability relative to an ohmic gate which has a stable threshold voltage throughout measurement. A detailed TCAD analysis validating the proposed physical mechanisms and the effect of ohmic and Schottky contact are also demonstrated in this chapter*

## 5.1 Introduction

For large scale testability of p-GaN HEMTs it is essential to investigate threshold voltage ($V_{TH}$) instability from the perspective of the measurement induced instability. While the stress induced $V_{TH}$ instability has been studied in the literature, the impact of the gate bias occurring during $V_{TH}$ measurement on $V_{TH}$ itself has not been investigated as extensively [85]. In this study, we disaggregate the key $I_D$-$V_G$ measurement parameters that have an impact on $V_{TH}$ estimation and thereby promote better understanding of measurement induced $V_{TH}$ instabilities. This work provides an insight into the underlying dynamic effects occurring during the gate bias and is based on extensive measurements of commercially available p-GaN HEMTs and TCAD modelling. It is important to note that in mass manufacturing, during wafer acceptance test (WAT) procedures, it is a common practice to vary measurement time and measurement voltage ranges (e.g., $0.5V_{TH}$ to $1.5V_{TH}$) to adjust throughput. However, in this paper we show that variations in the measurement time and the gate bias history induce a significant change in the reading of the $V_{TH}$ value. We illustrate further that the characteristics of this effect can vary significantly depending on the gate-stack technology used by different manufacturers.

## 5.2 Experimental methods

650V, 200mΩ, p-GaN gate AlGaN/GaN-on-Si normally off HEMTs (see *Figure* 5.1) with a Schottky gate contact (Type A) and nominal $V_{TH}$ = 1.3V are primarily used in this study. Type A HEMT comprises 60-80 nm thick Mg doped p-GaN layer, 15-25 nm AlGaN layer and ~ 5um GaN epi layer grown on a Silicon substrate with an intermediate transition layer. Type A HEMT is based on 650V TSMC technology [86]. A second set of p-GaN gate AlGaN/GaN-on-Si normally off HEMTs with an ohmic gate contact (Type B) are used in some experiments for comparison. Type B HEMTs are commercially available devices from Infineon [87]. The normalized gate leakage current (at $V_G$ = 3V, $V_{DS}$ = 50mV) of Type B HEMTs is 2 to 3 orders of magnitude higher, compared to Type A HEMTs. This is expected as the gate contact is ohmic rather than Schottky [88].

In one experiment, the Type A HEMT is subjected to a gate bias ($V_G$ bias) of 1.5V and drain bias ($V_D$ bias) of 50mV for 180 minutes and the corresponding drain current ($I_D$) is sampled at varied time intervals as illustrated in *Figure* 5.2 utilizing Keysight precision SMUs. The choice of $V_G$ bias is such that it is ~10% greater than the nominal $V_{TH}$. At this bias level the channel starts to turn-on and the effects of low-level gate bias on $I_D$, and therefore the channel 2-DEG concentration, can be observed.

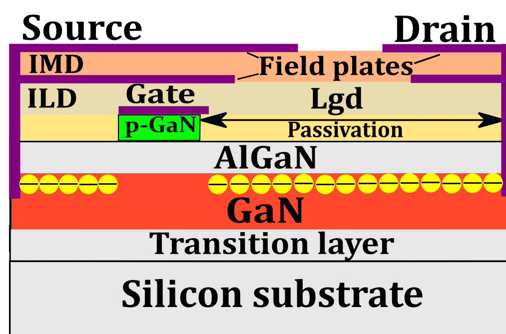



*Figure 5.1*

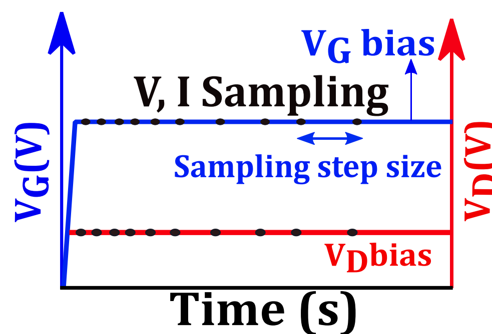



*Figure 5.2*

*Figure 5.1: Standard normally off p GaN gate AlGaN/GaN HEMT structure*

*Figure 5.2: Illustration of drain current sampling at fixed gate bias ($V_G$ bias)*

Based on these measurements we can begin to understand the effect of equivalent accumulated gate bias during transfer characteristic sweep ($I_D$-$V_G$) up to the $V_{TH}$ value. The sampled $I_D$ over time as plotted in *Figure 5.3 (Till 4s), Figure 5.4 (Till 180mins)* shows

a significant $I_D$ decay trend exemplifying the possible impact of low voltage gate bias history on $I_D$ measured during $I_D$-$V_G$.

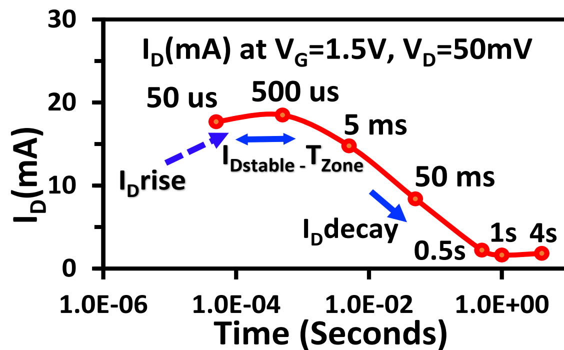



Figure 5.3

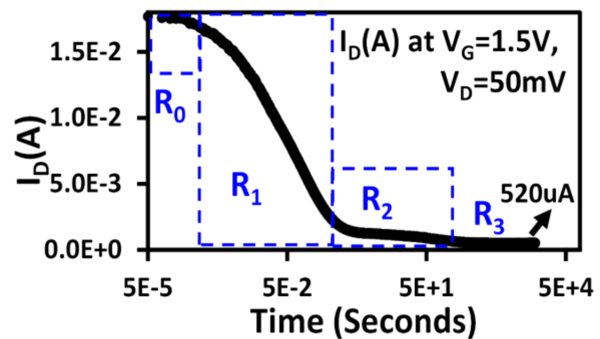



Figure 5.4

*Figure 5.3: $I_D$ sampling at $V_G$ bias 1.5V show $I_D$ stable-Tzone (100-500us), Type A HEMT*

*Figure 5.4: $I_D$ sampling at $V_G$ bias 1.5V showing varied slopes of $I_D$ in Type A HEMT*

For p-GaN HEMTs $V_{TH}$ is commonly estimated by a constant current technique (10uA/mm) using pulsed $I_D$-$V_G$ (*Figure* 5.5) or DC step $I_D$-$V_G$ (*Figure* 5.6) measurement. Pulse on-time (Ton) and DC step size (Tstep) are the key parameters that affect the gate bias history developed during pulsed and DC step transfer characteristic measurements respectively. The impact of Ton, Tstep on $I_D$, and thereby $V_{TH}$ is illustrated by measuring $V_{TH}$ for various Ton, Tstep values ranging from 100μs to 50ms. The measurement delay time (Tmede) is fixed at Ton/2 for pulsed and Tstep/2 for DC step measurements

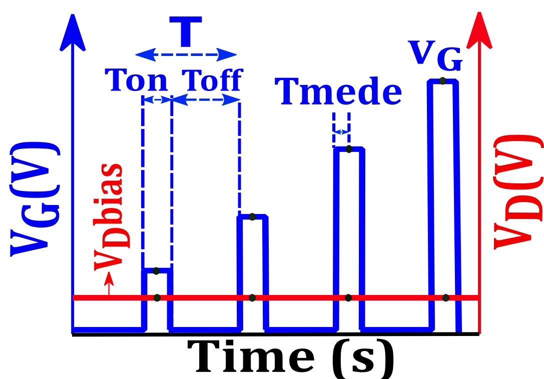



Figure 5.5

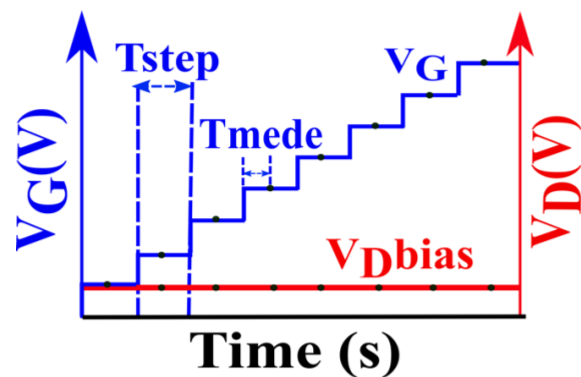



Figure 5.6

*Figure 5.5: Illustration of pulsed $I_D$-$V_G$ transfer characteristic measurement*

*Figure 5.6: Illustration of DC step $I_D$-$V_G$ transfer characteristic measurement*

respectively. In both pulsed and DC step measurements a sweep range of 0 to 3V with 3mV step is used. The effect of Ton, Tstep on $V_{TH}$ extracted using constant current technique from pulsed and DC step $I_D$-$V_G$ measurements in Type A and Type B HEMTs are plotted in *Figure* 5.7, *Figure* 5.8, *Figure* 5.9 and *Figure* 5.10 respectively. Finally, DC step $I_D$-$V_G$ hysteresis and loop measurements (5x consecutive $I_D$-$V_G$ sweep) are performed in both samples (*Figure* 5.11, *Figure* 5.12, *Figure* 5.13, *Figure* 5.14). Sweep ranges are limited to 3V in the hysteresis and loop measurements to remove the effect of high gate voltage stress which is not the focus of this study.

## 5.3 Quantifying effect of $V_{TH}$ measurement on $V_{TH}$

The drain current ($I_D$) sampling over time ( *Figure 5.3 , 5.4* ) at $V_G$ bias of 1.5V and $V_D$ bias of 50mV for Type A HEMT reveals a) an initial rise period where $I_D$ marginally rises b) a stabilization period (100-500us) ($I_{D\ stable}$-$T_{zone}$) where $I_D$ stabilizes at 18 mA and c) a fall period where $I_D$ significantly decays to 520uA (- 97%) at 180 minutes. The initial rise period observed is attributed to the gate voltage bias rise time, limitations of the measurement equipment. The significant decay observed in $I_D$ is analysed in more detail in *chapter 5.6*.

In the pulsed $I_D$-$V_G$ measurements when Tmede < $I_{D\ stable}$-$T_{zone}$ (<100us) or Tmede> $I_{Dstable}$-$T_{zone}$ (>500us) the $I_D$ measured at each $V_G$ bias point during $I_D$-$V_G$ sweep, corresponds to the rise or fall period. During these periods $I_D$ values are smaller leading to higher (5-20%) extracted $V_{TH}$ values as illustrated in *Figure* 5.7. When Tmede is within $I_{D\ stable}$-$T_{zone}$ (= 100us, 250µs & 500us) the $I_D$ measured is within the stabilization period where $I_D$ values are relatively larger leading to a lower measured $V_{TH}$ explaining the trend observed in *Figure* 5.7. Similar behaviour is observed for DC step $I_D$-$V_G$ measurements. However, in DC step measurements there is no Toff period and hence the bias stress is more cumulative, making it harder to interpret especially when Tmede < $I_{D\ stable}$-$T_{zone}$. In DC step $I_D$-$V_G$ measurements when Tmede > $I_{D\ stable}$-$T_{zone}$ (> 500us), $V_{TH}$ extracted is higher (5-15%) than values extracted when Tmede is within $I_{D\ stable}$-$T_{zone}$ as observed in *Figure* 5.8. As these results illustrate, $V_{TH}$ is a hard parameter to define in Schottky p-GaN HEMTs. As such, and similar to the Dynamic Ron effect [89], Dynamic $V_{TH}$ is becoming the subject of investigation in application conditions [90] where any

adverse effects (e.g. false turn on, increased reverse conduction losses) caused by the instability of the Schottky p-GaN gate are of great interest.

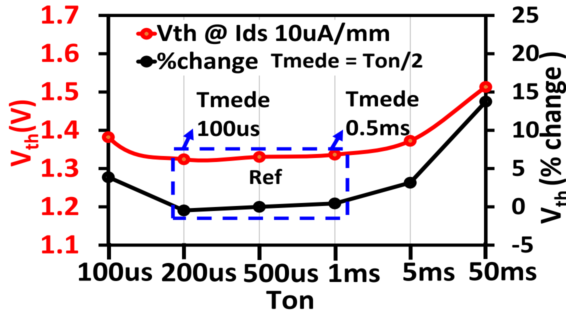
In summary, to measure $V_{TH}$ of p-GaN gate HEMTs with a Schottky contact (Type A) reliably, the following procedure was followed:

• Identify $I_{Dstable}$ -$T_{zone}$ by biasing gate ($V_G$ bias) at a voltage 10% greater than expected $V_{TH}$ and by sampling $I_D$ over time (0-5s). The $I_D$ transients and thus $I_{Dstable}$-$T_{zone}$ can vary depending on the gate stack composition and processes.

• Choose Ton (Tmede) in pulsed $I_D$-$V_G$ measurements within $I_{Dstable}$-$T_{zone}$ or Tstep (Tmede) in DC step $I_D$-$V_G$ measurements less than or within $I_{Dstable}$-$T_{zone}$. A recommended simplified methodology to measure the $V_{TH}$ of p-GaN Schottky gate HEMTs (given the duty cycle and pulser limitations) would be to use DC step $I_D$-$V_G$ measurements and sweep the gate bias as fast as possible. That means Tstep selected should be as short as the measurement equipment permits. This simplified approach will extract the lowest possible nominal $V_{TH}$ which is a parameter of great interest when designing to avoid the possibility of false turn-on due to oscillations in the gate loop.

## 5.4 Comparison of Ohmic and Schottky gate devices

The choice of Schottky or Ohmic gate contact depends upon the manufacturer and application scenarios, thus it is quintessential to study this dynamic effect on both the contacts. Type B (Ohmic gate) HEMTs when subjected to $V_G$ stress bias of 1.5V and $V_D$ bias of 50mV for 180 minutes have a constant $I_D$, unlike Type A HEMTs. It is also observed that variations of Ton, Tstep in pulsed $I_D$-$V_G$ measurements and DC step $I_D$-$V_G$ measurements have negligible to no effect on $V_{TH}$ as illustrated in *Figure* 5.9, *Figure* 5.10. This absence of threshold voltage instability in ohmic gate HEMTs is expected as there is no time dependent $I_D$ variation with constant gate bias. This suggests that the ohmic gate contact is preferable from the perspective of $I_D$-$V_G$ measurement induced $V_{TH}$ stability. Nonetheless, a considerable proportion of commercially available normally off p-GaN HEMTs have Schottky gate contacts to minimize gate leakage and minimize the current through the driver circuit.



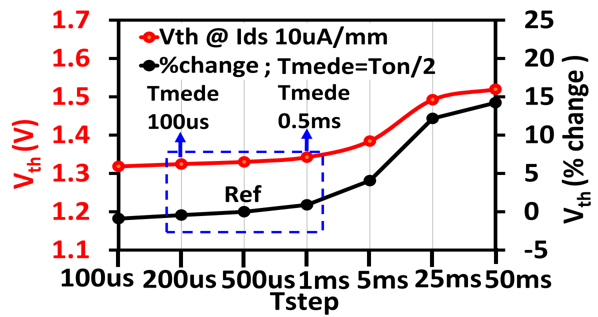
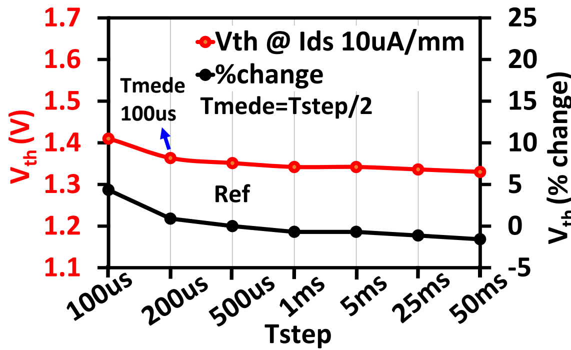




*Figure 5.7*

*Figure 5.8*

*Figure 5.7: Impact of Ton on $V_{TH}$ measured from pulsed $I_D$-$V_G$ in Type A HEMT*

*Figure 5.8: Impact of Tstep on $V_{TH}$ measured by DC step $I_D$-$V_G$ in Type A HEMT*



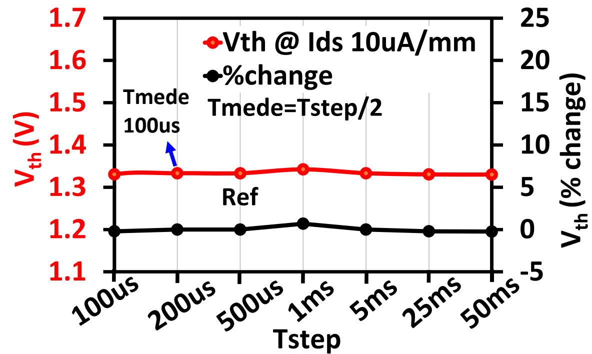




*Figure 5.9*

*Figure 5.10*

*Figure 5.9: Impact of Ton on $V_{TH}$ measured by pulsed $I_D$-$V_G$, Type B HEMT*

*Figure 5.10: Impact of Tstep on $V_{TH}$ measured by DC step $I_D$-$V_G$, Type B HEMT*

## 5.5 Effect of hysteresis and loop test on threshold voltage

To better understand the underlying trapping/detrapping mechanisms occurring in the gate stack, hysteresis measurements having a consecutive forward and reverse $I_D$-$V_G$ sweep (0 to 3V & 3 to 0V) and loop tests having 5 consecutive $I_D$-$V_G$ sweeps (5x 0 to 3V) are used. From hysteresis measurements it is observed that Vth of Type A HEMTs in forward sweep is smaller than in the reverse sweep (*Figure* 5.11) implying a gate bias induced positive (+ve) $V_{TH}$ shift. In Type B HEMTs, the $V_{TH}$ in the forward sweep is larger than in the reverse sweep (*Figure* 5.12) implying a negative (-ve) $V_{TH}$ shift.

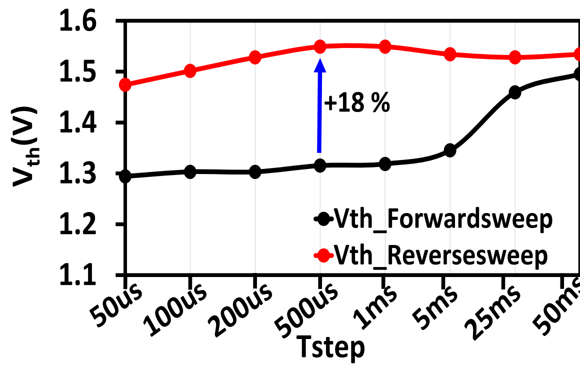



Figure 5.11

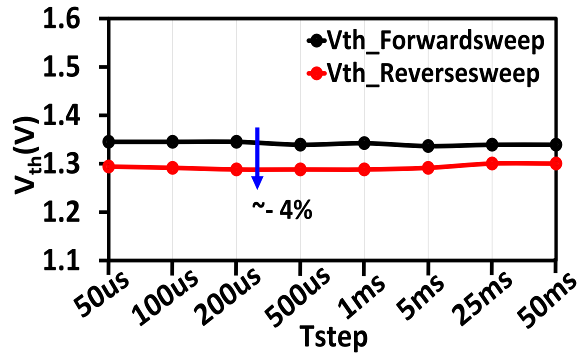



Figure 5.12

*Figure 5.11: Effect of hysteresis alongside Tstep on $V_{TH}$ extracted by DC step $I_D$ -$V_G$ measurements on Type A HEMT*

*Figure 5.12: Effect of hysteresis alongside Tstep on $V_{TH}$ extracted by DC step $I_D$ -$V_G$ measurements on Type B HEMT*

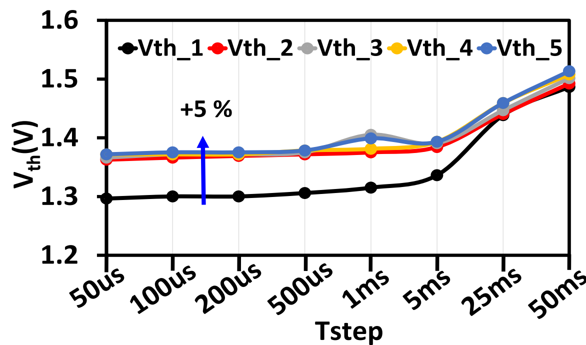



Figure 5.13

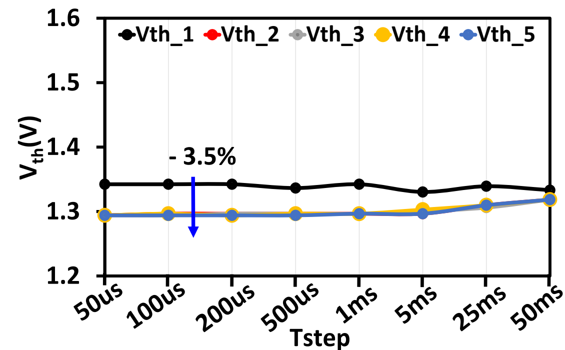



Figure 5.14

*Figure 5.13: Effect of 5x loop tests alongside Tstep on $V_{TH}$ extracted by DC step $I_D$-$V_G$ measurements on Type A HEMT*

*Figure 5.14: Effect of 5x loop tests alongside Tstep on $V_{TH}$ extracted by DC step $I_D$-$V_G$ measurements on Type B HEMT*

18% positive $V_{TH}$ shift is observed in Type A HEMT when Tstep is within $I_{Dstable}$-$T_{zone}$ whereas the relative $V_{TH}$ +ve shift reduces when Tstep > $I_{Dstable}$- $T_{zone}$ as reference Vth during forward sweep itself increases (*Figure* 5.11). When Tstep is within $I_{Dstable}$- $T_{zone}$, during forward sweep, $I_D$ measured corresponds to unstressed phase resulting in a nominal lower $V_{TH}$. However, in the following reverse sweep the gate stack is already stressed by the preceding forward sweep, a condition resulting in a higher $V_{TH}$. In contrast, in Type B HEMTs the small negative $V_{TH}$ shift stays constant at ~-4% irrespective of Tstep, agreeing with earlier observations. Positive and negative $V_{TH}$

shifts, for Type A and B HEMTs respectively, are also observed in the loop tests. $V_{TH}$ stabilizes for the second sweep in both cases as illustrated in *Figure* 5.13, *Figure* 5.14. However, when Tstep > $I_{Dstable-\ Tzone}$ for Type A HEMT the +ve $V_{TH}$ shift observed is relatively smaller, similar to the observation in the hysteresis test.

## 5.6 Physical understanding of instability mechanisms

A schematic band diagram across the gate stack of Type A HEMTs is shown in *Figure* 5.16. The band diagram illustrates the suspected mechanisms leading to the device behaviour presented in this study. *Figure* 5.16 depicts acceptor traps present at the AlGaN/GaN interface [91]. When a low forward voltage bias is applied 2-DEG electrons are trapped in these interface traps causing the significant $I_D$ decay observed during time periods R0, R1 in *Figure 5.4*. The $I_D$ decay rate reduces in time (R2 in *Figure 5.4*) due to

a) an increase in the interface trap occupancy reaching full occupancy levels.

b) an increase in the negative space charge at AlGaN/GaN interface screening the field pull from gate side.

c) a reduction in the overall 2-DEG density with time.

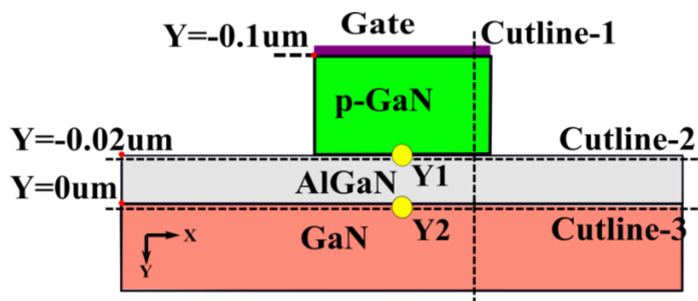



*Figure 5.15: Cross sectional view of the gate stack showing cutlines-1,2,3, p-GaN/AlGaN interface point Y1 and AlGaN/GaN-buffer interface pointY2.*

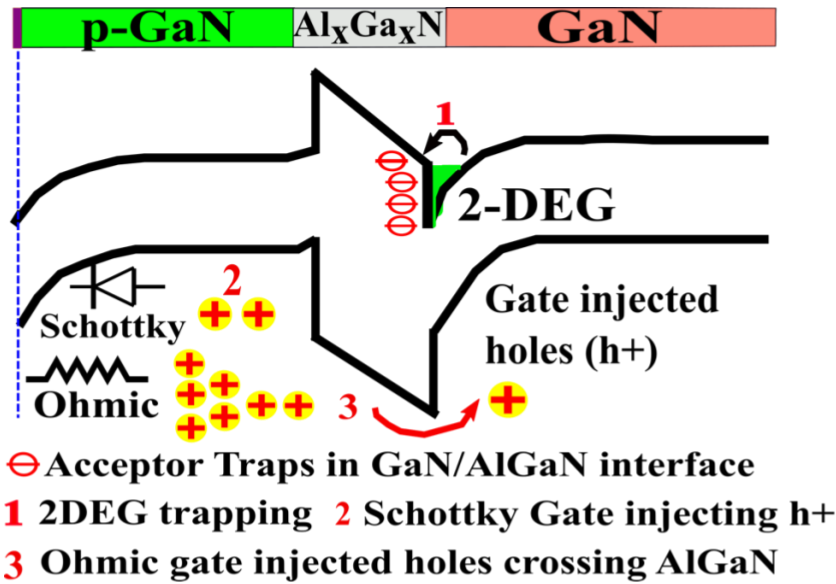


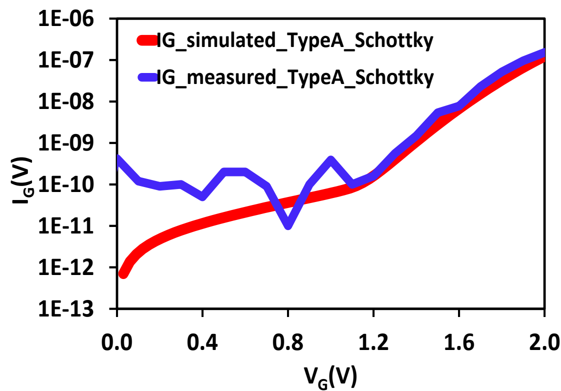

*Figure 5.16: Band diagram along cutline-1 p-GaN/AlGaN/GaN gate stack at $V_G$ bias 1.5/2V showing trapping of 2-DEG electrons in the AlGaN/GaN interface*

In the case of the ohmic gate HEMTs (Type B), under similar gate bias conditions the significant $I_D$ decay is not observed. This may be due to a reduced acceptor trap presence at the AlGaN/GaN interface in Type B devices by a different manufacturer. A second, potentially compounding, effect is that high hole injection from the gate during gate bias over time facilitates hole movement across the AlGaN barrier (*Figure* 5.11) and adds net positive charge in the GaN buffer leading to 2-DEG accumulation causing a negative $V_{TH}$ shift as observed in hysteresis tests and loop tests of type B HEMTs (*Figure* 5.12, *Figure* 5.14).

### 5.7 TCAD modelling and validation

To validate the physical understanding, a Technology Computer Aided Design (TCAD) model of Type A device has been developed. The gate stack of Type A device is modelled as detailed in chapter 4.4. The details of the TCAD model are explained in *chapter 3* and more details about the base TCAD model are given in [92]. In the model, a Schottky gate metal contact with a work function of 4.65 eV and a hole tunnelling mass 0.22 is used. The gate leakage current in the Schottky contact is modelled by creating a non-local mesh enabling electron and hole barrier tunnelling. By varying hole tunnelling mass, the ohmicity of the gate contact is controlled. A thermionic emission model is

defined across the gate stack to model the leakage over both the Schottky barrier and the heterojunction barrier. The simulated gate current is matched with the measured gate current of Type A (Schottky) devices as shown in *Figure* 5.17. To elucidate the change in carrier statistics at p-GaN/AlGaN interface (Y1) and AlGaN/GaN interface (Y2) cutline 2 and cutline 3 are made respectively during further TCAD introspection as shown in *Figure* 5.15



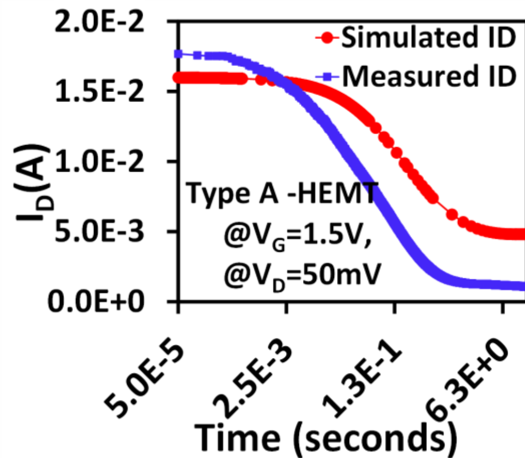
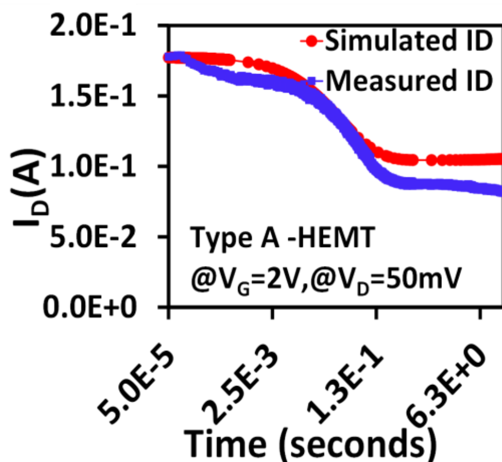




*Figure 5.17* *Figure 5.18*

*Figure 5.17: Simulated/experimental $I_G$-$V_G$ curve of Type A HEMT.*

*Figure 5.18: Simulated/Experimental $I_D$ curve of Type A HEMT at $V_G$ bias of 1.5V*



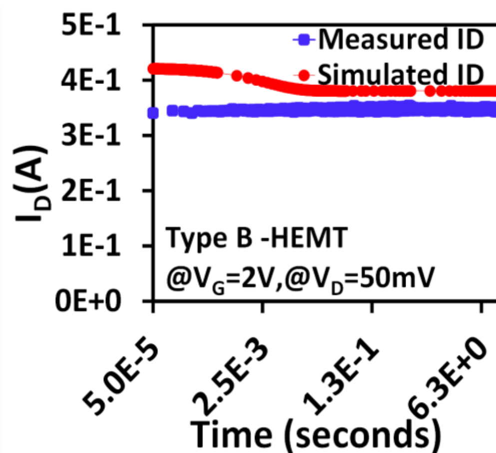




*Figure 5.19* *Figure 5.20*

*Figure 5.19: Simulated/Experimental $I_D$ curve of Type A HEMT at $V_G$ bias of 2V.*

*Figure 5.20: Simulated/Experimental $I_D$ curve of Type B HEMT at $V_G$ bias of 2V.*

It is to be noted that at voltages below 1.1V the measured $I_G$ is dominated by the noise from the measurement. Above 1.2V the simulated $I_G$ (Tmh=0.22) starts to match the

measurement well up to 2V, which is the area of focus in this study. Acceptor traps with a uniform density of $2\times10^{19}$ $cm^{-3}$ and activation energy 170 meV are introduced in the p-GaN region to simulate the Magnesium (Mg) doping. A Gaussian distribution of acceptor traps to simulate the Mg out-diffusion in the AlGaN layer is also introduced [93]. Acceptor traps at AlGaN/GaN interface are uniformly introduced between 0.15 eV to 0.45 eV below the conduction band with a density $3.5\times10^{12}$ $cm^{-3}$ and capture cross section $5\times10^{-20}$ $cm^2$. A transient simulation for a $V_G$ stress bias of 1.5V, 2V for 15 seconds at $V_D$=50mV is performed. It is observed that the simulated curve follows the experimental curve trend, as illustrated in *Figure* 5.18, *Figure* 5.19. The marginal mismatch of the current levels in *Figure* 5.18, *Figure* 5.19, are likely attributed to approximations in the interface trap energy, trap density used in the TCAD simulations.

To better understand the effect of the gate contact on the $V_{TH}$ shift, transient simulations are performed where the Ohmicity of the gate is increased by:

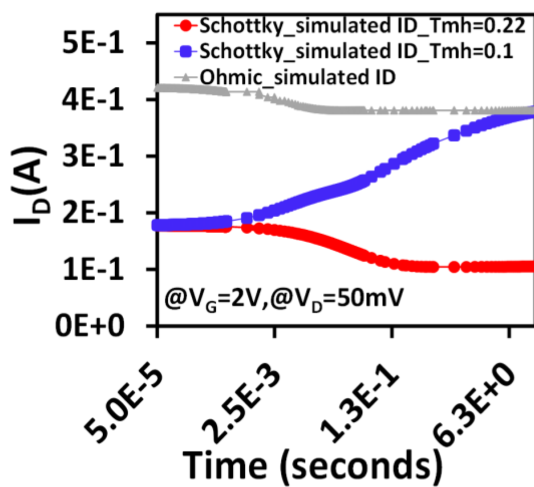
a) changing the gate contact type to ohmic (to relate to the gate contact in Type B devices).

b) reducing the hole tunnelling mass (Tmh) of the Schottky gate (from Tmh=0.22 to Tmh=0.1).

This model represents an interesting case in-between the Schottky (Tmh=0.22) and ohmic gate and leads to better understanding of the different mechanisms at play. Other parameters are kept unchanged. When the gate ohmicity is increased dramatically by changing the contact type to ohmic (similar to Type B device) it is observed that the initial simulated $I_D$ (at $V_G$=2V) is higher compared to the Schottky gate TCAD models (*Figure 5.20*). The comparison between the simulated ohmic gate device and the measured result for Type B device is shown in *Figure 5.20*. In the simulated ohmic case, after an initial mild decay, the $I_D$ reaches a steady value at 2.5ms. The decay observed in simulations is associated with the 2-DEG electron trapping at the AlGaN/GaN interface. The hole gas at the p-GaN/AlGaN interface directly correlates to the 2-DEG density [81] and a portion of the gate injected holes add to this, which explains relative higher $I_D$ levels for ohmic gate (Type B) at same voltage conditions (*Figure 5.21*).

In the TCAD model where tunnelling mass is reduced from Tmh=0.22 to Tmh=0.1, the initial $I_D$ value is identical to the Tmh=0.22 value (and lower than the ohmic gate value).

Nonetheless, the $I_D$ transient simulations at fixed $V_G$ bias for the Tmh=0.1 model no longer reveal an $I_D$ decay as in Figure *5.21*. Rather, $I_D$ starts to increase (after 2.5ms) signifying an increase in 2-DEG density at the channel as seen in *Figure* 5.22. The quantity of holes supplied by the gate contact increases with the ohmicity of the gate, leads to accumulation at the p-GaN/AlGaN interface, and eventually holes crossing the AlGaN barrier. The hole density increases with time, both close to the p-GaN/AlGaN interface (Y1) and AlGaN/GaN interface (Y2), for the Type A device with Tmh=0.1 as illustrated in *Figure* 5.23. In the simulation, we can monitor the edges of the Schottky contact depletion region at different times during the fixed $V_G$ bias by monitoring the space charge in the region. We observe that the edge of the depletion remains almost constant or shows a marginal retraction over time in the case of the Schottky contact with tunnelling mass 0.1, as illustrated in *Figure* 5.24. This suggests that the holes added to the 2-DHG over time do not originate from any charge redistribution in this depletion region but rather come from the gate hole current, as the depletion region width marginally retracts, rather than expand, with time.



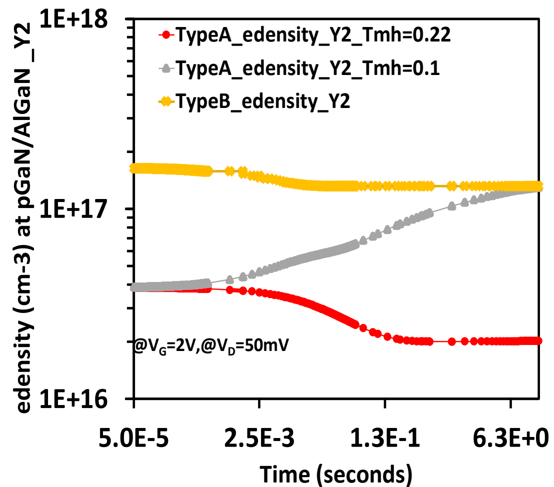




*Figure 5.21* *Figure 5.22*

*Figure 5.21: Simulated $I_D$ curve at $V_G$ bias of 2V of TCAD model with ohmic gate contact (Type B), Schottky gate contact (Type A, Tmh=0.1, 0.22).*

*Figure 5.22: Electron density at AlGaN/GaN interface (Y2) of Schottky gate model (Type A) and ohmic gate model (Type B).*

Accumulation of holes can occur in the p-GaN layer and at the p-GaN/AlGaN interface over time, as the hole current from the Schottky gate terminal and the hole current over the heterojunction barrier are not necessarily matched. This may explain the marginal

retraction in the Schottky contact depletion region. No change in the depletion region boundary was observed in the simulation with tunnelling mass Tmh=0.22. In the case of Tmh=0.1 the $I_D$ over time (> 6s) settles at a higher constant value. This constant value matches the equivalent steady state value of the ohmic gate model $I_D$ (Figure *5.21*). In the case of the ohmic gate, the supply of holes from the gate terminal is relatively high from the start, reaching a steady state value much earlier or instantaneously.

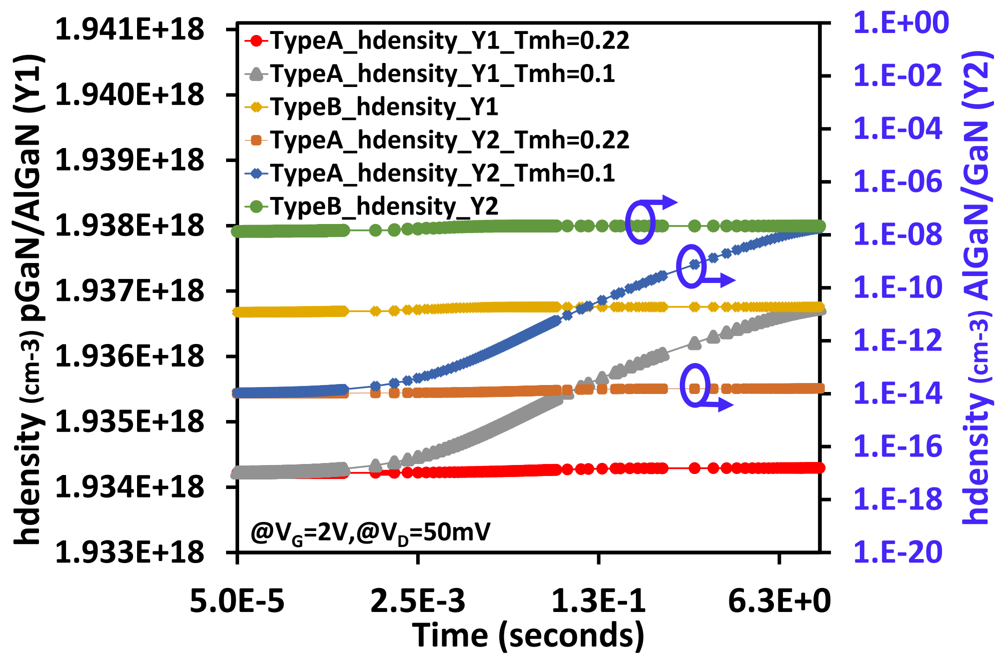



*Figure 5.23 : Hole density at p-GaN/AlGaN interface (Y1), AlGaN/GaN interface (Y2) of Schottky gate model (Type A) and ohmic gate model (Type B).*

These observations imply coordinated, time-matched changes in hole density (at Y1) and electron density at the AlGaN/GaN interface (at Y2) which are strongly controlled by the ohmicity, and therefore hole current supplied, of the gate contact. The TCAD simulations with reduced Tmh=0.1 and ohmic gate support the proposed theory that the ohmic gate contact facilitates higher hole current from the gate terminal, leading to additional holes at the p-GaN/AlGaN interface as well as holes crossing the AlGaN barrier and compensating the 2-DEG acceptor trapping. Furthermore, TCAD simulations also illustrate that the effect of hole current from the gate terminal on the transient $I_D$ (and therefore perceived $V_{TH}$) is faster for a relatively more ohmic contact.

To summarize, three time-dependent mechanisms are identified as crucial components of the $V_{TH}$ instability:

1) 2-DEG electron trapping at the AlGaN/GaN interface traps due to field pull from gate side (*Figure* 5.22).

2) hole current from the gate terminal and accumulation at the p-GaN/AlGaN interface (Y1 axis on *Figure* 5.23).

3) holes crossing the AlGaN barrier, thus changing the charge balance and attracting additional electrons to the 2-DEG. Holes crossing the AlGaN barrier cause a six order of magnitude increase ($1x10^{-14}cm^{-3}$ to $1x10^{-8}cm^{-3}$) in hole density at the AlGaN/GaN interface (Y2 axis of *Figure* 5.23) for the type A device with tunnelling mass Tmh=0.1. The hole density values observed at a gate bias voltage of 2V are not very significant compared to the other charges illustrated.

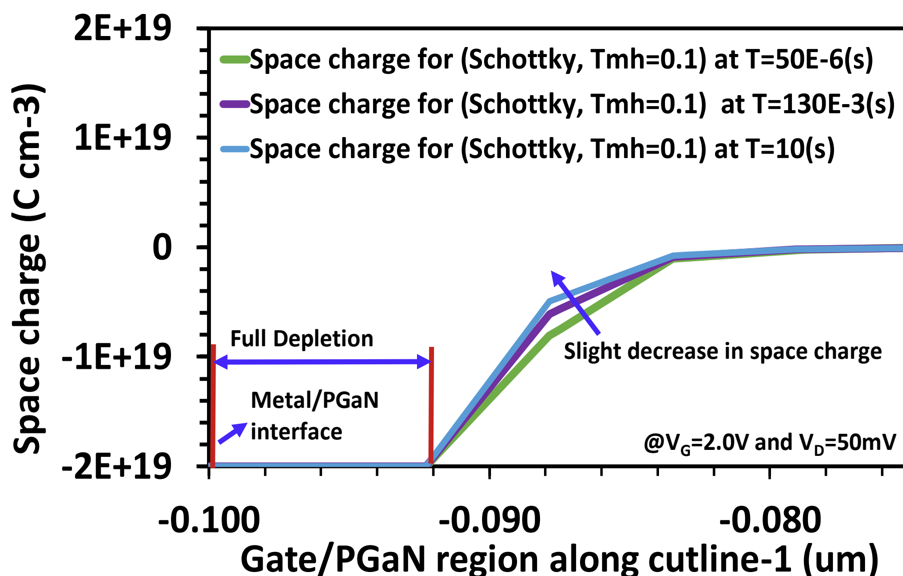



*Figure 5.24: Simulated space charge across the gate/p-GaN region for type A devices (Tmh=0.1) along cutline -1 at $V_G$=2.0V, $V_D$=50mV at various time instances (50us, 130ms and 10s) showing the boundary of the depletion region*

However, as the gate bias increases this hole density will grow exponentially, due to the forward biasing of the heterojunction diode. This hole density may play a significant role in conductivity modulation at higher gate bias values as reported originally in [94]. With sufficient time at a fixed gate bias (t > 6s), the three mechanisms

lead to an equilibrium reaching a constant $I_D$ value. The time-dependent effects listed are more prominent at gate voltage bias close to the threshold voltage where 2 DEG density is lower and the interface acceptor traps are less likely to reach full occupancy. Relating the TCAD findings to the experimental results we can understand the following:

• In a Type A device, a significant $I_D$ decrease in time is observed. This suggests that the effect of trapping at the AlGaN/GaN interface is dominating, and the gate terminal hole current effect is negligible. This of course agrees with the more Schottky gate contact of the Type A device.

• In a Type B device, a constant $I_D$ is observed which is reflected in a fairly stable $V_{TH}$ extraction. A small reduction in extracted $V_{TH}$ is observed compared to a fresh device. The TCAD modelling suggests that the small reduction in extracted $V_{TH}$ may relate to accumulation of holes at the p-GaN/GaN and AlGaN/GaN interface and is related to the magnitude of hole current from the gate terminal. The significant $I_D$ decrease is not observed in Type B samples. This may be due to a reduced acceptor trap density at the AlGaN/GaN interface as they are devices from a different manufacturer with a different gate stack. Additionally, the $I_D$ decrease may be suppressed by the counteracting effect of the increased hole current from the ohmic contact as demonstrated in the simulations.

### 5.8 Conclusion

- In this chapter the impact of accumulated gate bias stress during standard transfer characteristic measurements ($I_D$-$V_G$) in a p-GaN AlGaN/GaN-on-Si normally off HEMT is quantitatively analysed and modelled.
- We have quantified threshold voltage measurement ($I_D$-$V_G$) induced $V_{TH}$ instability and proposed an approach to understand and mitigate it in normally off p-GaN Schottky gate HEMTs.
- Ton in pulsed $I_D$-$V_G$, Tstep in DC step $I_D$-$V_G$ are critical parameters that control the gate bias history and need to be chosen such that the measurement of the drain current, $I_D$, happens within a stable time zone (identified via a demonstrated drain current sampling technique) for obtaining a nominal stable $V_{TH}$.

- We suggest that the threshold voltage instability observed is attributed to electron trapping at the AlGaN/GaN interface.
- Furthermore, we show that the higher hole current from the gate terminal in ohmic gate HEMTs, compared to Schottky gates HEMTs, may counter compensate the electron trapping resulting in negligible or no threshold instability due to the stress of the threshold voltage measurement. These findings are based on extensive experimental results and are supported by TCAD modelling.

# 6. Nominal ON/OFF state stress induced threshold voltage instability

*After an analytical understanding of the threshold voltage and its instability induced by measurement in chapter 4 and 5 respectively, this chapter investigates the instability arising in the threshold voltage due to nominal ON state and OFF - state operations. The $V_{TH}$ instability arising due to the gate voltage stresses (ON state) and the drain voltage stresses (OFF state) are studied by developing novel measurement setup. The physical mechanisms hypothesized are further validated using the TCAD simulations.*

## 6.1 Introduction.

A significant amount of effort has been directed towards understanding the behaviour of the p-gate for achieving normally-off GaN HEMT devices [81][92][95]. Several studies in literature have dealt with the stability of the threshold voltage ($V_{TH}$) of these devices under forward gate bias stress. Different studies attribute the threshold voltage shift observed to the accumulation or depletion of holes in the p-GaN region[88][89] or electron trapping in the AlGaN region [96][97]. The out-diffusion of Mg doping from the p-gate in the AlGaN and GaN layers underneath has been identified as a potential source of the trapping phenomena observed [96][97]. Both positive and negative threshold voltage shifts have been reported depending on the process and design[88][89][96][97]. Alternatively, a large amount of research has been directed at understanding the effects of off-state bias stress on the dynamic on-state resistance of GaN HEMTs. In the early stages of research in GaN HEMTs, trapped charges at the AlGaN/passivation interface were often reported to be the cause of current collapse [98][99]. However, in recent years, with improvements in the passivation of GaN HEMTs the dynamic $R_{ON}$ degradation observed is less commonly attributed to trapped charges on the surface of the device [100]. Dynamic $R_{ON}$ degradation during off-state stress is instead often considered the result of electron trapping due to the presence of acceptor traps in the carbon doped GaN buffer [101][102][103]. In this chapter, we demonstrate that off-state drain bias stress does not only affect the dynamic $R_{ON}$ of the p-GaN HEMT but also impacts on the stability of the threshold voltage. Here we discuss in detail the mechanisms behind this observation and validate it with suitably calibrated

TCAD simulations. We also measure the positive and negative gate stress induced $V_{TH}$ instabilities to analyse the nominal operational stresses during the ON state switching operations.

### 6.2 Experimental methods

Normally-off lateral AlGaN/GaN-on-Si HEMT devices (650V, 15A) based on p-gate technology (see *Figure* 6.1*)* were used in this study. Standard dynamic Ron measurements were first performed using a Keysight B1505A power device analyser and a N1265A ultra high current expander fast switch[104]. The drain terminal of the device was biased at various OFF-state bias voltage levels (Vdstress) for 1 second. Post-stress, the N1267A [104] fast switch was used to switch the device to ON-state within a time interval of 20µs and the output characteristics at various gate bias levels were recorded.

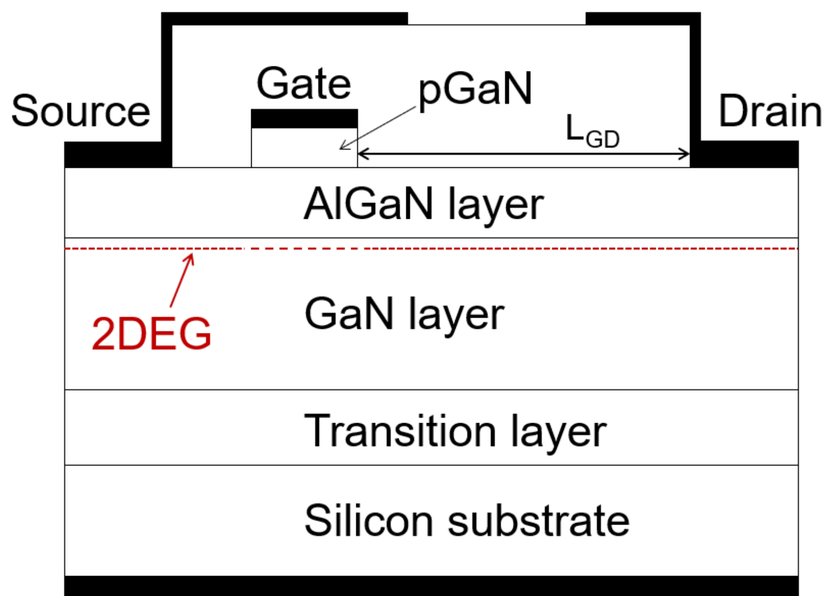



*Figure 6.1: AlGaN/GaN HEMT cross section, standard.*

The measurement methodology is illustrated in *Figure* 6.2. The dynamic $R_{ON}$ is extracted from the linear region of the output characteristics measured post drain stress. The $R_{ON}$ extracted against the various Vdstress voltages ranging from 10V to 500V is plotted in *Figure* 6.3 for gate voltage, Vg = 3V and in *Figure* 6.4 for gate voltage Vg = 5V respectively. The difference in the magnitude of the drain stress induced $R_{ON}$ increase at the two gate bias voltages (3V, 5V) is quite significant. At lower on-state gate bias the

effects of dynamic $R_{ON}$ degradation were much more severe which indicated that an increase in the threshold voltage during off-state stress may be an important factor.

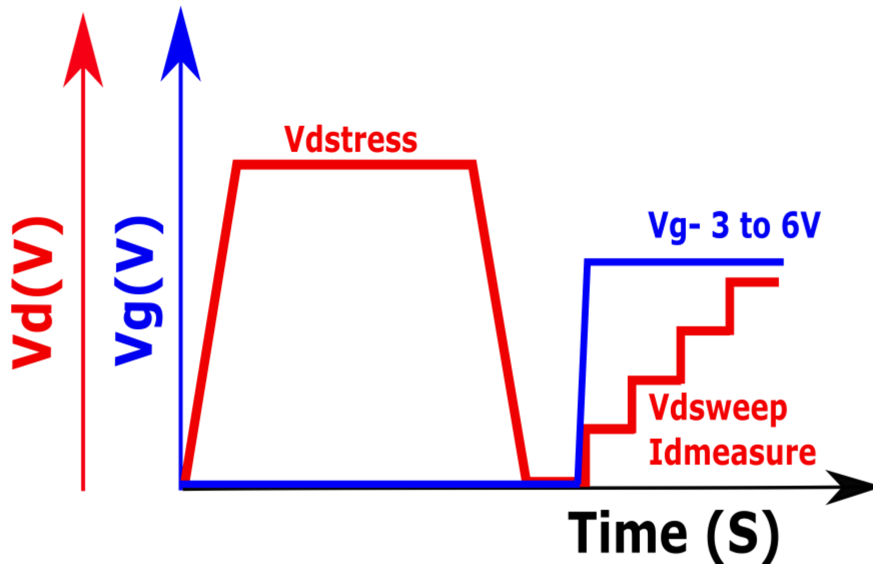



*Figure 6.2: Illustrative testing waveforms depicting Dynamic $R_{ON}$ test.*

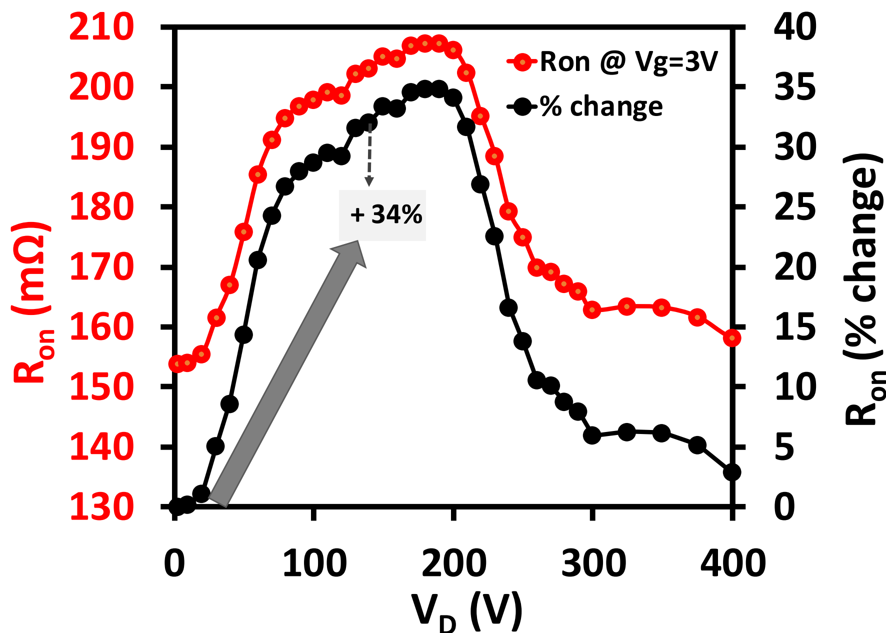



*Figure 6.3: Dynamic $R_{ON}$ degradation post drain stress at gate bias $V_G = 3V$*

Further measurement techniques to specifically investigate the $V_{TH}$ shift were used. Double pulse transfer characteristic tests such as the one shown in *Figure* 6.5 are common practice to investigate the $V_{TH}$ shift in GaN HEMT devices with the quiescent point of the gate pulse being the gate stress time as used to investigate ON state $V_{TH}$ instability in *chapter 6.4*.

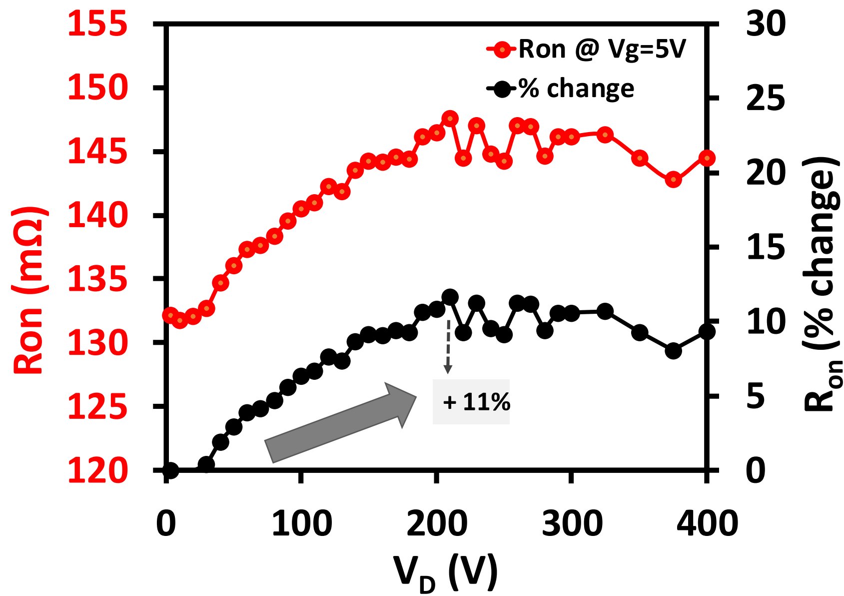



*Figure 6.4: Dynamic $R_{ON}$ degradation post drain stress at gate bias $V_G = 5V$*

For measuring OFF state stress induced $V_{TH}$ instability, a novel set up where drain off-state stress rather than a gate stress was used during the quiescent point of the gate pulse characteristic as shown in *Figure* 6.6. The stress time and measurement time in these tests were 20ms and 1ms respectively. The drain stress was ramped up to 200V (in steps of 10V) and its effect on $V_{TH}$ was observed by measuring the transfer characteristic in each case. The threshold voltage was quantified using a constant current technique i.e. $V_D$ at $I_D$ = 10μA/mm with $V_D$ = 50mV. The results for $V_{TH}$ shift at different drain stress levels are plotted in *Figure* 6.7. Both tests outlined in this section $V_D$ were performed on several devices with consistent results.

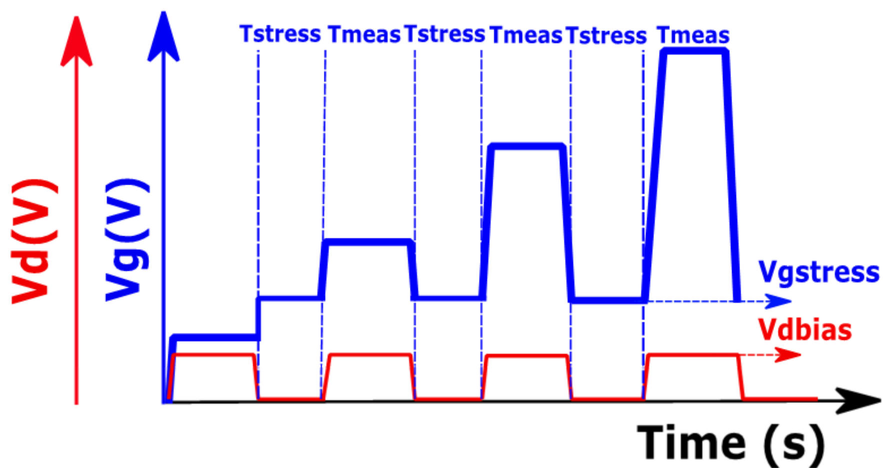



*Figure 6.5: Standard double pulse transfer characteristic test for $V_{TH}$ shift characterization with gate stress*

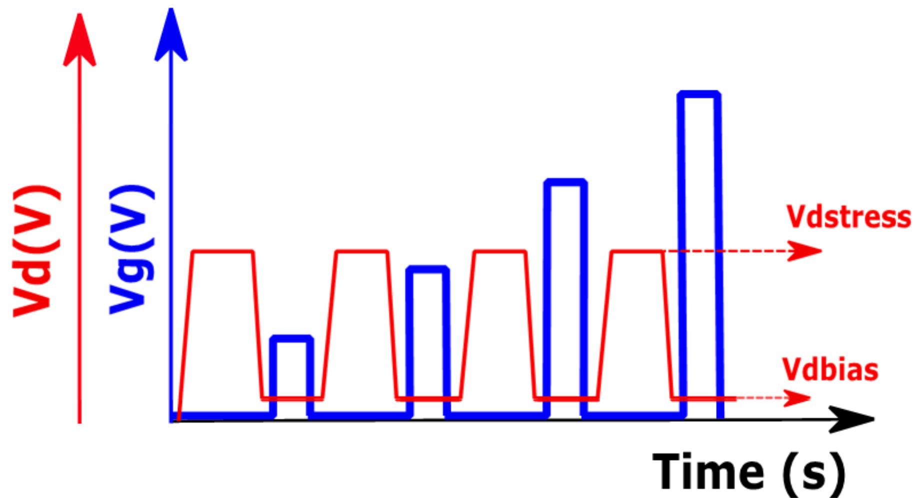



*Figure 6.6: Double pulse transfer characteristic test with off-state drain bias*

### 6.3 Effect of OFF state stress on threshold voltage

The drain stress induced dynamic $R_{ON}$ degradation in *Figure* 6.3, *Figure* 6.4 shows that the maximum % $R_{ON}$ increase at a lower gate bias $V_G$ = 3V is +34%, is significantly higher than that observed at higher gate bias $V_G$ = 5V, +11%. Such observations from dynamic $R_{ON}$ measurements indicated that an increase in the threshold voltage during off-state stress may be an important factor. This is due to the positive $V_{TH}$ shift being of less significance to the total on-state resistance at higher gate bias voltages (5V) when the 2-DEG channel is fully formed.

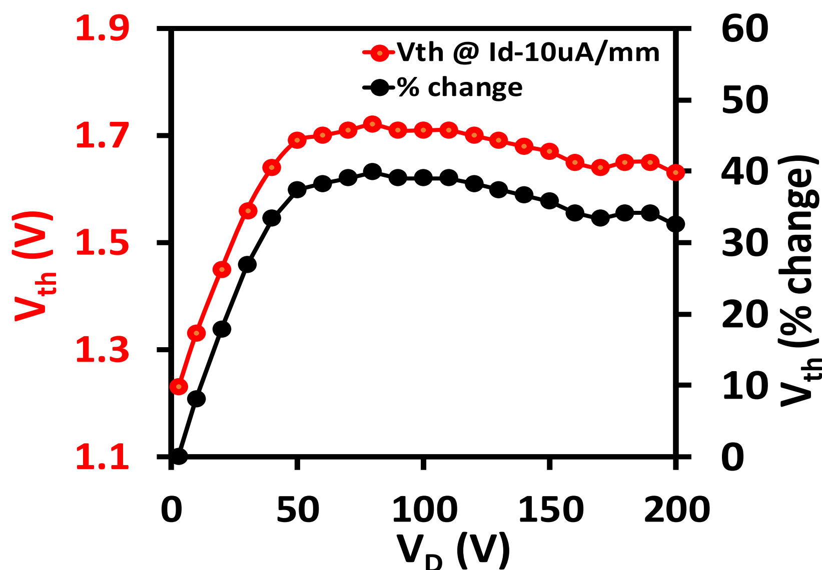



*Figure 6.7: $V_{TH}$ shift at increasing off-state bias stress ($V_D$).*

The double pulse transfer characteristic tests (as described in *Figure* 6.6) revealed a significant positive threshold voltage shift with a linear $V_{TH}$ increase up to a maximum of approximately 40%. The increase in $V_{TH}$ reaches this maximum value at $V_D$ ~ 50V and saturates as the drain bias is increased further. These results are plotted in *Figure* 6.7.

## 6.4 Effect of ON state stress on threshold voltage

In these measurements gate is stressed to understand if there will be any effect measurable as $V_{TH}$ change when the gate terminal alone is stressed without any change at the 2 DEG channel. The double pulse transfer characteristic tests (as described in *Figure* 6.5) with a positive gate voltage stress from 0 to 10V reveals a significant positive threshold voltage shift with a linear $V_{TH}$ increase up to a maximum of approximately 60%. The increase in $V_{TH}$ reaches this maximum value at $V_G$ stress voltages of ~ 6V and saturates at higher $V_G$. These results are plotted in *Figure* 6.8. This positive shift in the $V_{TH}$ is attributed to the trapping of the 2-DEG electrons due to the field pull exerted by the positive gate stress. The 2- DEG electrons predominantly get trapped in the acceptor traps at the AlGaN/GaN interface, these acceptor traps after the capture of an electron gets negatively charged and equivalently pulls up the conduction at the AlGaN/GaN interface. Thus, causing a 2-DEG depletion and an equivalent positive threshold voltage shift.

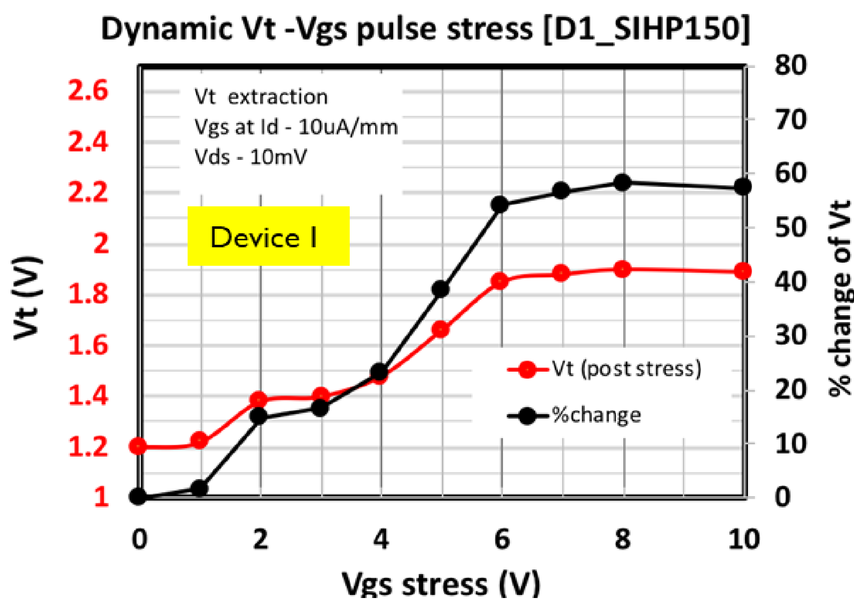



*Figure 6.8: The effect of positive $V_G$ stress voltage on the $V_{TH}$ of GaN HEMT*

## 6.5 Physical understanding and mechanisms involved

According to the analytical model of the p-gate operation [81] a threshold voltage increase can be the result of excess negative space charges in the AlGaN layer. We propose that this may be due to ionization of the out-diffused Mg [81][105] in the AlGaN region because of the high electric field at the edge of the p-GaN gate during off-state drain bias. The ionization of the Mg acceptors leads to a high concentration of holes in the AlGaN. The removal of the generated holes from the AlGaN region through the gate contact creates the charge conditions (excess negative charges in AlGaN) for a positive $V_{TH}$ shift to be observed as the holes removed during the off-state bias are not immediately replaced in the on-state condition.

## 6.6 TCAD modelling and validation

A Technology Computer Aided Design (TCAD) of the device tested is used for further understanding of the proposed model. The TCAD model is matched thoroughly with the experimental device measurements and the device specifications used in the development of the model are detailed in *chapter 4.4* [106]. p-GaN gate Mg concentration is set at $2x10^{19}$ $cm^{-3}$ and the out-diffused Mg dopant tail was introduced as acceptor traps along the p-GaN/AlGaN/GaN gate stack region to investigate the proposed model. The profile of the out-diffused acceptor trap concentration specified in the GaN HEMT TCAD model is shown in *Figure* 6.9. An off-state bias voltage ramp was applied to the device and the ionization of the Mg doping defined as acceptor traps (170meV from VB [3]) was monitored. As illustrated in *Figure* 6.10, hole de-trapping is enhanced with increasing off-state bias ($V_D$) and full ionization of the Mg acceptor traps occurs at the gate edge at $V_D$ ~50V.

The band diagram along the AlGaN layer, shown in *Figure* 6.11, illustrates the hole de-trapping in the AlGaN layer (i.e. capture of electrons from the valence band) and the hole path to the gate terminal at an off - state bias of 20V. During off-state bias conditions there is no barrier for the generated holes to be removed from the AlGaN to the p-GaN and subsequently through the gate contact. However, in on-state bias conditions the heterojunction barrier at the p-GaN/AlGaN interface is preventing the fast replenishment of holes in the AlGaN region which is essential for rebalancing the

negative charges. This recovery can be a slow process in the order of tens/hundreds of seconds.

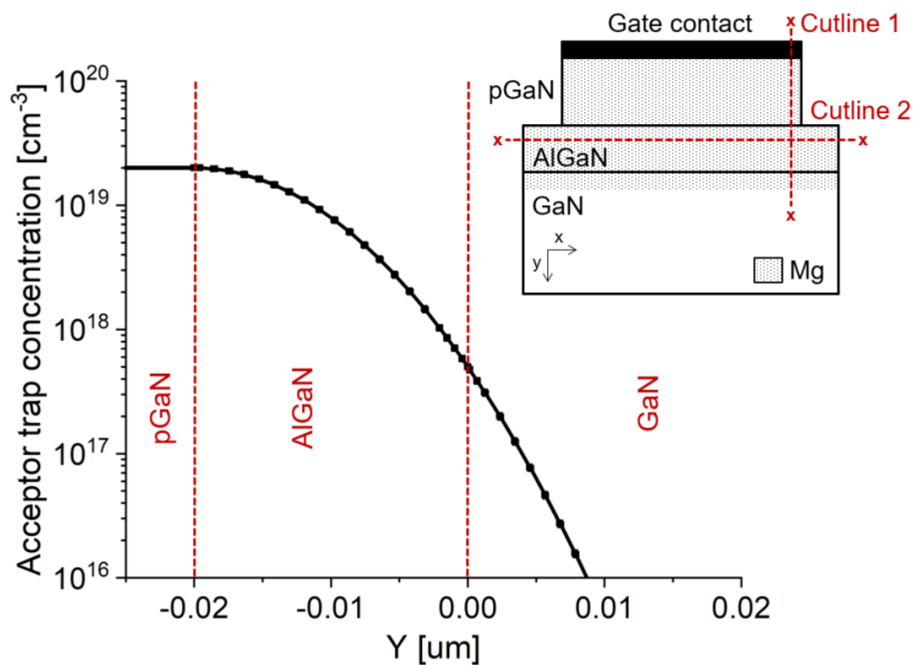



*Figure 6.9: Profile of out-diffused Mg along cutline 1 in inset*

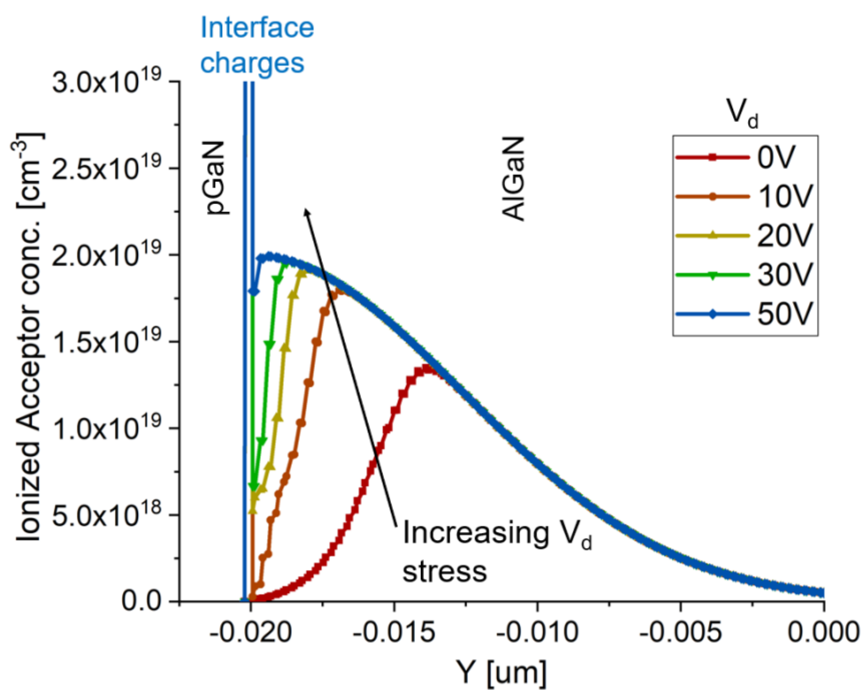



*Figure 6.10: Ionized Mg acceptor conc. at gate edge (cutline 1 in Fig.6.9 inset)*

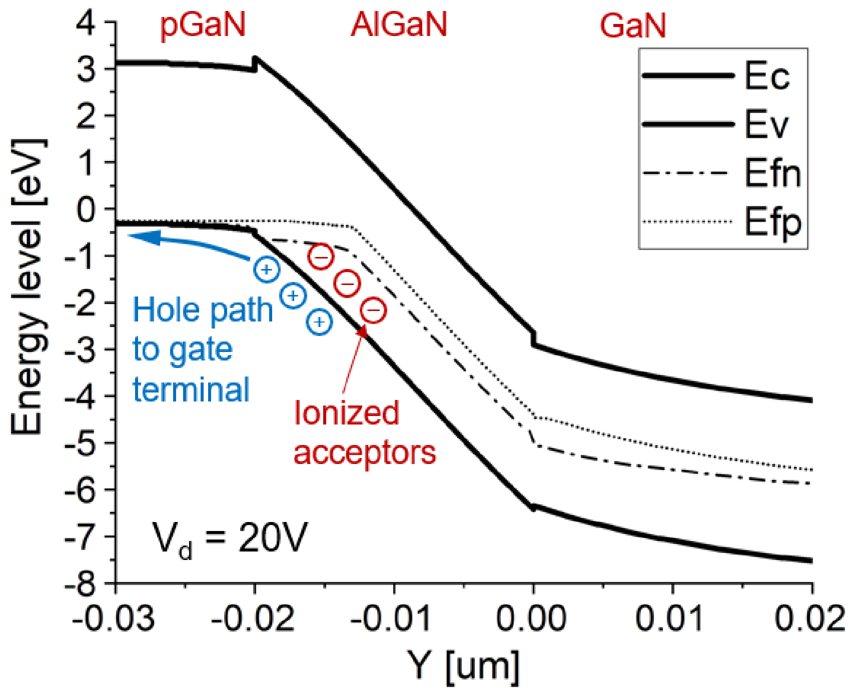


*Figure 6.11: Band diagram along cutline 1 in Fig. 6.8 inset*

The electric field across the AlGaN layer in the TCAD simulations was monitored at increasing drain off-state bias. The peak electric field at the gate edge is reached at an off-state bias of ~50V as shown in *Figure* 6.12. This agrees with the saturation in the positive $V_{TH}$ shift observed in *Figure* 6.7 at $V_D$~50V. The field plate structure has a significant effect on this.

The electric field simulations match well with capacitance measurements that confirm the depletion of the 2-DEG near the gate at around 50V observed as a sudden drop in $C_{gd}$ as shown in *Figure* 6.13. This significant decrease in $C_{gd}$ observed at $V_D<50V$ indicates the growth of the depletion region laterally from the gate contact towards the drain contact. Therefore, both measurements and simulations agree that the maximum stress on the gate occurs at around 50V and then remains constant.

Finally, the $V_{TH}$ shift using negative gate bias stress as shown in *Figure* 6.14 was also measured indicating a positive $V_{TH}$ shift (measurement setup as in *Figure* 6.5). This agrees with the results presented above as the gate bias conditions at the gate edge are similar under off-state drain stress and negative gate stress. They both result in the ionization of the Mg acceptor tail and the removal of generated holes from the AlGaN region.

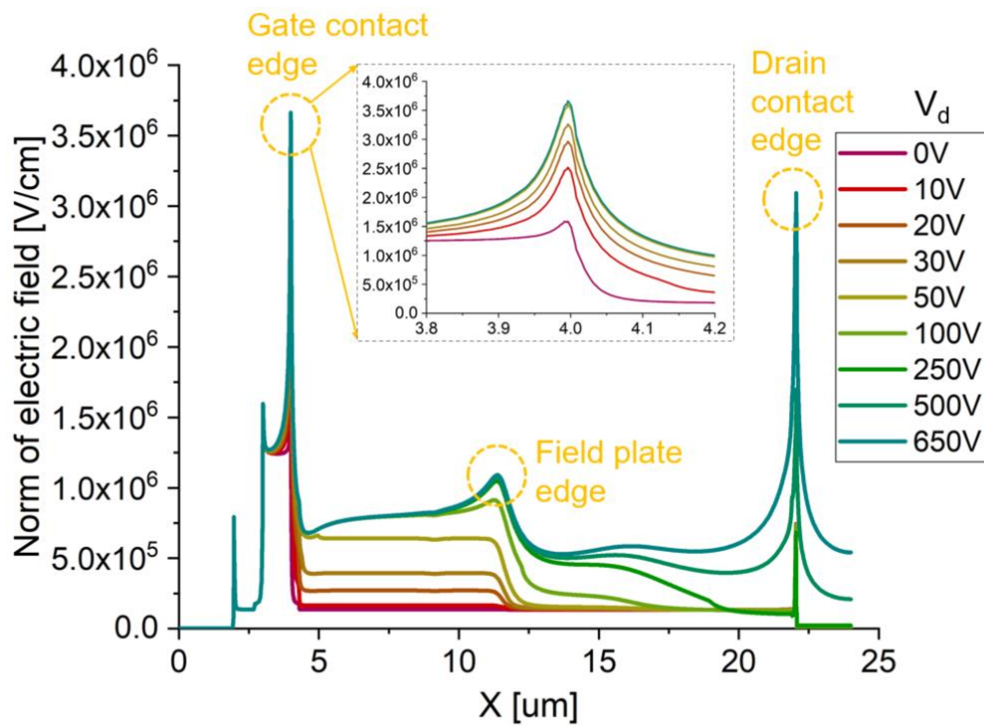



*Figure 6.12: Norm of the electric field across the AlGaN barrier along cutline 2 in Fig. 5(a) inset at different off-state bias voltages.*

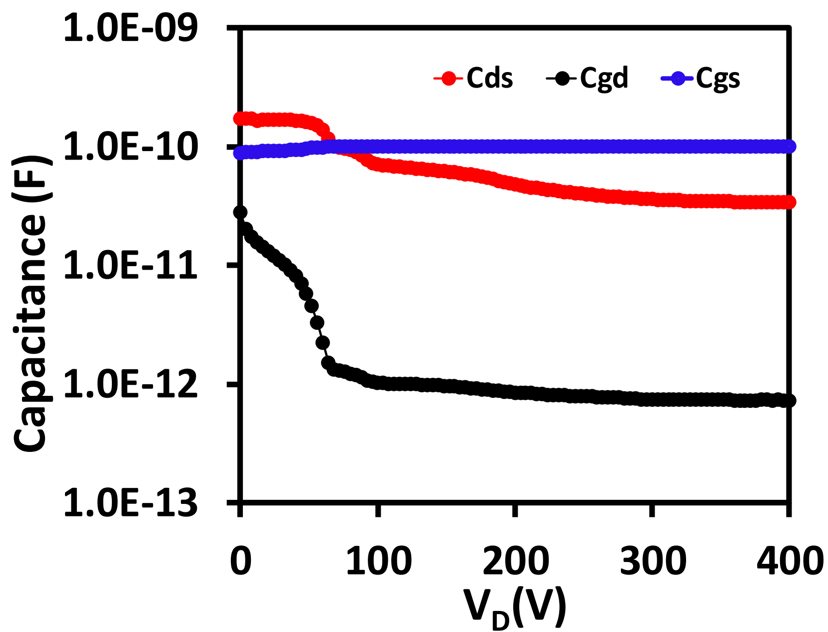



*Figure 6.13: GaN HEMT capacitance measurement.*

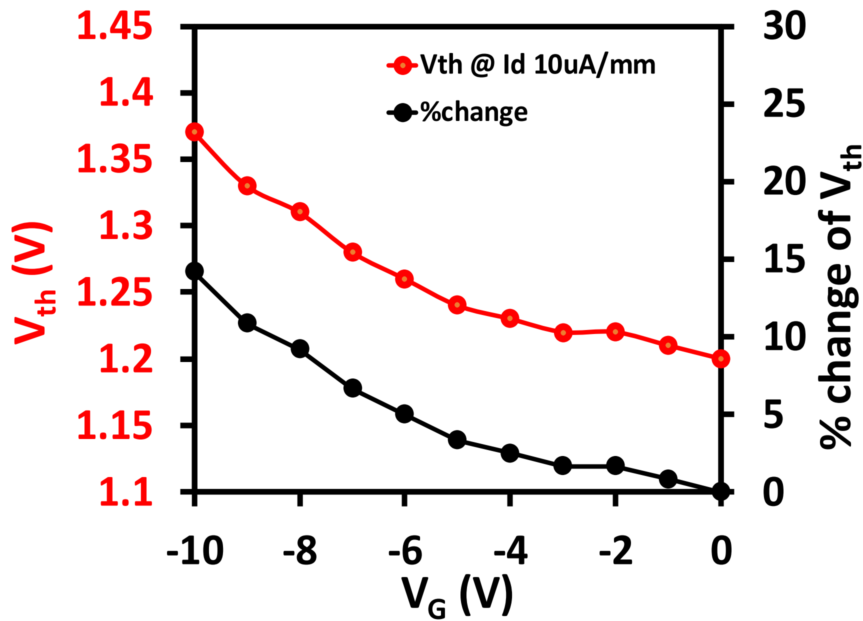



*Figure 6.14: $V_{TH}$ shift quantified using double pulse transfer characteristic test with negative gate stress.*

The TCAD modelling presented demonstrates that the mechanism described in this study is compatible with the experimental results observed. Nonetheless, the creation of non-equilibrium negative space charges (following a period of off-state stress) in other regions of the gate stack can also lead to a positive $V_{TH}$ shift. Such competing mechanisms may be distinguishable from the different stress/recovery times for which this effect is observable.

### 6.7 Conclusion

- In this chapter we investigated by means of experimental results and TCAD simulations the threshold voltage instability due to off-state drain stress in p-GaN gate AlGaN/GaN-on-Si HEMTs.
- When the drain of the p-GaN HEMT is biased in the off-state the threshold voltage ($V_{TH}$) shows a linear positive $V_{TH}$ shift increase up to ~ 40%. This increase saturates at drain bias voltages above 50V.
- The positive $V_{TH}$ shift is attributed to the ionization of acceptor traps in the AlGaN region below the p-GaN gate with the source of these trapping sites suggested to be the p-GaN gate out-diffused Mg dopant atoms.

- The ionization of the Mg acceptors due to high electric field during off-state bias and the removal of the generated holes from the AlGaN region through the gate contact creates the charge conditions for a positive $V_{TH}$ shift.
- The sharp decrease in the gate drain capacitance ($C_{gd}$) for $V_D < 50V$, the simulated gate edge electric field reaching its peak for a drain voltage bias $V_D \sim 50V$ and the positive threshold voltage shift observed for negative gate stress further validate the proposed model.

# 7. Recovery time measurement technique post threshold voltage instability

*Threshold voltage instability due to the $V_{TH}$ measurement, nominal ON state stress and OFF-state stress are quantified, measured and the underlying physical mechanisms are understood in chapter 5,6. It is essential to know the time taken to recover after threshold instability for the power system designers to enable reliable designs overcoming the instability induced transient. In this chapter a measurement technique that could eliminate the effect of measurement induced instability and measure the time required to recover from the threshold voltage change post stress is explained. The effect of the stress voltage, effect of stress time on the recovery time is also summarised.*

## 7.1 Introduction

Threshold voltage ($V_{TH}$) instability is reported during nominal operational OFF state stress [107][108], ON state stress [88][109][110][111] and $V_{TH}$ measurements [112][113][114]. $V_{TH}$ instability is often attributed to the dynamic charge conditions created in the gate stack operationally. For instance, trapping of 2-DEG electron in the AlGaN barrier cause a positive $V_{TH}$ shift. Whereas accumulation or depletion of holes in the p-GaN gate region cause a negative & positive $V_{TH}$ shift respectively. Threshold voltage instability remains a serious concern as negative VTH shift could lead to faulty turn on of the device and positive $V_{TH}$ shift could mandate higher gate drive voltages alongside causing an increase in reverse conduction voltages adding to the dead time losses while switching as discussed previously in chapter 2.6.1. It is essential for the power system designers to understand the time taken for the threshold voltage to recover post an instability event to foresee the potential reliability issues during the transients. The reported $V_{TH}$ recovery time measurement methods [115] typically involve a stress pulse at the gate terminal or the drain terminal, followed by a threshold voltage measurement by a full transfer characteristic ($I_D$-$V_G$) sweep. However, in these measurement techniques, the additional $V_{TH}$ instability arising during the event of VTH measurement post stress is not decoupled and the estimated recovery time measurements can be misleading. Xiangdong et.al [114] recommended ultrafast transfer characteristic measurement sweeps with total measurement time <2μs to eliminate measurement

induced effects however it involves expensive fast measurement units Keysight B1530A, Agilent 81110, AMCAD with dedicated interfaces and Bilal Akin et.al [63] highlighted these measurement issues and developed a setup at application level to measure realistic VTH instability effects due to OFF state stress. Also, the p-GaN gate HEMT's gate stacks across manufacturers have design variations in gate contact (Ohmic or Schottky) and process variations in terms of active Mg doping (p-GaN doping). These variations across manufacturers induce variations in the trapping/de-trapping processes in the gate stack associated with the $V_{TH}$ shift caused during the $I_D$-$V_G$ sweep. Thus, the recovery time estimated by the existing techniques involving an $I_D$-$V_G$ sweep will embed additional $V_{TH}$ shift variations due to the $I_D$-$V_G$ sweep, and this additional shift varies across manufacturers. Hence, a measurement technique to precisely measure recovery time, eliminating the inconsistencies arising due to the measurement technique, is required. In this work, a $V_{TH}$ recovery time estimation technique based on sensing the channel current prestress and post-stress at a single gate voltage at an optimum time interval is proposed. This technique eliminates the $V_{TH}$ shift caused by the transfer characteristic sweep, which is typically present in the nominal measurement schemes. The ON state-induced $V_{TH}$ instability recovery time is estimated by utilizing this technique, and the effect of stress voltage and stress time on recovery dynamics is understood. Based on the time taken to recover post-instability and the slope of the recovery characteristics, the technique is further used to empirically ascertain the trap location.

### 7.2 Experimental methods and measurement technique

Normally-off lateral AlGaN/GaN-on-Si HEMT devices (650V, 15A) based on p-gate technology with a threshold voltage of 1.35 V are used in this study. The devices used are based on TSMC technology [86] with 60-80nm thick Mg doped p-GaN layer, 15-25nm of AlGaN layer and ~ 5μm of GaN epitaxy layer grown on silicon substrate with an intermediate transition layer. The devices under investigation had a Schottky gate with a threshold voltage of 1.3 V, which, upon gate stress (1–4 V), showed a positive threshold voltage shift, as measured by a double pulse test. The proposed recovery time measurement technique involves a 'stress pulse' where the gate stress voltage ($V_G$_stress) and the stress time (T_stress) can be defined. The gate stress is followed by

a ‘measurement pulse’ which is fixed at a gate voltage ($V_G$_measure) 10% greater than a $V_{TH}$ with a fixed pulse width (T_meas). T_meas of the ‘measurement pulse’ is selected to ensure that $I_D$ is sampled precisely without the influence of measurement-induced stress. To estimate T_meas, the drain current ($I_D$) is sampled over time at a $V_G$ bias of 1.1 $V_{TH}$, and the time period in which the $I_D$ sampled is stable is chosen as T_meas [112][113]. For the samples under investigation, it was observed that at a $V_G$ bias of 1.1 $V_{TH}$, $I_D$ reached a stable phase between 100 and 500 µs, interpreted as $I_D$stable-Tzone (chapter 5, Figure 5.3), beyond which $I_D$ decayed rapidly. Thus, a T_meas of 200 µs was chosen for these samples in this analysis hereafter. The drain terminal ($V_D$ bias) was maintained at 50 mV throughout the course of measurements. The $I_D$ measured post-stress by the measurement pulse after a delay of T_stable is termed ‘$I_D$_recovery’. The $I_D$ measured with no stress pulse by the measurement pulse after a delay of T_stable is termed ‘$I_D$_reference’ (Figure 7.1). The time interval between stress pulse and measurement pulse when $I_D$_recovery matched $I_D$_reference was estimated as the recovery time. The time interval was iteratively varied through various times to estimate the recovery time for a given condition. In all the measurements, $I_D$_recovery was sampled after 100 µs with a measurement pulse of width 200 µs. Keysight B2912A high resolution SMUs were used to realize the measurement schematic involving variable $V_G$_stress (1.5/2/4 V) levels and fixed $V_G$_measure (1.1 $V_{TH}$) pulses. Due to hardware programming interface limitations, a single SMU cannot be used to generate the stress and recovery pulse at different voltage levels. To overcome this, two Keysight B2912A high-resolution SMUs with a protection Zener diode (Nexperia IN4728A) as shown in Figure 7.2 a), were used to realize the recovery measurement setup. The 2 SMUS were synchronized by a N1294A-032 I/O trigger cable and switched as required. The gate terminal was stressed at ($V_G$_stress) 1.5 V–4 V for various time intervals (T_stress) from 500 µs to 100 s by SMU1. The time taken for the depleted 2-DEG channel to recover to prestress levels was sensed by $I_D$ sampled in the measurement pulse by SMU2, as shown in Figure 7.1. Post-stress, depending on the extent of positive (+ve) $V_{TH}$ shift, a drop in $I_D$ (2-DEG density in the channel) sampled at $V_G$_measure by the measurement pulse relative to prestress levels was seen. The $V_G$_measure was chosen at optimum levels (1.1$V_{TH}$) to ensure that it was close to $V_{TH}$. If $V_G$_measure is >> 1.1 $V_{TH}$, there exists a possibility that the 2-DEG channel density is too high relative to the 2-DEG changes caused by gate stress, thus making the

$I_D$ measured insensitive to stress and recovery. In other words, the $I_D$ sensed would be from the constant regime of $I_D$-$V_G$ transfer characteristics, as shown in Figure 7.2 b), missing the dynamic component caused by stress. Post-stress $I_D$, thus measured by measurement pulse after a recovery time (iteratively changed), is plotted as % normalized with respect to $I_D$_reference (prestress channel currents measured at $V_{GS}$ = 1.1 $V_{TH}$, $V_{DS}$ = 50 mV), as shown in Figures 7.3a–c. For example, after a 2 V, 500 µs stress pulse was administered, followed by a recovery time of 0.05 s; the $I_D$ measured in the measurement pulse was 35% of $I_D$_reference, as shown in the encircled in Figure 7.3 b. $I_D$_reference is shown as 100%, and the % recovered with respect to various recovery times is plotted to observe the recovery dynamics. The time when % $I_D$ recovered reaches 100% is representative of the time taken for the $V_{TH}$ to recover post-stress, corresponding to the stress voltage/time. By employing this technique of using a short measurement pulse instead of a complete transfer characteristic sweep, the effect of measurement-induced $V_{TH}$ instability was removed, providing an actual estimate of the recovery time. This recovery time measurement approach, post $V_{TH}$ instability, can be an apt representative replacement for the existing methods.

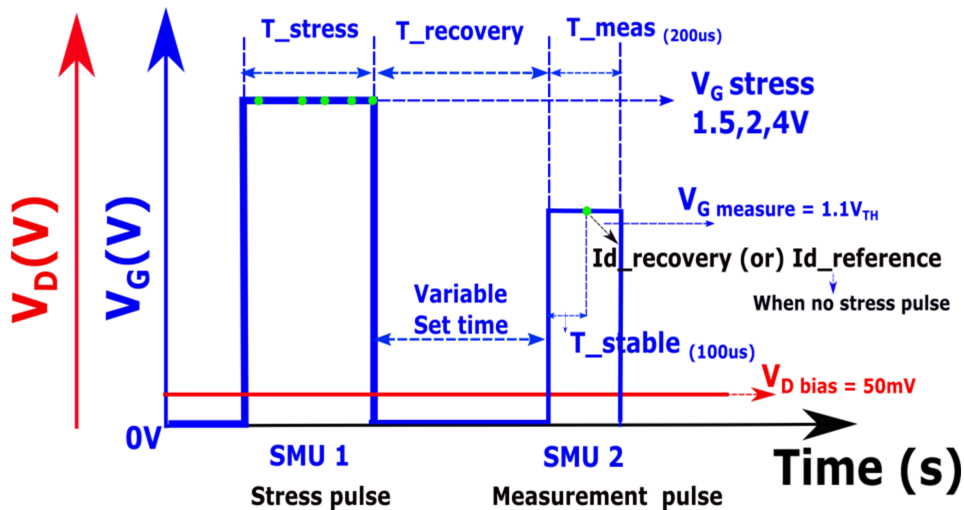
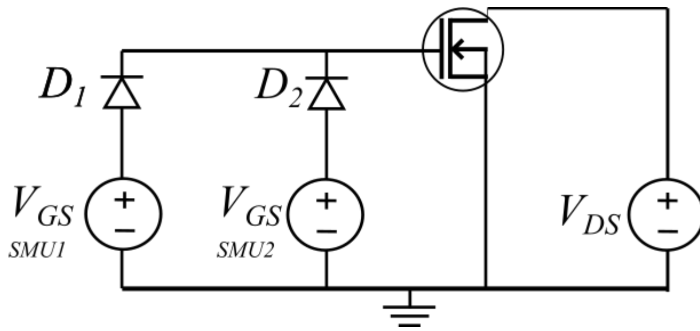



*Figure 7.1: Illustrious gate and drain terminal voltage waveforms demonstrating the threshold voltage recovery time measurement technique*

The effect of the stress voltage and the stress time on $V_{TH}$ recovery dynamics and recovery time are shown in Figure 7.3 (a-c), Figure 7.5 (a-g) and Figure 7.4, Figure 7.6 respectively.



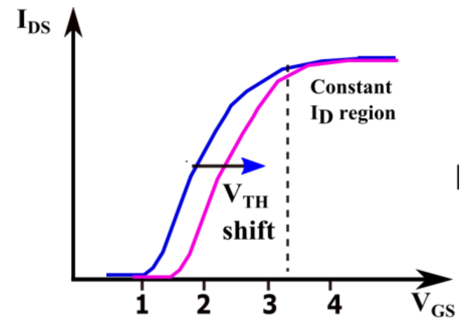




Fig 7.2 a) Fig 7.2 b)

*Figure 7.2 a): Schematic of the measurement setup where SMU1 and SMU2 are alternatively switched corresponding to the test waveform shown in Figure 7.1 b): Transfer characteristic showing constant $I_D$ region insensitive to $V_{TH}$ shift caused by $V_G$ stress.*

### 7.3 Effect of stress time and voltage on the recovery time

**As stress time increases, a larger decrease in the $I_D$ is observed**; this decrease is attributed to the depletion of electrons in 2-DEG. With increasing stress time from 500 µs to 50 ms at a $V_G$_stress of 1.5 V/2 V, the $I_D$ sampled at 1.1 $V_{TH}$ post-stress shows a decreasing trend, and for stress times > 50 ms, the decrease in $I_D$ reaches saturation with no further decrease, as seen in Figure 7.3 a) b). At a higher $V_G$_stress of 4 V (Figure 7.3 c), even a short stress time of 500 µs causes a strong 2-DEG depletion (sensed by $I_D$ sampled at 1.1 $V_{TH}$ post-stress), and with further increasing stress times, the 2-DEG depletion saturates. The time taken by the drain current to recover to 100% of its prestress current levels, extracted at 1.1 $V_{TH}$, is defined as the recovery time (Tr). The recovery process is non-existent to negligibly small until 0.5s and strongly kickstarts after 5s, and the relative rate of recovery of trapped 2-DEG electrons for different stress voltages and stress times is similar, as observed from the slope of recovery curves in Figure 7.3 a–c. With increasing T_stress from 500 µs to 50 ms, the recovery time (Tr) extracted shows an increasing trend, as observed in region 1 of Figure 7.4. When T_stress is increased from 50 ms to 10 s, the Tr extracted plateaus, and when T_stress is increased from 10 s to 100 s, the Tr extracted shows a strong increasing trend, as observed in regions 2 and 3, respectively (Figure 7.4). These observed trends agree with the 2-DEG depletion trends observed in Figure 7.3 a–c.

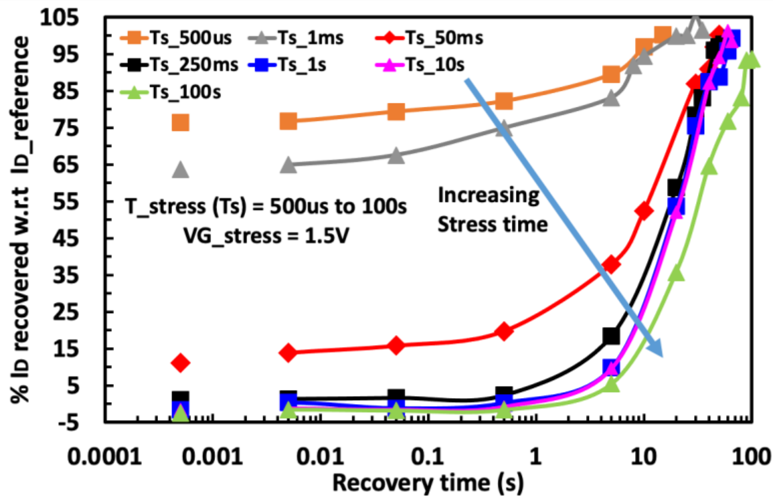



Fig 7.3 a)

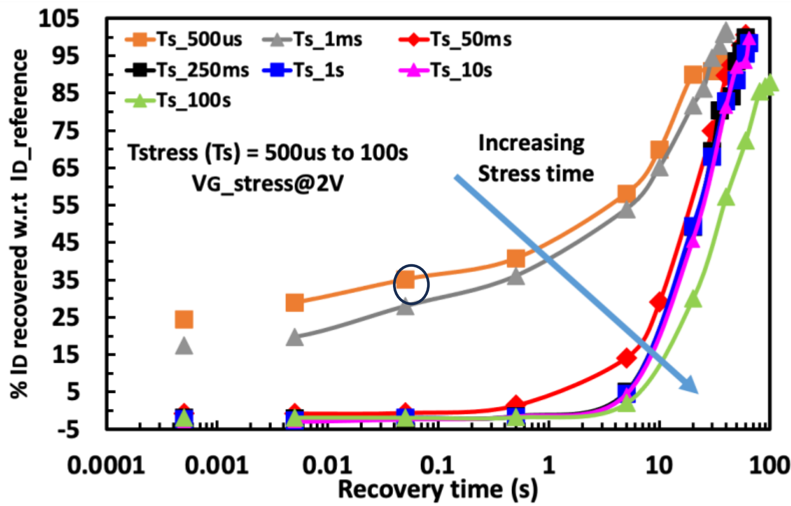



Fig 7.3 b)

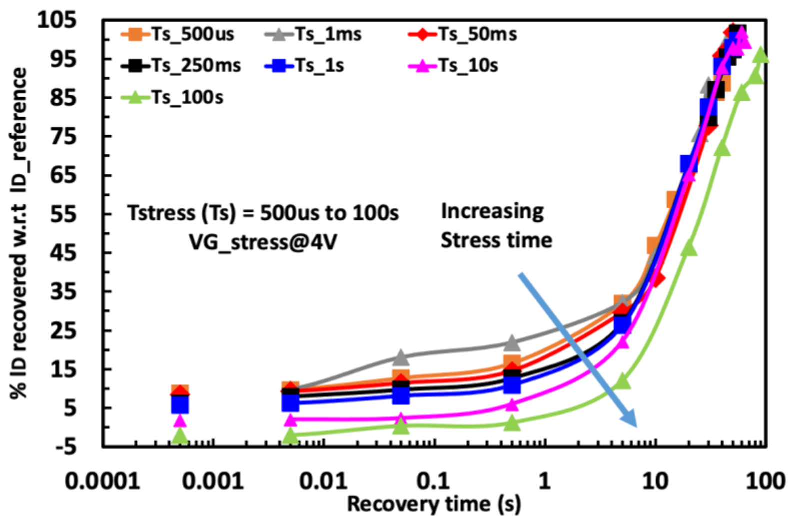



Fig 7.3 c)

*Figure 7.3: Dynamics of $V_{TH}$ recovery measured by time taken for $I_D$ to recover to prestress levels ($I_D$-reference) across varying stress times (500 µs to 100 s) for different $V_G$_stress values of 1.5 V (**a**), 2 V (**b**), and 4 V (**c**).*

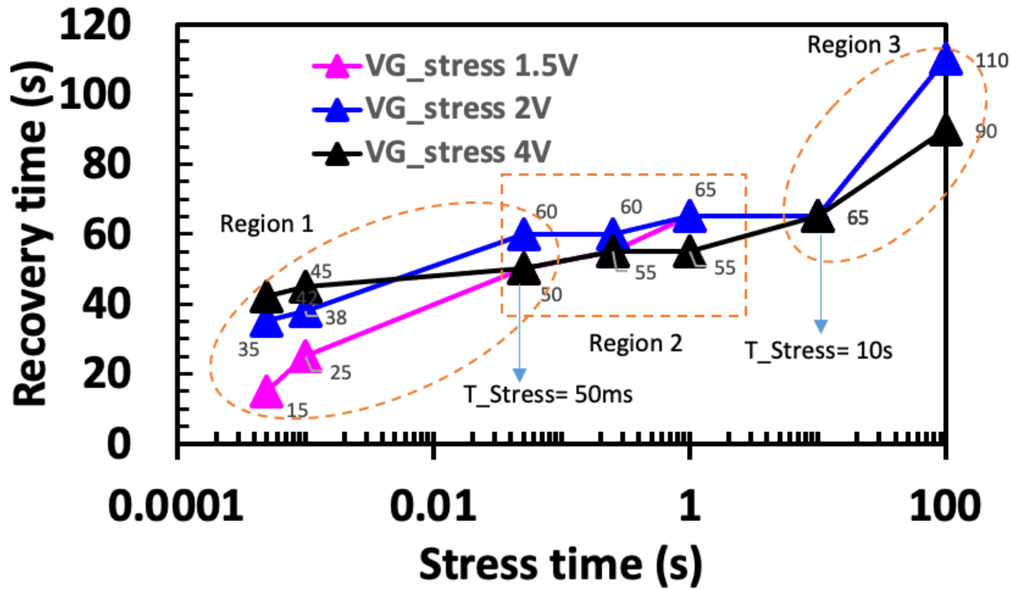



*Figure 7.4: Effect of $V_G$ stress time on the recovery time extracted by the proposed technique illustrating the recovery trends*

**As stress voltage increases, a larger decrease in the $I_D$ is observed**, revealing the depletion of electrons in 2-DEG, as observed in Figure 7.5 a–g. With increasing $V_G$_stress from 1.5 V to 4 V, for stress times of 500 µs and 1 ms, the $I_D$ sampled at 1.1 $V_{TH}$ post-stress shows an evidently decreasing trend (Figure 7.5 a,b). At a $V_G$_stress of 1.5 V and 2 V, with stress times ranging from 50 ms to 100 s, it is observed that the $I_D$ sampled at 1.1 $V_{TH}$ post-stress decreases marginally. Upon further increase of $V_G$_stress to 4 V, with stress times ranging from 50 ms to 100 s, the decrease in $I_D$ starts to saturate and gradually reverse, as seen in Figure 7.5 c–g. At lower stress times of 500 µs and 1 ms, the recovery time increases with stress voltage (Figure 7.6). At stress times beyond 50 ms, the recovery time is similar for stress voltages of 1.5 V and 2 V and marginally decreases at 4 V (zone 2 of Figure 7.6). It is to be noted that at a $V_G$_stress of 4 V, the $I_D$ change due to 2-DEG trapping is negligibly small compared to the high channel current, as the device operates in the constant $I_D$ regime of the transfer characteristic (Figure 7.2 b). Also, in instances when the $I_D$ has collapsed fully to off-current levels, either by increasing time/voltage to high levels, it does not mean the $V_{TH}$ shift has stopped at that respective stress time and voltage.

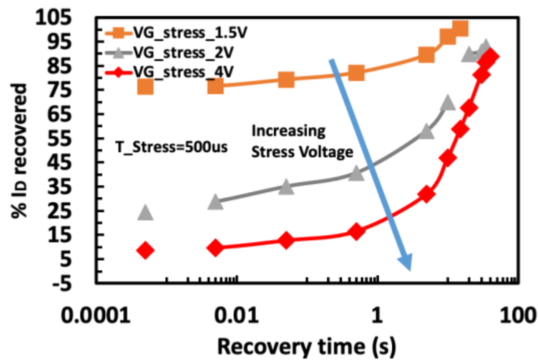



Fig. 7.5 a)

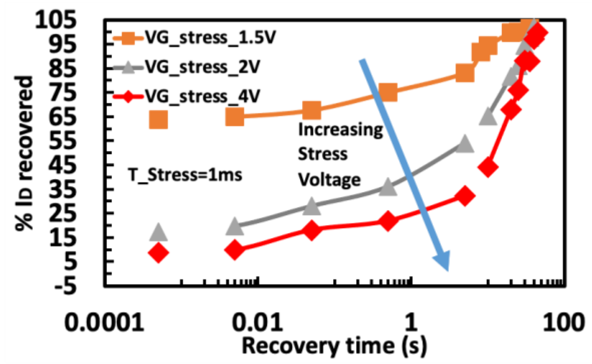



Fig. 7.5 b)

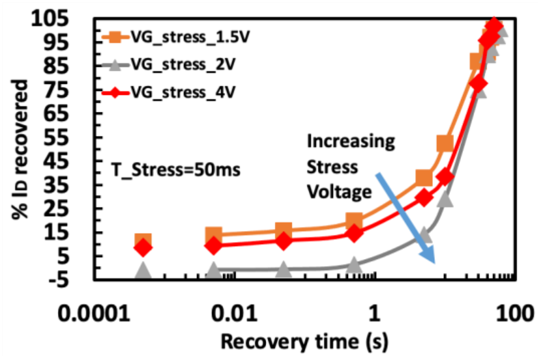



Fig. 7.5c)

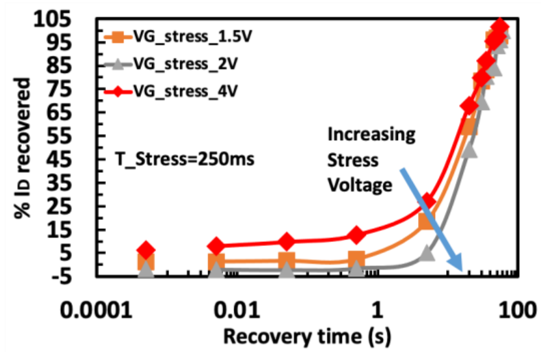



Fig. 7.5 d)

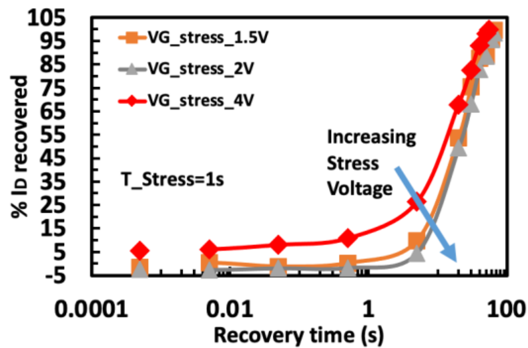



Fig. 7.5 e)

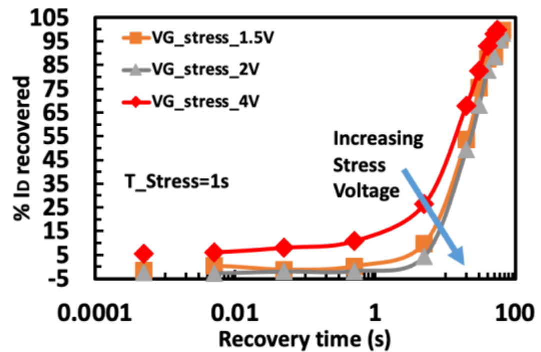



Fig. 7.5 f)

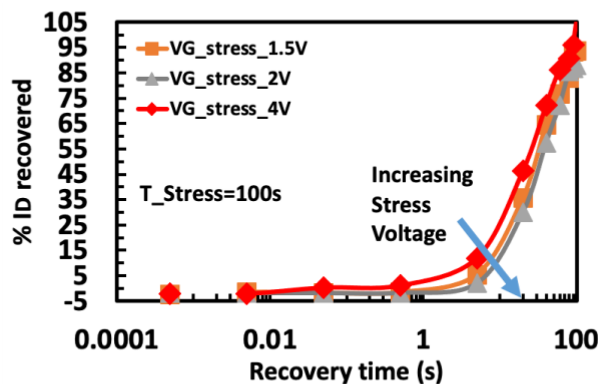



Fig. 7.5 g)

*Figure 7.5: Dynamics of $V_{TH}$ recovery sensed by time taken by $I_D$ to recover to prestress levels ($I_D$-reference) for varying stress voltages (1.5/2/4V) at various stress times (500μs – Fig 7.5 a; 1ms – Fig 7.5 b; 50ms – Fig 7.5 c; 250ms – Fig 7.5 d; 1s – Fig 7.5 e; 10s – Fig 7.5 f; 100s – Fig 7.5 g;)*

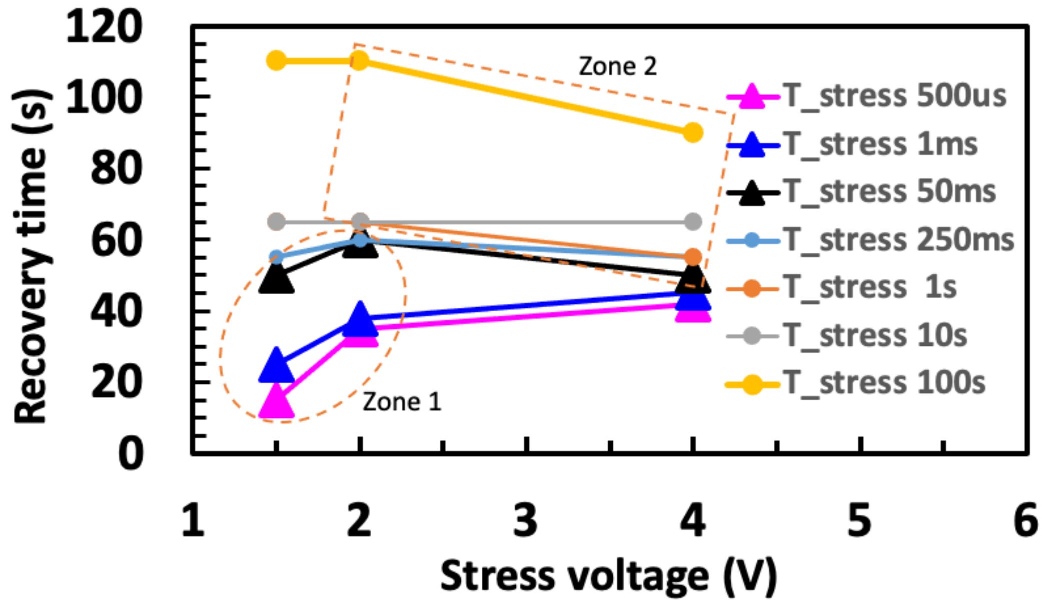



*Figure 7.6: Effect of $V_G$ stress voltage on the recovery time extracted by the proposed technique illustrating the recovery trends*

In summary,

- As stress time increases, recovery time also increases until reaching a critical stress time of 50 ms, beyond which recovery time plateaus until a stress time of 10 s.
- The effect of increasing stress time on recovery time is subdued while the gate is stressed at a higher voltage (4 V).
- As stress voltage increases, recovery time also increases until a critical stress voltage (2 V), beyond which recovery time plateaus.
- The effect of increasing stress voltage on recovery time is subdued while the gate is stressed beyond higher stress times (50 ms).

Thus, based on the trends observed above, there are three T_stress zones: (a) 500 μs to 50 ms, (b) 50 ms to 10 s, and (c) 100 s (marked as region 3 in Figure 7.4). There are also two $V_G$_stress groups: (a) $V_G$_stress = 1.5 V and 2V, and (b) 4V (marked as zone 2 in Figure 7.6).

## 7.4 Process of 2-DEG trapping and recovery

The 2-DEG depletion causing the positive $V_{TH}$ shift can be explained by the trapping of the 2-DEG electrons during the positive gate bias. At the positive gate bias, a vertical field pull can cause trapping of 2-DEG electrons at four possible locations/regions: (a)

the pGaN/AlGaN interface, (b) the AlGaN bulk, (c) the AlGaN/GaN interface, and (d) the AlGaN/GaN interface and borderline region (some nanometers inside the AlGaN region from the AlGaN/GaN interface is referred as the borderline region). Various capture processes are in play depending on the trapping location, as depicted in Figure 7.7. For example, direct tunneling (DT), trap-assisted tunneling (TAT), and phonon-assisted tunneling (PAT) are processes associated with 2-DEG trapping at the AlGaN bulk. Thermal transition and thermionic emission are the capture processes associated with 2-DEG trapping at the p-GaN/AlGaN interface. Direct capture, direct capture together with borderline hopping, are the processes associated with 2-DEG gettting trapped at the AlGaN/GaN interface and borderline region. The capture time varies depending on the location of traps and the respective processes involved. The stress time or the stress voltage can effectively control how many 2-DEG electrons are trapped and the location where they are trapped. However, the trap energy levels, trap density, and their distribution are fixed irrespective of the stress voltage (operational levels) and time. Hence, the recovery time is solely dependent on the emission. The equations explaining the capture and emission process are detailed in *chapter 33.3* and the emission time [76] as given by

$$\tau_e = \frac{\exp(E_c - E_T)/\mathrm{KT}}{\sigma_n * v_{th} * N_c}$$

where $\tau_e$ is the emission time of the electron, $E_c$ is the conduction band minimum energy level, $E_T$ is the trap energy level, K is the Boltzmann constant, T is the temperature, $\boldsymbol{\sigma_n}$ is the electron capture cross-section of the trap, $\boldsymbol{v_{th}}$ is the electron thermal velocity, and $N_c$ is the effective density of states in the conduction band. With exponential dependence on trap electron energy level position, the recovery time has a direct exponential dependence on the difference in energy levels between trap energy level, conduction band minimum, and inverse linear dependence on capture cross section and effective density of states. Thus, recovery time and its dynamics can be an effective indication of the trap characteristics.

*Figure 7.7: Illustrative viable capture processes by which 2-DEG could be trapped due to vertical field pull by positive gate bias*

*Figure 7.8: $I_D$ sampled at $V_G$ bias of 1.5 V over various stress times (Ts) and respective recovery times (Tr) extracted by this recovery time estimation technique*

### 7.5 Hypothesis on Trap location and recovery processes

Based on the recovery dynamic shown in Figures 7.3a–c and 7.5a–g, it is observed that 90% of the $I_D$ recovery post-stress for all stress times and voltages happens between 5 s and its respective Tr. The recovery process has predominantly similar rates of recovery (slope) in most cases where trap occupation levels are not negligibly small (for stress times > 1 ms), implying similar emission processes. For similar emission processes

with similar rates of emission irrespective of $V_G$_stress voltages and times, the trapping or capture processes should be a simplistic, repetitive process and not significantly altered by voltage/time changes. On the other hand, if trapping/emission processes involve crossing barriers such as AlGaN or tunneling through barriers, they might be affected by stress voltage and times, affecting barrier shape and height. Thus, it is hypothesized that 2-DEG getting trapped at the AlGaN/GaN interface is the dominant process relative to the other processes highlighted in Figure 7.7

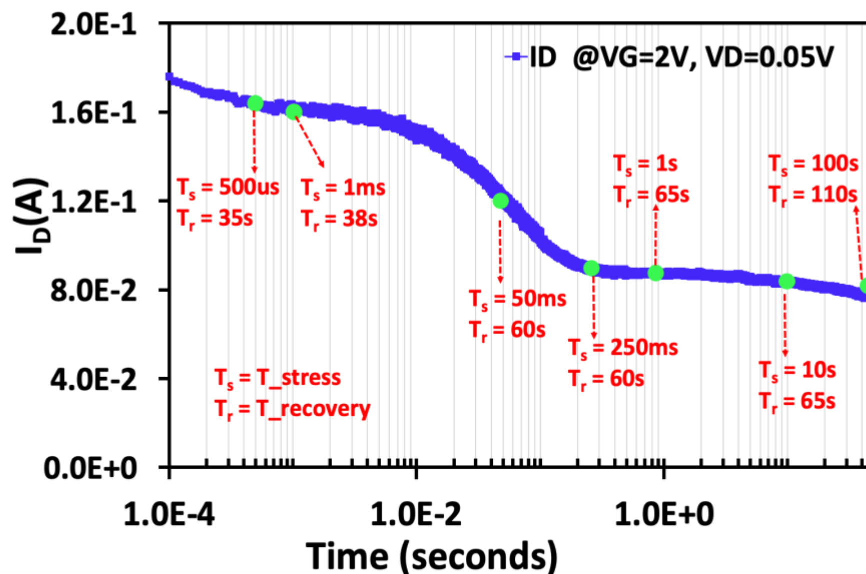



*Figure 7.9 $I_D$ sampled at $V_G$ bias of 2 V over various stress times (Ts) and respective recovery times (Tr) extracted by this technique*

Having empirically hypothesized the trapping location, the trapping processes during stress and emission processes post-stress at the AlGaN/GaN interface, represented in terms of band diagram, are graphically illustrated for $V_G$_stress values = 1.5 V and 2.0 V. Prestress, the conduction band minima (EC_min) is above the GaN buffer electron fermi level (eEf_GaN), signifying the normally-off operation; the difference between the EC_reference and the EC_min is the conduction band discontinuity (Ecbd), which remains constant irrespective of stress voltage/time. On application of +ve gate voltage (Time = 0), EC_min moves below eEf_GaN, forming a 2-dimensional quantum confined space holding the 2-dimensional electron gas (2-DEG). Over time (stress phase), the 2-DEG starts to get trapped at the shallow acceptor traps (ET_shallow) at the AlGaN/GaN interface due to the field pull (processes 1.0 and 1.1, respectively, in Figure 7.10).

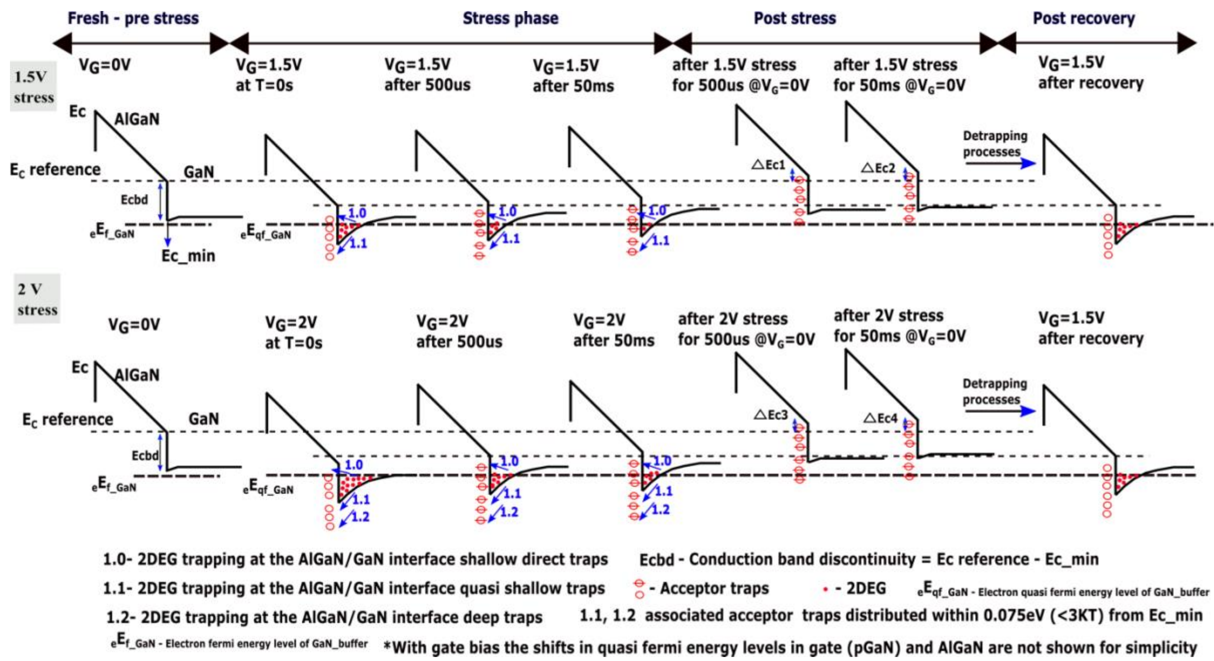



*Figure 7.10: Illustrative schematic showing the AlGaN/GaN interface's conduction band movement relative to fermi energy level prestress, during stress with increasing times, post stress, post recovery after a relaxation time for 1.5V and 2V stress*

When the stress time increases:

- The number of 2-DEG electrons becoming trapped in the ET_shallow level increases until trap levels are fully filled or 2-DEG is fully depleted and ID decays correspondingly, as shown in Figure 7.8 and in Figure 7.9 at constant gate bias (1.5/2 V).
- The acceptor trap, after trapping an electron, becomes negatively charged, generating a net negative charge in the AlGaN region, causing EC_min to move up relative to the fermi energy level, representing rapid 2-DEG depletion (stress phase in Figure 7.10).
- When the gate stress voltage increases, 2-DEG density increases, and the 2-DEG electrons become trapped at the deeper (ET_deep) acceptor trap energy levels (process 1.2 in Figure 7.10 for $V_G$_stress values of 2 V; process 1.3 in Figure 7.11 for $V_G$_stress values of 4 V).

The traps are termed deep/shallow based on their relative position with respect to Ec_min. During the stress phase, 2-DEG electrons get trapped at the AlGaN/GaN interface, causing the conduction band maxima at the interface to move up relatively, correlating with the extent of trapping.

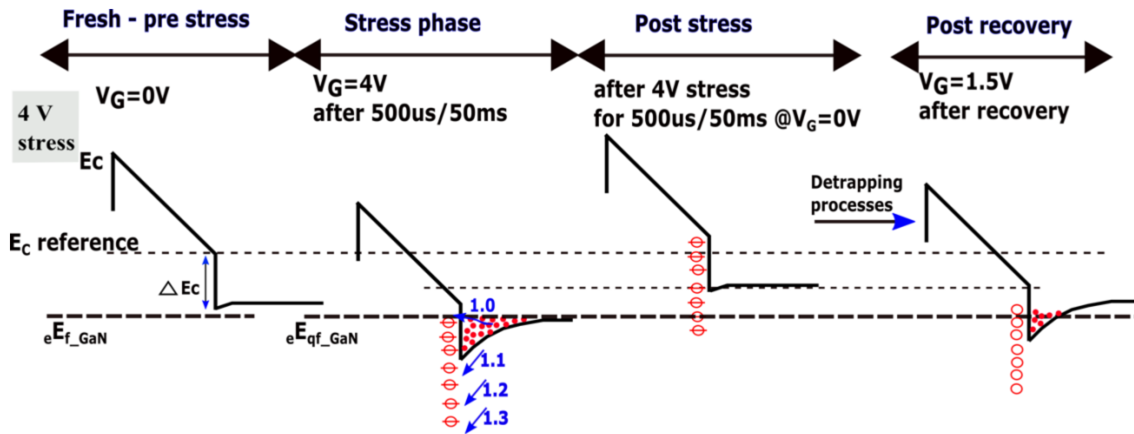



*Figure 7.11: Illustrative schematic showing the AlGaN/GaN interface's conduction band movement relative to fermi energy level prestress, during stress with increasing times, post stress, post recovery after a relaxation time for 4V stress*

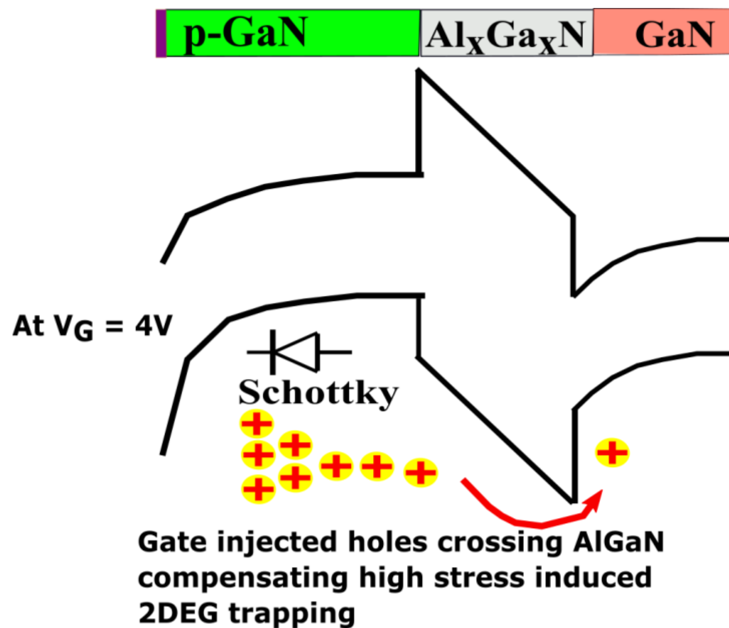



*Figure 7.12: Equivalent band diagram showing the high hole injection across the Schottky gate enabling holes to cross the AlGaN barrier*

Once the stress is removed (post-stress at VG = 0V), the number of 2-DEG electrons trapped during the stress phase determines the extent by which conduction band maxima at the interface moves up relative to Ec_reference, measured as $\Delta Ec$. Because of increased 2-DEG electron trapping with increasing stress time, $\Delta Ec1\ (for\ Tstress\ 500us) < \Delta Ec2\ (for\ Tstress\ 50ms)$, and $\Delta Ec3 < \Delta Ec4$, as shown in Figure 7.10. During this period, the devices are allowed to relax at room temperature,

and the trapped electrons are emitted from ET_shallow or ET_deep to the triangular quantum well by thermal energy.

As the emission time has an exponential dependence on ET-EC, those trapped at ET_deep will take more time to emit, explaining the increase in recovery time with higher stress voltages (zone 1 of Figure 7.6). However, at higher stress voltages of 4 V, the gate leakage current becomes higher [84], and the injected holes cross the AlGaN barrier by thermionic emission and tunneling (Figure 7.12), setting a potential counter compensation for the 2-DEG trapping, causing net reduced 2-DEG trapping explaining the relatively same or slightly shorter recovery times as in $V_G$_stress of 4 V (zone 2 of Figure 7.6). It is to be noted that, unlike 1.5/2 V $V_G$_stress instances, the 2-DEG density during 4 V stress, with increasing times, shows negligible change as the $I_D$ at $V_G$ 4 V is in the saturation regime and is not affected by the $V_{TH}$ shift, as explained earlier in Figure 7.2 b). As stress time increases beyond 50 ms (until 10 s), the trap density at the AlGaN/GaN interface, within the thermodynamic reach of 2-DEG, starts becoming saturated by trapped electrons, causing constant recovery times (region 2 of Figure 7.4). At a high-stress time of 100 s, the 2-DEG electrons, post-saturating the AlGaN/GaN interfaces, hop to the borderline region traps (2–3 nm from the interface) of AlGaN, leading to higher emission times and thus higher recovery times (as shown in region 3 of Figure 7.4). Thus, from the dynamic recovery trends and times, we could ascertain that the AlGaN/GaN interface is the predominant trapping site. This recovery time measurement could be extended to understand OFF-state stress-induced 2-DEG trapping, as well. Deep Level Transient Spectroscopy (DLTS) in depth profiling mode could be used to determine the trap's exact energy levels and concentration, as well as the trap's density[116]. With DLTS, alongside temperature-dependent Arrhenius analysis, the trap location ascertained by the proposed recovery time measurement technique could be verified, which could be a part of future work.

### 7.6 Conclusion

- We proposed a simple measurement technique to quantitatively measure the time taken by threshold voltage of normally off p-GaN AlGaN/GaN HEMTs to recover from a nominal operational gate stress induced instability.

- The proposed technique eliminates the requirement to do a full transfer characteristic sweep post stress, thereby eliminating the measurement induced instability effect colluding the exact recovery time measurement.
- The rate of recovery, recovery times extracted hold significance in empirically ascertaining the location of traps in the AlGaN barrier region causing $V_{TH}$ instability.
- The gate terminal of the HEMT is stressed for various time intervals from 500μs to 100s for a range of gate voltages from 1.5Vto 4V and the time taken for the drain current to recover to prestress levels measured at near threshold voltage (~ 1.1 $V_{TH}$) signifying the 2-DEG channel recovery (hence $V_{TH}$) is measured. With increasing gate stress voltages 2-DEG get trapped at relatively deeper trap energy level at the AlGaN/GaN interface requiring more emission time during the process of recovery mandating larger recovery times.
- At higher stress voltage like *4V* the Schottky gate leakage current is high enough enabling injected holes to cross the AlGaN barrier and counter compensate for the deeply trapped 2-DEG requiring relatively same recovery times as lower stress voltages where their gate leakage is negligibly small.
- With increasing time, the amount of 2-DEG trapped increase requiring more recovery time to de-trap and beyond certain time, saturation of the trap density happens causing the recovery time to plateau.

# 8. Conclusion and future work

## 8.1 Conclusion

Scaling of the logical transistors which offered significant performance improvements at reduced cost in the past decades, famously called Moore's law has hit the material limit and is becoming expensive. Therefore, to improve functionality for a given chip area, 'more than Moore' approach of monolithically integrating power management circuits, sensors, analog and RF circuits on chip or single package are actively pursued. The focus of our study is to enable efficient power management integrated circuits. Power semiconductor devices lie at the core of all the power management integrated circuits operating at voltage ranges from 5V to 1kV. Silicon based semiconductor devices traditionally have been used in these power management circuits and improvements in these devices have a significant impact on the size, efficiency, and power density of the systems. There has been a persistent increase in the demand for higher current, high voltage, high temperature, high efficiency power systems and silicon-based devices are approaching the theoretical limits. This had led to the exploration of wide bandgap semiconductor materials and Gallium Nitride is the most promising material set to challenge silicon in the 200V – 600V segment with characteristics of an ideal power switch.

- Gallium Nitride by virtue of its wide bandgap (3.4eV) has high breakdown field (3.3 MV/cm) and lower intrinsic carrier concentration. Thus, transistors based on Gallium Nitride can have smaller drift regions for high breakdown voltage and hence lower on state resistance in comparison with their silicon counterparts.

- High quality Gallium Nitride layers can be grown epitaxially by MOCVD (metal organic chemical vapor deposition) or MBE (molecular beam epitaxy) on various substrates including silicon. Despite the huge lattice mismatch, by continuous improvement of the AlN transition layers crack free GaN layers with least dislocation densities have been made possible. GaN on Si has been a significant breakthrough which made lateral GaN transistors CMOS compatible enabling monolithic integration

- GaN allows the formation of heterostructures using Aluminium to create $Al_xGa_{1-x}N$ layer sandwiched on top of the GaN layer. By varying the Aluminium mole fraction the band gap can be engineered.

- Gallium nitride by virtue of its non-centrosymmetric wurtzite hexagonal crystal lattice has an intrinsic spontaneous and piezoelectric polarisation potential which enables the formation of a high mobility (up to $2000cm^2/Vs$), high density (of the order of $10^{13}$ $cm^{-2}$) 2-dimensional electron gas (2-DEG) at the AlGaN/GaN heterojunction without any intentional doping.

- The high mobility 2-DEG formed by the AlGaN/GaN heterostructure grown on Si along with an ohmic source/drain and a Schottky gate forms normally ON high electron mobility transistor (HEMT). For the power electronic applications normally, off transistor is preferred for safety and reliable gate drive designs

- Of the many normally off architectures, p-GaN gate based AlGaN/GaN on Si is the leading structure for commercialisation. P-GaN gate is formed by Magnesium doping and magnesium tends to be incompletely ionised due to its high activation energy.

- Such normally off p-GaN gate AlGaN/GaN on Si has faced reliability issues such as the Dynamic on resistance, Kink effect and threshold voltage instability arising during the nominal operations.

- Reliability issues such as dynamic on resistance and kink effect have been investigated in detail in the past decade. In this thesis we investigate threshold voltage instability (or) dynamic $V_{TH}$ arising during the measurements (chapter 5), during the nominal ON state and OFF state operations (chapter 6) and propose a technique to measure the time taken for the threshold voltage to recovery post an instability event (Chapter 7).

- Sentaurus Technology Computer Aided Design (TCAD) models have been built (chapter 3, 4) to elucidate gate stack dynamic charge conditions and is used to

hypothesize and validate the physical mechanisms causing the threshold voltage instability

- Measurement induced $V_{TH}$ instability make $V_{TH}$ measurement challenging and the associated instability varies depending on the gate contact being Ohmic or Schottky. The measurement induced $V_{TH}$ instability, guidelines to mitigate them and the validated physical mechanisms causing them are summarised in Chapter 5. This is the first study to comprehensively address the above
  - In this chapter the impact of accumulated gate bias stress during standard transfer characteristic measurements ($I_D$-$V_G$) in a p-GaN AlGaN/GaN-on-Si normally off HEMT is quantitatively analysed and modelled.
  - Ton in pulsed $I_D$-$V_G$, Tstep in DC step $I_D$-$V_G$ are critical parameters that control the gate bias history experienced and need to be chosen such that the measurement of the drain current, $I_D$, happens within a stable time zone (identified via a drain current sampling technique) for obtaining a nominal stable $V_{TH}$.
  - It is suggested that the threshold voltage instability observed is attributed to electron trapping at the AlGaN/GaN interface. Furthermore, we show that the higher hole current injection from the gate terminal in ohmic gate HEMTs, compared to Schottky gates HEMTs, may counter compensate the electron trapping resulting in negligible or no threshold instability due to the stress of the threshold voltage measurement. These findings are validated by the TCAD modelling.

- Nominal operation induced $V_{TH}$ instability happens due to the ON-state gate stress and the OFF-state drain stress. The OFF state induced $V_{TH}$ instability is quantified, and the associated physical mechanisms are hypothesized and validated by TCAD for the first time as detailed in chapter 6
  - In this chapter it is showed by means of the experimental results that when the drain of the p-GaN HEMT is biased in the off-state the threshold voltage ($V_{TH}$) shows a linear positive $V_{TH}$ shift increase up to ~ 40%. This increase saturates at drain bias voltages above 50V.

- The positive $V_{TH}$ shift is attributed to the ionization of acceptor traps in the AlGaN region below the p-GaN gate, with the source of these trapping sites suggested to be the p-GaN gate out-diffused Mg dopant atoms.
- The ionization of the Mg acceptors due to high electric field during off-state bias and the removal of the generated holes from the AlGaN region through the gate contact creates the charge conditions for a positive $V_{TH}$ shift.
- The sharp decrease in the gate drain capacitance ($C_{GD}$) for $V_D < 50V$, the simulated gate edge electric field reaching its peak for a drain voltage bias $V_D \sim 50V$ and the positive threshold voltage shift observed for negative gate stress further validate the proposed model.

- Post $V_{TH}$ instability the time taken to recover is measured by a transient drain current measurement technique which doesn't include the measurement induced instability effects providing a realistic estimate on the time taken for the ON state stress induced instability to recover for the first time, as detailed in chapter 7
  - In this chapter a simple measurement technique to quantitatively measure the time taken by threshold voltage of normally off p-GaN AlGaN/GaN HEMTs to recover from a nominal operational gate stress induced instability is proposed.
  - The proposed technique eliminates the requirement to do a full transfer characteristic sweep post stress, thereby eliminating the measurement induced instability effect colluding the exact recovery time measurement.
  - The rate of recovery, recovery times extracted hold significance in empirically ascertaining the location of traps in the AlGaN barrier region causing $V_{TH}$ instability.
  - The gate terminal of the HEMT is stressed for various time intervals from 500μs to 100s for a range of gate voltages from 1.5Vto 4V and the time taken for the drain current to recover to prestress levels, measured at near threshold voltage ($\sim 1.1\, V_{TH}$) signifying the 2-DEG channel recovery (hence $V_{TH}$), is measured. With increasing gate stress voltages 2-DEG get trapped at relatively deeper trap energy level at the AlGaN/GaN interface requiring more emission time mandating larger recovery times for the recovery.

- At higher stress voltage like $4V$ the Schottky gate leakage current is high enough enabling injected holes to cross the AlGaN barrier and counter compensate for the deeply trapped 2-DEG requiring relatively same recovery times as lower stress voltages where their gate leakage is negligibly small.
- With increasing time, the amount of 2-DEG trapped increase requiring more recovery time to de-trap and beyond certain time, saturation of the trap density causes the recovery time to plateau.

In conclusion threshold voltage instability in normally OFF p-GaN gate AlGaN/GaN on Si HEMTs during measurements, nominal ON state, nominal OFF state stress are investigated, quantified by novel bench top measurements and respective comprehensive TCAD models validating the physical mechanisms have been developed. A novel measurement technique to measure the recovery time is also developed and the recovery process involved is physically understood.

## 8.2 Future work

This work can be continued in several possible directions

The first direction concerns the recovery time measurement technique post gate stress.

- The proposed hypothesis of 2- DEG trapping and detrapping at the AlGaN/GaN interface traps can be validated by the TCAD simulations and is a work in progress.
- These transient drain current measurements could be done at various temperatures to extract the trap energy levels at the AlGaN/GaN interface using Arrhenius plots of time constants at different temperatures and validated by DLTS.
- The $V_{TH}$ recovery time post drain stress by the proposed measurement technique would be of very high interest. A study investigating the threshold voltage recovery dynamics post drain stress could be measured using the proposed recovery time measurement technique. The drain terminal could be stressed at the appropriate voltage in the stress pulse and post stress the drain current can be sampled at $1.1V_{TH}$ to observe the recovery dynamics. Based on the recovery dynamics the physical trapping mechanisms could be ascertained and validated by the TCAD simulations.

The second direction could be concerned with development of a comprehensive TCAD model including all the trapping processes possible in the AlGaN barrier. In addition to the standard thermionic emission models, trap assisted tunnelling, phonon assisted tunnelling, direct tunnelling models could be incorporated. This TCAD model could be further developed into a simple SPICE model. The effect of $V_{TH}$ instability at the application level could also be potentially incorporated in the model.

The third direction would be to review, bench mark the various threshold voltage measurement and extraction techniques. For instance, the threshold voltage measurement bias conditions listed in the data sheet vary from manufacturer to manufacturer and the methodology of threshold voltage extraction (constant current technique and maximum transconductance technique) also varies. Doing an experimental analysis followed by simulation is planned.

The fourth direction could be concerned with developing a measurement technique which could potentially decouple trapping processes causing threshold voltage instability and dynamic Ron during OFF state stress. Finally novel GaN device structures which could potentially withstand the threshold voltage instability could be developed.

## List of publications

- **Karthick Murukesan,** L. Efthymiou, and F. Udrea, “On the challenges of reliable threshold voltage measurement in ohmic and schottky gate p-GaN HEMTs,” *IEEE J. Electron Devices Soc.*, vol. 9, no. July, pp. 831–838, 2021.

- **Karthick Murukesan,** L. Efthymiou, and F. Udrea, “Gate stress induced threshold voltage instability and its significance for reliable threshold voltage measurement in p-GaN HEMT,” in *2019 IEEE 7$^{th}$ Workshop on Wide Bandgap Power Devices and Applications, WiPDA 2019*, pp. 177–180.

- L. Efthymiou, **Karthick Murukesan**, G. Longobardi, F. Udrea, A. Shibib, and K. Terrill, “Understanding the Threshold Voltage Instability during OFF-State Stress in p-GaN HEMTs,” *IEEE Electron Device Lett.*, vol. 40, no. 8, pp. 1253–1256, Aug. 2019.

- **Karthick Murukesan** L. Efthymiou, and F. Udrea, “Physical understanding of normally OFF p-GaN/AlGaN/GaN HEMTs gate stack and review of $V_{TH}$ measurement techniques,” J Phys D Appl Phys, doi: 10.1088/1361-6463/ad8010

- **Karthick Murukesan,** and F. Udrea, “Threshold votlage recovery time Post $V_{TH}$ Instability in Normally-Off p-Gate GaN High Electron Mobility Transistors,” MDPI, Electronics. vol. 13, no. 20, doi: 10.3390/electronics13204118

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