Applied Physics Letters

Suppression of substrate coupling in GaN high electron mobility transistors (HEMTs) by hole injection from the p-GaN gate

Cite as: Appl. Phys. Lett. **115**, 203502 (2019); https://doi.org/10.1063/1.5121637
Submitted: 02 August 2019 . Accepted: 30 October 2019 . Published Online: 12 November 2019

D. Pagnano, G. Longobardi, F. Udrea, J. Sun, R. Garg, H. Kim, C. Ostermaier, M. Imam, and A. Charles

Applied Physics Letters ARTICLE scitation.org/journal/apl

Suppression of substrate coupling in GaN high electron mobility transistors (HEMTs) by hole injection from the p-GaN gate

Cite as: Appl. Phys. Lett. **115**, 203502 (2019); doi: 10.1063/1.5121637
Submitted: 2 August 2019 · Accepted: 30 October 2019 ·
Published Online: 12 November 2019

D. Pagnano,[1,a)] G. Longobardi,[1] F. Udrea,[1] J. Sun,[2] R. Garg,[2] H. Kim,[2] C. Ostermaier,[3] M. Imam,[2] and A. Charles[2]

AFFILIATIONS

[1]Engineering Department, University of Cambridge, Cambridge, CB2 1PZ, United Kingdom
[2]Infineon Technologies Americas Corp., El Segundo, California 90245, USA
[3]Infineon Technologies Austria AG, 9500 Villach, Austria

[a)]Electronic mail: dp515@cam.ac.uk

ABSTRACT

GaN-on-Si is a lateral technology and as such it allows the integration of high voltage High Electron Mobility Transistors and low voltage devices on the same chip, thus enabling the miniaturization and reduction of parasitic inductances. Due to the fact that integrated devices share a common substrate, the performance of one device can be significantly affected by the operation of another. The choice of the substrate bias is particularly important in the integrated half-bridge, a popular topology which includes a low- and a high-side device. A grounded substrate will cause vertical stress on the high-side device, while a floating substrate will couple with the high voltage, resulting in stress on the low-side device. This is highly problematic as the devices may fail to turn on or have a significantly increased R_{ON}. In this work, we carefully investigate the substrate coupling of a high-side and low-side device via backgating measurements. We demonstrate that the unwanted R_{ON} increase in the high side device could be suppressed by hole injection from the gate, if the gate is formed of a p-type material.

When compared to silicon solutions for power applications, GaN-based High Electron Mobility Transistors (HEMTs) have a smaller form factor, offer lower on-state losses, and are able to switch at higher frequencies. This makes them promising candidates for high-efficient power conversion systems.[1,2] Among all the available normally off technologies such as the GaN+Si cascode and MIS-gate FET, GaN-based devices with hole injection from p-GaN gates and drain have demonstrated excellent stability up to 600 V.[1] The final adoption of GaN HEMTs in the market is not only related to the dynamic R_{ON} but also to the possibility to monolithically integrate these transistors which would allow higher switching frequencies, reduced module size and parasitics, and therefore reduce cost. However, the monolithic integration of GaN high-voltage devices has been proven to be challenging mainly due to substrate coupling and the cross talk[3,4] between devices sharing the same substrate. Suppression of substrate coupling has been demonstrated for a GaN-on-SOI technology[5] by electrically connecting the source of trench-isolated devices to their respective substrates, so that no high vertical potential differences are applied to the devices. Vertical conduction mechanisms have also been shown to affect the vertical potential distribution within the buffer layers of GaN-on-Si transistors, having a significant impact on the behavior of the transistor under backgating experiments and on the device dynamic Ron.[6] In this paper, we investigate the substrate coupling issue via backgating measurements of both ungated and p-gate gated GaN-on-Si transistors. The experimental analysis demonstrates that hole injection from the p-GaN gate can suppress coupling and prevent detrimental effects on R_{ON}.

The experiments supporting our conclusions were performed on wafer-level small area structures, both gated and ungated. The gated structure has a p-GaN gate with a nonrecessed barrier, schematically shown in Fig. 1 (left). One should note that the nonrecessed barrier leads to a normally on behavior of the transistor, as shown in the transfer characteristics reported in Fig. 1 (right). The lateral device dimensions, L_{GS}/L_G/L_{GD}, are consistent with a 600 V device and the width, W_G, is 200 μm. The ungated structure (not shown) has the same L_{SD} and width.

Backgating measurements are routinely employed to characterize buffer traps[6] and substrate coupling.[3] In this measurement technique, the drain current is monitored while the substrate potential is either ramped or held at a given negative voltage. It is important to note that the applied potential difference between the channel and substrate of a

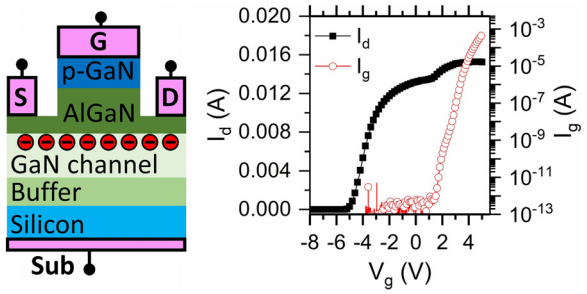

FIG. 1. (Left) Schematic cross sections of the normally on p-GaN HEMT with a nonrecessed AlGaN barrier. (Right) Transfer characteristics showing both the drain and gate current functions of the gate voltage.

nonintegrated high-voltage transistor subject to a backgating bias is equivalent to the one that a high-side device in an integrated half-bridge configuration would experience when the substrate is grounded, as schematically shown in Fig. 2. The impact of the substrate potential on the lateral drain current is due to two phenomena: (i) charge trapping in the buffer and (ii) capacitive coupling. Charge trapping is dependent on the capture/emission processes related to traps,[6,7] leakage paths, and transport mechanisms, both vertical and lateral, within the device.[6,8]

Capacitive coupling is observed if the vertical leakage is lower than the displacement current.[6] This is usually the case for a low substrate bias and fast ramps, depending on the particular device, so taking the tangent of the I_d-V_{sub} curve at low voltages and comparing it with the full I_d-V_{sub} curve, one can infer that there is positive charge accumulation if the actual I_d-V_{sub} lies above the tangent, negative vice versa, with the hysteresis giving an indication of the charge dynamics.[6]

According to this criterion, a backgating ramp measurement on the ungated structure (not shown) demonstrates some accumulation of positive charge. A similar behavior has been reported in Ref. 9, where an incremental increase in the normalized drain current is also demonstrated in the measurements and simulations during backgating ramps and is attributed to lateral and vertical hole leakage.

Both capacitive coupling and trapping associated with backgating cause a charge imbalance in the device that can negatively affect the 2DEG density. Here, we show that active hole injection suppresses the backgating effect up to $V_{sub} = -600$ V with relatively fast time constants, by neutralizing the negative space charge in the vicinity of the 2DEG channel.

Figure 3 shows the backgating ramp measurement performed on the normally on structure, represented in Fig. 1, at different gate voltages and with a ramp speed of 60 V/s. The first thing to note is that, depending on the gate bias, there is a given V_{sub}, $V_{sub\text{-}OFF}$, at which the channel is depleted, resulting in a zero drain current. For $V_g = 0$ V, $V_{sub\text{-}OFF}$ is approximately −200 V and it becomes more negative as the gate bias increases. This is true for all the gate biases considered in the experiment except $V_g = 2.5$ V, for which the drain current is constant throughout the experiment. One can note that for $V_g = 0$ V, the drain current decreases quasilinearly as V_{sub} gets more negative, with the device switching off at approximately $V_{sub} = -200$ V. For $V_g > 0$ V, the slope of the I_d-V_{sub} curve decreases with the increasing gate bias until $V_g = 0.75$ V where the curve becomes horizontal, implying no sensitivity to the substrate voltage. The curve for $V_g = 0.75$ V still shows a steeper decrease in the drain current for V_{sub} higher than −500 V, which is further delayed increasing the V_g.

Figure 4 shows the backgating bias experiment on the same structure and gives an insight into the time dependence of the substrate coupling suppression. In this set of measurements, the constant substrate and gate biases are applied at the beginning of the measurement, with the rise times negligible compared to the minimum measurement time resolution. The stress substrate voltage, V_{sub}, is −100 V for all the curves, while the gate voltage is increased between the measurements. The $V_g = 0$ V curve shows a minor, slow recovery which may be due to charge transport from the contacts or substrate.

As the gate voltage is increased, not only the drain current recovers to a higher value, as expected from the similar V_g dependence observed in the backgating ramp measurement, but the time constant of the increase becomes shorter. For $V_g = 1$ V, the time constant is in the 1–10 s range, while it decreases two orders of magnitude for $V_g = 1.5$ V, and it becomes smaller than our sampling resolution at $V_g = 2.5$ V. This implies that while a low gate voltage and hole injection are sufficient to suppress the substrate coupling, the effect may

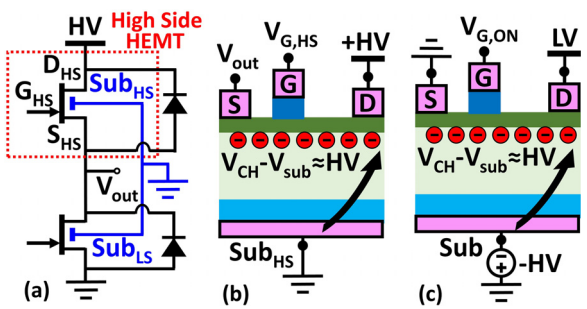

FIG. 2. (a) Half-bridge configuration highlighting the common grounded substrate connection (blue) and the high side device (red). (b) Schematic cross section of the high side HEMT, highlighting the potential difference between the substrate and channel, V_{CH}-V_{sub}. (c) Schematic cross section of a HEMT with the substrate bias applied as in the typical backgating measurement, showing a similar vertical potential difference as a high-side HEMT.

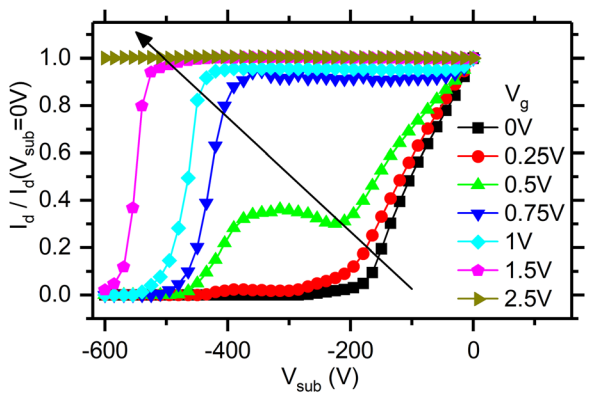

FIG. 3. Backgating ramp measurement on a normally on device at different gate voltages. The plot clearly shows the suppression of the backgating effect by hole injection from the p-gate.

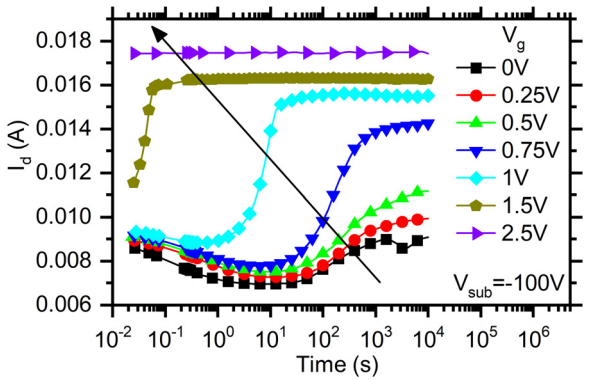

FIG. 4. Backgating bias measurement on a normally on device at different gate voltages, showing the time dependence of the hole injection as suppressing the substrate coupling.

not be fast enough in fast switching applications. The mechanism is dependent on the transport of holes, therefore, while the concept is valid for all carbon-doped lateral HEMTs, device epitaxy and design are tightly bound to the effect.

It needs to be emphasized that, while Fig. 1 shows a static current of approximately 5 μA at Vg = 2 V, the dynamic current during the transients is expected to be higher and dependent on the buffer traps which in turn depend on the epitaxial layer design and process, as demonstrated in Ref. 9 where the dynamic off-state current was investigated on comparable devices with a Ohmic gate and featuring gate hole injection.

Figure 5 shows the backgating bias measurement at $V_g = 1$ V and different substrate voltages. This set of measurements show that, while increasing the substrate voltage impacts the magnitude of the drain current, the recovery process is qualitatively equal. Finally, it is worth noting that while the experiments here were carried out on normally on p-GaN gate and ungated structures, the analysis and conclusions equally apply to normally off p-GaN gate HEMTs, where the drain current is measurable only if $V_g > V_{TH} \approx 1.2$ V. Simulations were carried out to further clarify the physical mechanism for the suppression of substrate coupling.

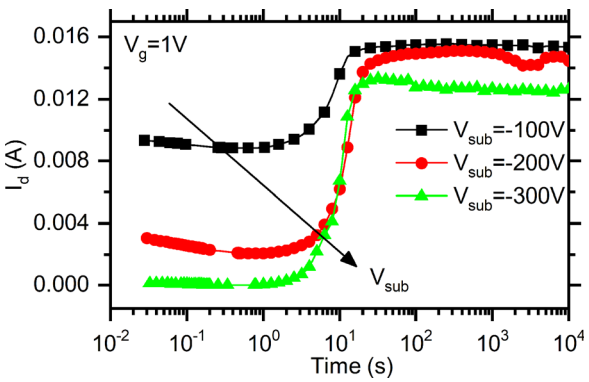

FIG. 5. Backgating bias measurement on a normally on device at different substrate voltages, showing a higher drain current decrease when the substrate bias voltage is increased, which does not affect the recovery.

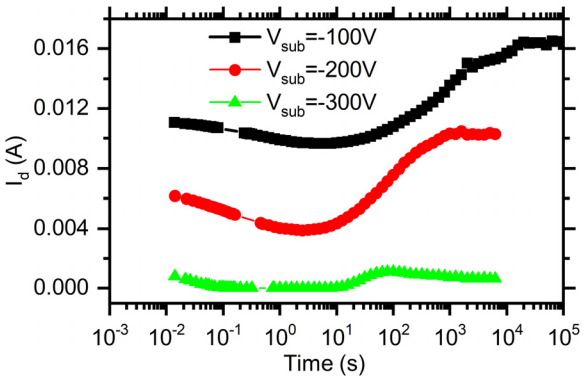

FIG. 6. Backgating bias measurement on an ungated structure, showing a slow, spontaneous recovery of the drain current.

To emphasize the importance of active hole injection, the backgating bias experiments, as in Figs. 4 and 5, were also performed on the ungated structure. The result, reported in Fig. 6, shows that the drain current is still able to recover from a substrate stress of $V_{sub} = -100$ V but the process takes a much longer time without hole injection from the p-GaN gate. Furthermore, the stress is only partially recovered for $V_{sub} = -200$ V and the recovery for $V_{sub} = -300$ V becomes negligible. Such a slow recovery process is coherent with the leakage of holes from the contacts, as in Ref. 9, or a thermal generation process.

Technology computer-aided design (TCAD) simulations of GaN HEMTs are challenging due to the complex buffer structure, trap and transport modeling, and uncertainty of the material parameters. We have discussed these issues in our previous studies[7,10] and here we adopt a similar TCAD approach. We model the buffer as a uniform GaN layer with hole traps, with trap parameters as in Ref. 7. Despite the modeling assumptions, it has been possible to qualitatively reproduce the time dependence of the backgating transients and provide valuable physical insight.

Figure 7 shows the simulated drain current transient at different gate voltages. The time dependency of the recovery is qualitatively similar to that given by the experiment, but in the simulations, the gate voltage necessary to achieve the substrate coupling suppression is

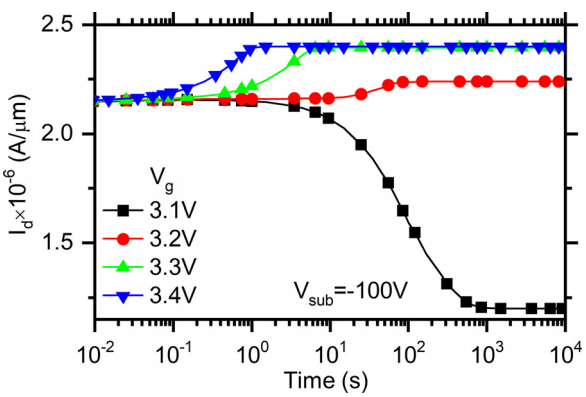

FIG. 7. TCAD simulation of the backgating bias experiment as in Fig. 5.

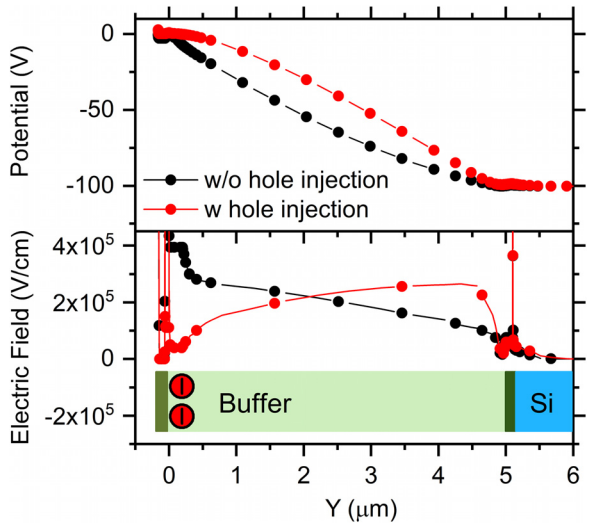

FIG. 8. Vertical potential and electric field distributions at different V_g, qualitatively showing the effect of hole injection.

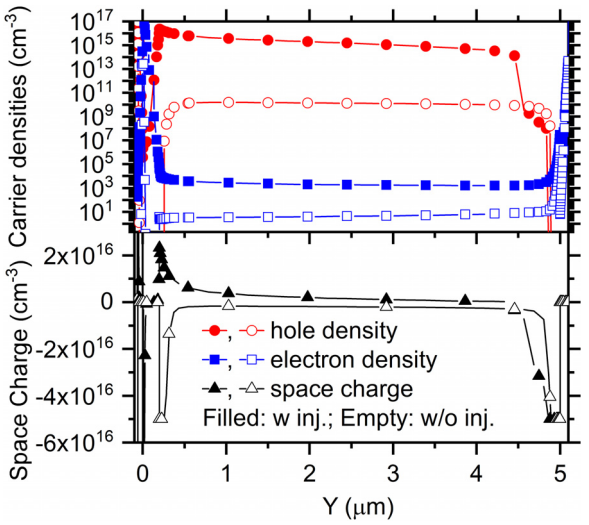

FIG. 9. Free carrier and space charge density distributions, with the hole injection ("w inj." in the figure) and without the hole injection ("w/o inj.").

shifted by approximately 3 V. The curve in Fig. 7 with a negligible hole injection shows a typical decrease in the drain current associated with backgating.[11] The lack of a quantitative matching between the experiment and simulation is due mainly to the difference in the experimental and simulated gate current and, in particular, the ideality of the AlGaN barrier and the p-GaN/2DEG diode, which do not allow sufficient hole injection at lower voltages.

Figure 8 shows a comparison of the simulated electric field and vertical potential distributions, for the cases with and without the hole injection. This data is extracted at 10^4 s from the simulations in Fig. 7. In the case of no hole injection, the electric field is high close to the 2DEG, so that a significant part of the potential drop is sustained by the junction it forms with the p-type buffer. As holes are injected, they neutralize the negative space charge and the electric field is significantly lowered in the vicinity of the channel, while the buffer sustains the entire potential drop. This shows a significant shift (flip) in the electric field from the channel side of the buffer toward the other side of the buffer layer. The effect resembles that of the Kirk effect in bipolar transistors, where the depletion region flips due to bipolar injection. In the real device, the exact potential distribution and the time constants associated with the recovery will depend on the epitaxial layer design, the processing, the presence of traps, and the different intentional and unintentional doping distributions and electrical properties.

For the same simulation outputs, Fig. 9 shows a comparison of the free career and space charge density distributions, for the cases with and without the hole injection. In the former case, it is clearly possible to note the increased free hole density in the buffer, together with a minor increase in the electron density. The increased hole density causes the accumulation of a positive space charge in the channel and the upper regions of the buffer, as opposed to the negative space exhibited by the case with no hole injection, leading to the electric field redistribution shown in Fig. 8.

In conclusion, the present study has been concerned with understanding the effect of the substrate voltage on the characteristics of lateral HEMTs. The study is relevant to high voltage ICs, where multiple devices are monolithically integrated. A typical half bridge case contains a low side and a high side power device. When the high side is operated in the on-state, a large substrate to surface voltage is present. It has been found that the hole injection from the p-GaN gate helps to minimize the drain current collapse when negative substrate voltages are applied. The hole injection is in turn dependent on the gate voltage and at high enough gate voltages, the substrate effect is virtually suppressed, possibly up to high frequencies. Finally, the higher the substrate voltage applied, the stronger the initial drain current decrease, but this does not affect the recovery and its time constant. Finally, we have found that the holes of the gate current flip the electric field from the region close to the channel to the other side of the buffer in a similar way to a Kirk effect in bipolar transistors. This leads to a stable operation of the 2DEG in the high side device without a degradation in R_{ON} due to the substrate effect.

REFERENCES

[1]K. J. Chen, O. Häberlen, A. Lidow, C. l Tsai, T. Ueda, Y. Uemoto, and Y. Wu, "GaN-on-Si power technology: Devices and applications," IEEE Trans. Electron Devices **64**(3), 779–795 (2017).
[2]G. Longobardi, "GaN for power devices: Benefits, applications, and normally-off technologies," in *International Semiconductor Conference (CAS)* (IEEE, 2017), pp. 11–18.
[3]B. Weiss, R. Reiner, V. Polyakov, P. Waltereit, R. Quay, O. Ambacher, and D. Maksimović, "Substrate biasing effects in a high-voltage, monolithically-integrated half-bridge GaN-Chip," in *IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)* (IEEE, 2017), pp. 265–272.
[4]Q. Jiang, Z. Tang, C. Zhou, S. Yang, and K. J. Chen, "Substrate-coupled cross-talk effects on an AlGaN/GaN-on-Si smart power IC platform," IEEE Trans. Electron Devices **61**(11), 3808–3813 (2014).
[5]X. Li, M. Van Hove, Z. Ming, K. Geens, W. Guo, S. You, S. Stoffels *et al.*, "Suppression of the backgating effect of enhancement-mode p-GaN HEMTs on 200-mm GaN-on-SOI for monolithic integration," IEEE Electron Device Lett. **39**(7), 999–1002 (2018).
[6]M. J. Uren, S. Karboyan, I. Chatterjee, A. Pooth, P. Moens, A. Banerjee, and M. Kuball, ""Leaky dielectric" model for the suppression of dynamic Ron in

carbon-doped AlGaN/GaN HEMTs," IEEE Trans. Electron Devices **64**(7), 2826–2834 (2017).
[7]D. Pagnano, G. Longobardi, F. Udrea, J. Sun, M. Imam, R. Garg, H. Kim, and A. Charles, "On the impact of substrate electron injection on dynamic Ron in GaN-on-Si HEMTs," Microelectron. Reliab. **88**, 610–614 (2018).
[8]C. Koller, G. Pobegen, C. Ostermaier, and D. Pogany, "Evidence of defect band in carbon-doped GaN controlling leakage current and trapping dynamics," in *IEEE International Electron Devices Meeting (IEDM)* (IEEE, 2017), pp. 33–34.
[9]P. Moens, M. J. Uren, A. Banerjee, M. Meneghini, B. Padmanabhan, W. Jeon, S. Karboyan *et al.*, "Negative dynamic Ron in AlGaN/GaN power devices," in *29th International Symposium on Power Semiconductor Devices and IC's (ISPSD)* (IEEE, 2017), pp. 97–100.
[10]G. Longobardi, S. Yang, D. Pagnano, G. Camuso, F. Udrea, J. Sun, R. Garg, M. Imam, and A. Charles, "On the vertical leakage of GaN-on-Si lateral transistors and the effect of emission and trap-to-trap-tunneling through the AIN/Si barrier," in *29th International Symposium on Power Semiconductor Devices and IC's (ISPSD)* (IEEE, 2017), pp. 227–230.
[11]A. Chini, G. Meneghesso, M. Meneghini, F. Fantini, G. Verzellesi, A. Patti, and F. Iucolano, "Experimental and numerical analysis of hole emission process from carbon-related traps in GaN buffer layers," IEEE Trans. Electron Devices **63**(9), 3473–3478 (2016).