Carbon 247 (2026) 121089

Contents lists available at ScienceDirect

Carbon

journal homepage: www.elsevier.com/locate/carbon

Research paper

# Diamond-based non-volatile memory

Martin Kah [a,b,c,*], Cédric Masante [a,b], Nicolas Rouger [b], Fabrice Donatini [a], Juliette Letellier [d], Franz A. Koeck [e], Robert J. Nemanich [e], Julien Pernot [a,f]

[a] Univ. Grenoble Alpes, CNRS, Grenoble INP, Institut Néel, 38000 Grenoble, France
[b] LAPLACE, Université de Toulouse, CNRS, 31000 Toulouse, France
[c] Cambridge University, Department of Engineering, Electrical Engineering Division, Cambridge, UK
[d] DIAMFAB, 25 avenue des Martyrs, 38000 Grenoble, France
[e] Arizona State University, Tempe, AZ 85281, USA
[f] Institut Universitaire de France (IUF), 75231 Paris, France

ARTICLE INFO

*Keywords:*
Diamond
Junction field effect transistor
Non-volatile memory

ABSTRACT

The digital age has brought unprecedented challenges in data storage, with exponential growth in data generation outpacing traditional storage solutions in capacity, speed, and reliability. Long-term data preservation is particularly concerning, as current technologies like semiconductor drives and hard disk drives struggle with data longevity beyond a few decades. Optoelectronic memories show promise among emerging storage-class memory technologies, but they face trade-offs between information retention time and fatigue cycles due to material limitations. Diamond, with its exceptional physical properties, especially its ultra-wide bandgap, emerges as a strong candidate for developing non-volatile memories capable of retaining information over extremely long periods. This paper explores the fundamental aspects and fabrication methods of diamond non-volatile memories, focusing on the information storage mechanisms and unique properties of the ultra-deep nitrogen donor in diamond, as well as the associated junction field effect transistor. The study describes the physical concept of the memory effect and the transistor structure, details the fabrication and properties of the samples, and addresses key challenges in creating efficient devices. These findings establish diamond as a viable material for ultra-stable memory applications and provide key insights into its long-term performance.

## 1. Introduction

The storage of digital data presents significant challenges in the modern era of information technology. As the volume of data generated and consumed continues to grow exponentially, traditional storage solutions struggle to keep pace with the demands for capacity, speed, and reliability [1,2]. More important, the longevity of data storage is a critical concern, as many existing technologies are susceptible to degradation over time, leading to potential data loss. Current memory technologies, whether semiconductor drives based on silicon technology or Hard Disks Drives (HDD) based on magnetic materials, enable data to be stored non-volatility for years, even decades, but hardly any longer.

This limitation raises questions about our ability to store sensitive digital data for periods extending beyond several centuries. Among emerging storage-class memory technologies, optoelectronic memories has demonstrated promising performances [3–12]. However it still faces challenges especially, trade-off between information retention time and fatigue cycles, or suffers from high programming voltage asides with long programming time.

These limitations, common to most storage-class memory, stem from material properties. As a novel material for this application, diamond has garnered attention due to its exceptional physical properties, particularly its ultra-wide bandgap, positioning it as a strong candidate for the development of non-volatile memories capable of retaining information over extremely long periods. Such advanced storage solutions aim to ensure long-term data retention with minimal degradation, preserving valuable information over extended timescales. Some of us recently described an innovative method for manufacturing diamond non-volatile memory (NVM) devices [13], called non volatile photoswitch (NVPS). This technology is based on the use of an ultra-deep nitrogen donors in diamond crystal lattice. This ultra-deep dopant can be manipulated optically to store information in a non-volatile manner in a diamond device, offering a robust solution for ultra-long-term data storage. Promising proof-of-concept diamond transistors based on n-type doping, including JFETs [14] and inversion-mode MOSFETs

* Corresponding author at: Cambridge University, Department of Engineering, Electrical Engineering Division, Cambridge, UK.
*E-mail address:* mryk2@cam.ac.uk (M. Kah).

https://doi.org/10.1016/j.carbon.2025.121089
Received 18 July 2025; Received in revised form 3 November 2025; Accepted 19 November 2025
Available online 20 November 2025

[15], have recently emerged, highlighting the growing maturity of diamond electronics; yet, achieving precise doping control remains a critical requirement to transition from experimental demonstrations to fully competitive technologies. Whether this level of maturity is now sufficient to enable the fabrication of ultra-long-term memory devices remains a central consideration. This paper delves into the fundamental aspects and fabrication methods of diamond non-volatile memories, with a particular focus on the information storage mechanisms and unique properties of the ultra-deep nitrogen donor in diamond, as well as the associated junction field effect transistor (JFET).

The paper will be structured as follows. The first part introduces the physical concept of the memory effect, and examines the underlying theory of dopant ionization. An ideal JFET architecture is then proposed, highlighting the balance between theoretical optimization and practical fabrication constraints. The second part will detail the fabrication of proof-of-concept prototypes and presents their structural, chemical, optical and electrical properties. Particular attention will be brought on the key challenges in fabricating efficient devices and propose solutions to overcome them, supported by initial experimental results. Performances of the fabricated memory, including writing, reading, and storage times is also discussed, while the performance of the initial demonstrators will be compared with model predictions. Finally, the paper will conclude with perspectives on the requirements and challenges to be addressed in the coming years to establish diamond as an ultra-long-term memory solution.

## 2. Diamond-based non-volatile memory concept

### 2.1. Working principle

In its initial theoretical form, the memory device is conceived to operate through the ON and OFF states of a diamond-based JFET. The gate electrode on the n-side relies on deep donors, whose ionization energy lies sufficiently deep within the bandgap to ensure a very low ionization rate, while the channel incorporates shallow acceptors to enable and ensure conduction between the drain and source electrodes, as illustrated in Fig. 1(a). In the ON state, the JFET permits current to flow through the channel, representing a stored bit of information or one of the two possible logical state of the memory (“1”). Conversely, in the OFF state, current flow is blocked, providing the second logical state (“0”), or the absence of a stored bit. The key feature of this non-volatile device is its ability to maintain deep donor atoms in a non-equilibrium state, provided no external disturbances, such as elevated temperature, light, or ionizing radiation, supply enough energy to ionize the electron-donating impurities. It enables the storage of the JFET’s ON or OFF state for a duration that is effectively governed by the kinetic limitation of the space charge region (SCR) extension within the p-channel. The evolution of the SCR, marked by the variations of the pn-junction’s band alignment, is in turn, limited by the ionization timescale of the n-type dopants which, controls the local charge equilibrium, as detailled in [13]. Providing that donors lies sufficiently deep inside the bandgap, a pseudo-equilibrium state is established in which the ionization timescale can theoretically approach infinity relative to a human lifetime. This makes the controllable state of the JFET stable and reliable without the need for an external bias. Ideally, the ionization energy of the deep donors should be sufficiently high to be fully decoupled from thermal energy while remaining susceptible to modulation by energetic radiation such as illumination. Light excitation of the deep donors and bias voltage will be needed to write the bit state, but only electrical measurement will be needed to read the bit state, as shown in Fig. 1. The structure proposed in this work distinguishes itself from conventional charge-trapping memories (CTM) by directly utilizing the semiconductor dopants as a non-volatile gate’s charge traps, without the need for a dedicated charge trap layer or a multilayer gate stack [16,17]. In this architecture, the stored information is inherently coupled to the semiconductor, while the read/write operations are triggered by an external light source, analogously to EPROM-type memories.

To ensure clear distinction between the ON (“1”) and OFF (“0”) states, the ON/OFF drain current ratio of the JFET must be optimized, while preserving the architectural and geometrical conditions required for the memory effect. To achieve a conductive bulk p-channel with an arbitrary resistivity around 1 mΩ cm$^2$, thereby minimizing electrical loss in the ON state, a high carrier density $p$ is required. Choices are very constrained for diamond as the shallowest and most efficient acceptor known up to date is boron, with an ionization energy of $E_A$ = 380 meV. However, this value remains high compared to more conventional wide-bandgap semiconductors such as SiC or GaN, so p-type diamond suffers from a low ionization rate at room temperature. As an example, in the optimized trade-off adopted for the prototypes presented in this work, the p-channel doping level was targeted at $N_A \simeq 2\times10^{17}$ cm$^{-3}$. This yields an ionization rate below 1%, but still preserves a high hole mobility of $\mu_h \simeq 1400$ cm$^2$/V s at room temperature [18]. This structural choice, made at the expense of ionization efficiency, was taken to favour high conductivity while maintaining a low threshold gate voltage [19].

Regarding the n-side region, deep donor is needed to ensure no free electron at temperatures ranging between 300 K and 500 K. This property can be achieved with a very deep donor like nitrogen in diamond with $E_D$ = 1.7 eV. With substitutional nitrogen ionization energy even higher than silicon bandgap, it is insured that almost no free electron remain available in the n-gate without radiative excitation, such as light. Thus, the JFET is in a read-only state because the n-side is completely insulating without light excitation and the space-charge region of the JFET cannot be modulated by a bias voltage. The efficient way to create free electrons is to use one-photon processes on electrons bound to substitutional nitrogen with $h\nu > E_D$ = 1.7 eV. The write and read modes can be achieved by illuminating the device with appropriate light, as summarized in Fig. 1 (b.). Given these considerations, it is evident that a trade-off will be necessary between the non-volatile stability of the read-only state in the dark, where a deeper donor results in a longer-preserved state, and the switching frequency of the device, which is limited by the RC constant of the circuit composed of the capacitance of the JFET gate in the OFF state (reverse-biased pn junction) and the resistance of the nitrogen-doped region under illumination. The balance between retention time and switching speed is initially governed by the ionization energy of deep donors, but can be adjusted and improved through careful transistor design. Although such designs must account for the current fabrication limits of diamond devices, it remains essential to first outline the theoretical models that form the basis of this memory concept before discussing prototype results.

### 2.2. The stability of the non volatile state: emission time constant of deep dopants in diamond

To further elaborate on the concept of nearly infinite retention time, theoretically proposed in this work, it is essential to discuss the physical models underlying this innovative approach to semiconductor-based memory. In the present concept, information retention, encoded through the JFET states, is governed by the time constant required for the pn-junction space-charge region to return to electro-thermal equilibrium. In the absence of external energy input (e.g., illumination), deep nitrogen donors in diamond establish a stable and reliable pseudo-equilibrium state. While, at thermal equilibrium, the fraction of ionized impurities in semiconductors is well described by the steady-state Gibbs distribution [20], the out-of-equilibrium ionization ratio must be treated as time dependent, and is therefore better described by a generalized Shockley–Read–Hall (SRH) model [21] under transient conditions. Since the memory states are governed by electron capture at, or emission from, deep donor levels (capture in the ON state, and emission in the OFF state, both in non-volatile configuration without

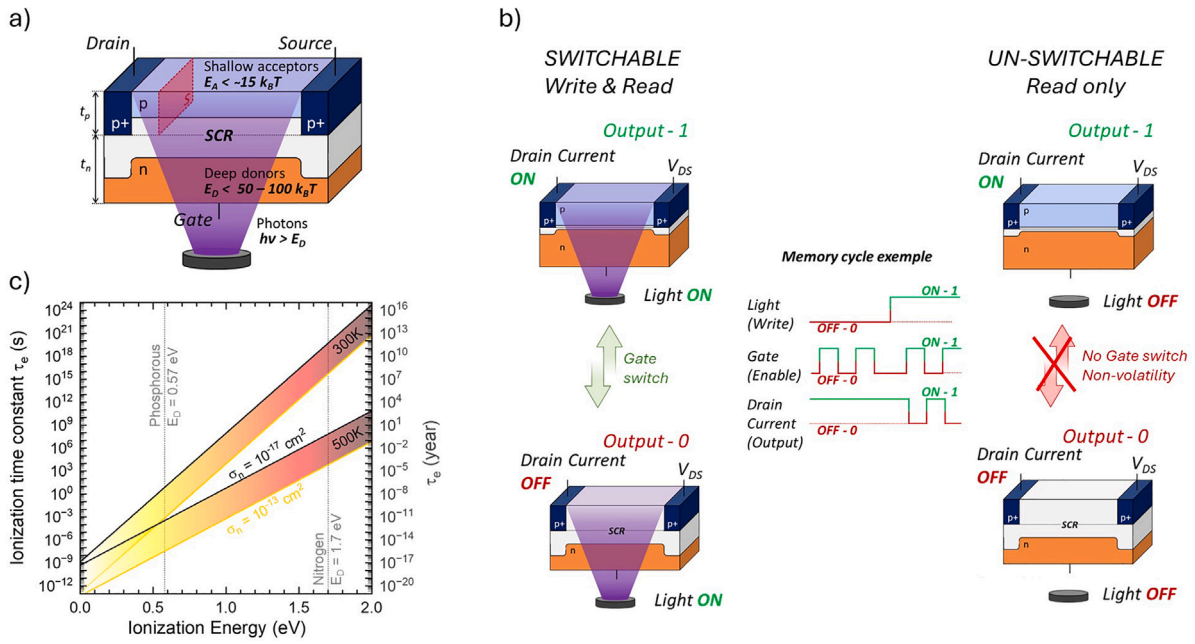


**Fig. 1.** (a) Ideal NVPS cross sectional representation with emphasis done on dopants ionization energies $E_A$ for p-type and $E_D$ for n-type. (b) Diagram of a NVPS-based memory cycle enlightening the inverting logic of the transistor, where the device is active, or controllable, during illumination and frozen, or inactive, without it. (c) Ionization time constant $\tau_e$ as function of n-dopants ionization energy $E_D$, for impurity electron capture cross-section comprised between $10^{-13}$ and $10^{-17}$ cm$^2$, at 300 K and 500 K.

illumination) the mean retention time of the memory can be reduced to the ionization time constant $\tau_n$, expressed as:

$$\tau_n = \frac{1}{e_n + n \times c_n} \tag{1}$$

where $e_n$ and $c_n$ are respectively the emission and capture rate of electrons, given by:

$$e_n = \frac{\sigma_n v_{th} N_c}{g_n} \exp\left(\frac{E_D}{k_B T}\right)$$
$$c_n = v_{th} \times \sigma_n \tag{2}$$

Here, $\sigma_n$ is the electron capture cross-section of the deep donor, $v_{th}$ is the thermal velocity of electrons, $N_c$ is the effective density of states in the conduction band, $g_n$ is the degeneracy factor of the deep donors, $E_D$ is the energy level of the deep donor referenced from the bottom of the conduction band as the origin of energy, $k_B$ is the Boltzmann constant, and $T$ is the temperature. The ionization time constant $\tau_n$ describes the charge/discharge relaxation time of electrons associated with a donor level at energy $E_D$, and reach a maximum value inside depletion region, where $n = 0$. In this particular case, modelled by the non-volatile OFF state or when the memory is in the dark and the p-channel fully depleted (output "0"), the ionization time constant of nitrogen atoms in the n-side depletion region is solely equivalent to the inverse of the emission time constant. A rough evaluation of $\tau_n$ can be performed by assuming the capture cross section corresponding to an attractive centre of a positively charged donor, $\sigma_n \simeq 10^{-15}$ cm$^2$, and that $N_c \simeq 1.2 \times 10^{20}$ cm$^{-3}$ and $v_{th} \simeq 1.25 \times 10^7$ cm/s at 300 K, with $E_D = 1.7$ eV and $g_n = \frac{1}{2}$. One obtains $\tau_n \simeq 38$ billion of years, as shown in Fig. 1 (c.). It is important to note that, even when the JFET is forced into a pseudo-equilibrium state, charge neutrality remains a fundamental physical rule that needs to be satisfied at each sides of the pn-junction. Because the contraction of the SCR is dynamically limited on the n-side of the junction, the p-channel remains fully depleted due to charge conservation. The transient behaviour of the transistor, and consequently the change in the memory writing state, is governed by the deep donor impurities confined within the gate electrode. In the absence of illumination, any variation of the gate voltage (e.g. any attempt to modify the memory state through a write operation) on a timescale shorter than $\tau_n$ is kinetically limited, and the memory state cannot be set. Under the approximation of a single active defect, this read-only state is theoretically expected to persist for billions of years at room temperature, effectively "eternal" on a human timescale, but is reduced at elevated temperatures, down to couple weeks at 500 K. The assumption of a single active defect is convenient for establishing the theoretical proof of concept of the memory operation, but it is extremely difficult to realize in practical devices. If electrically active defects with ionization energies lower than that of nitrogen are present in the crystal, their contribution must be accounted in the SRH model proposed herein-above and they can introduce shorter ionization time constant. Therefore, achieving efficient prototypes requires particular attention to crystal quality, along with stringent control of doping in the diamond layers.

Based on this assessment, we can readily estimate that it is feasible to design micro-metric or even nano-metric components with nitrogen doping ranges that are easily achievable using conventional diamond plasma enhanced chemical vapour deposition techniques (between $10^{15}$ and $\times 10^{19}$ cm$^{-3}$). These components will be highly robust over time and will therefore be capable of maintaining the state of the bit for effectively infinite periods. The deep nitrogen donor is a perfect candidate for a reliable and stable non-volatile state. However, while the retention time of the memory state is envisioned to be very long-term, this must not come at the expense of the writing speed. To ensure the feasibility of high-frequency switching while preserving the longevity of the non-volatile OFF state, trade-offs at the device-parameter level must be anticipated. This work therefore aims to provide a comprehensive study of the physical mechanisms underlying memory operation, together with optimization strategies for the prototypes fabricated within this framework.

### 2.3. Write switching frequency: System RC time constant

Access to the memory state through channel conductance measurements is permanent, and the read operation is not expected to constrain the cycle speed, which is primarily determined by the characterization method. In contrast, speed limitations are anticipated during the

write operation, which requires constant illumination. The maximum switching frequency of the JFET can be modelled by the resistance–capacitance (RC) time constant of the circuit, composed of the depleted region capacitance in the OFF state (reverse-biased pn junction) and the internal gate resistance under illumination. This resistance is expected to be particularly high, as it arises from the incompletely ionized nitrogen-doped layer itself, in series with the resistance of the metal/n-doped diamond contact. Due to the high contribution of the n-gate contacting resistance to the RC time constant, a detailed analysis over this parameter is conducted in the supporting information. Details of the modelling and prototype characterization have already been reported elsewhere [22] by some of us, but it is important to emphasize here that the switching speed of the transistor is limited by the incomplete ionization of the n-layer, which is also the origin of its memory properties. A trade-off therefore exists between retention time and cycle speed, ultimately governed by the characteristics of the deep donors, in particular their ionization energy. To give a rough first order approximation of the time needed to turn-ON or -OFF the transistor, the capacitance is modelled through the SCR of an asymmetric *pn* junction, with an highly n-doped region and p-channel with a lower doping level. Considering a doping level in the range of $N_D \simeq 10^{19}$ cm$^{-3}$ for the n-side and $N_A \simeq 2 \times 10^{17}$ cm$^{-3}$ for the p-side, the capacitance lies around C = 50 nF/cm$^2$ for a fully depleted p-layer thickness of 400 nm. In this case the p-channel is assumed thin, to guarantee a threshold voltage of the transistor ranging between 20 and 30 V. The internal gate resistance is determined by the dimensions of the path that electrons must travel, considering that the mobility will be roughly constant regardless of the density of electrons excited by light, and mainly, the number of carriers photo-excited, $\Delta n$. This quantity depends on the optical capture cross-section of the nitrogen atoms, which in turn depends on the excitation wavelength and the photon flux. To illustrate a feasible case, let us assume that the n-layer is formed from a thick substrate of 500 μm, leading to an internal gate resistance in the GΩ–TΩ range, still considering a doping level of $N_D \simeq 10^{19}$ cm$^{-3}$. In this configuration, the resulting switching speed lies between one second and one millisecond, which may be limiting for real-time logic.

While thinning the n-layer may appear attractive for achieving faster switching in prototypes, reducing its thickness too much can lead to a significant decrease in light collection efficiency. For a fixed wavelength and photon flux, insufficient thickness prevents the absorption of all, or at least the majority of, photons crossing the layer, thereby reducing the photo-generated carrier density $\Delta n$ and ultimately slowing the switching speed of the memory. To overcome this limitation, an alternative is to use a shallower n-type dopant for the gate layer or to explore co-doping strategies [23]. Phosphorus is particularly suitable in this regard, as it exhibits an ionization energy of $E_D = 0.57$ eV, which can enhance photoelectron generation in the n-type gate layer for a fixed illumination energy, which induces lowering of the internal gate resistance. This improves NVPS dynamics, albeit at the cost of a reduced ionization time constant, as illustrated in Fig. 1c. Even though the trade-off between switching speed and retention time is expected, quantifying the relative influence of each parameter would require either comprehensive TCAD modelling or advanced prototypes.

## 3. From concept to prototypes

Two diamond-based memory architectures, deliberately designed to emphasize either retention time or switching speed, have been fabricated and experimentally characterized. The first prototype employs a thick n-gate layer doped with deep n-type donors (nitrogen), a configuration intended to maximize retention time but inherently limiting the device's switching speed. In contrast, the second prototype aimed to incorporate a thinner n-gate layer with shallower dopants, reducing the overall gate resistance and enabling faster switching, albeit at an expected cost of reduced data retention capability. The two designs used are schematized in Fig. 2, and are development of the proof of concept depicted in Fig. 1.

Five samples were fabricated, three with design #1 and two with design #2, with the characteristics affiliated to each design and samples, summarized in Table 1. Each design consisting of a stack based on a (001)-oriented, 500 μm-thick Ib HPHT diamond substrate provided by Sumitomo Electric. In design #1, a boron-doped p-type epitaxial layer was deposited, while in design #2, the deposition of a phosphorus-doped epitaxial layer was firstly attempted, prior to the boron-doped epitaxial layer, each grown using microwave plasma-assisted chemical vapour deposition (MPCVD). The boron-doped p-type and p++ layers were grown by Diamfab, while the phosphorus-doped layer was fabricated at Arizona State University using the process described elsewhere [24,25].

The doping level and thickness of the p-channel were targeted at $N_A = 2 \times 10^{17}$ cm$^{-3}$ and 400 nm, respectively. To ensure efficient ohmic contacts for source and drain electrodes, a selectively localized, heavily boron-doped ($N_A \simeq 10^{21}$ cm$^{-3}$) p++ type diamond layer was deposited on the p-layer, followed by the evaporation of Ti/Pt/Au (30/30/100 nm) metal contacts. In both samples, the lightly boron-doped layer serves as the JFET channel, while the gate contact configuration differs between the two designs, as illustrated in the cross-sections of Fig. 2. In design #1, the Ib HPHT substrate acts as the n-body of the pn junction and the metallic gate electrode is positioned on the backside of the sample. In design #2, the gate metallic contact is placed on the etched front side of the sample, where phosphorus-doped layer has been tentatively incorporated between the p-channel and the Ib HPHT substrate. It must be emphasized that in the case of Design #1, the back-side gate contact is made using silver paint coating and sticking on an insulating alumina plate. Identical protocols have been used on samples exhibiting design #2 to ensure similar light reflection from the reflective silver paint on the substrate backside, increasing in each samples the light interaction in the n-layer. Experimental transistor output characteristics, namely drain current as function of drain to source voltage are shown in Fig. 2 for samples REF0 and PS2, demonstrating good transistor operation for at least two samples with the two different design compared in this study.

Samples were characterized using a custom-built probe station equipped with vacuum and temperature control, as well as an illumination system for the device under test. While illumination source is provided by a Newport 1000 W, UV enhanced, Xenon Lamp, monochromatic light is obtained thanks to an Horiba iHR 320 monochromator allowing a light band-with through the whole setup between 200 nm (6.2 eV) and 2000 nm (0.62 eV). Light is then focused inside a probe station thanks to wavelength adapted optical fibres, and monochromatic signals are always filtered before injection to avoid second diffraction order transmission. It is important to notice that illumination energy dependent spectra have been acquired in separated windows and reconstructed afterwards to optimize filters cascade and optical fibre transmittance range. The I(V) measurements were performed using a Keithley 2612B, which features two source measurement units (SMUs) and is connected via triaxial cables. The Keithley 2612B has a current detection limit of $10^{-12}$ A and a maximum voltage range of ±200 V. Home-made program have been developed to trigger current detection at specific time interval, while maintaining constant drain to source voltage over a defined duration (cf Fig. 4). The probe station is equipped with a binocular microscope and micromanipulators, allowing precise probe positioning using piezoelectric motors. Sample temperature is controlled with a Linkam cooling system, operating between 77 and 600 K, and a Pt100 resistance probe placed on the sample holder for temperature verification.

## 4. Results and discussions

The performance of the JFET architecture critically depends on precise doping control and active layer thickness, as the formation

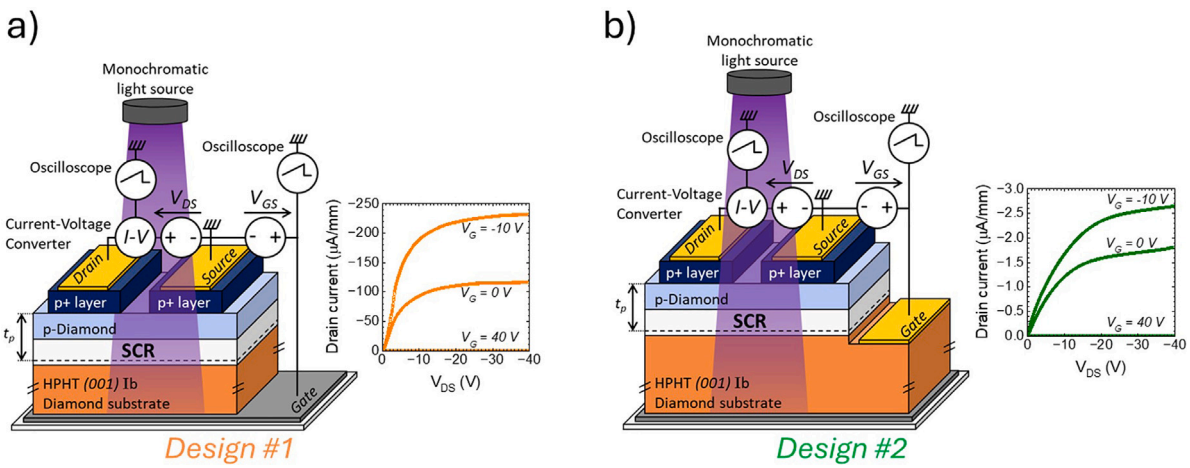


**Fig. 2.** (a) Schematic cross section of design #1, with the gate contact fabricated on the back-side of the Ib substrate and measured drain current density as function of drain to source voltage $V_{DS}$ for different gate bias, at room temperature and under white light illumination of 11 mW/cm$^2$ (REF0 sample). (b) Schematic cross section of design #2, with the gate contact fabricated on the front-side of the n-layer and measured output characteristics under the same conditions (PS2 sample). Measurement setup, including oscilloscopes used for transient analysis are also enlighten. The illumination was centred on the sample, covering the entire surface over an area of 19.6 mm$^2$.

**Table 1**
Samples design and targeted layer properties.

| sample name | Design | p-channel | | n-gate | | Gate contact |
|---|---|---|---|---|---|---|
| | | $N_A$ (cm$^{-3}$) | $t_{ch}$ (μm) | $N_D$ (cm$^{-3}$) | $t_G$ (μm) | |
| REF0<br>NS3<br>NS4 | #1 | $2 \times 10^{17}$ | 0.4 | $[N] = 10^{19}$ | 500 | Back-side of the substrate |
| PS1<br>PS2 | #2 | | | $[P] = 10^{19}$ | 0.5 | Mesa-etched front-side of the n-epilayer |

of ultra-sharp and stable pn junctions is essential for efficient transistor operation. While p-type diamond doping via chemical vapour deposition (CVD) benefits from decades of development and exhibits well-established control, variations at the component scale or from samples to samples still needs to be considered as reproducibility hindering factor. To provide a detailed analysis of the two fabricated devices, structural and chemical characterizations were carried out prior to opto-electrical measurements.

### 4.1. Chemical and optical analysis

In order to estimate punctual and volumic defects or p-layer doping level, 4 K sub-band-gap cathodoluminescence (CL) spectra [26] have been recorded on each fabricated samples at various positions as reported in Fig. 3 f. Unfortunately, no clear evidence of substitutional phosphorus incorporation into the (001)-oriented CVD layer could be given through excitonic spectra analysis above the detection limit of $N_D = 2{\times}10^{15}$ cm$^{-3}$ [27]. This result was confirmed afterwards by SIMS (Fig. 3 e.), where phosphorous incorporation is too low compared to the target and no evidence of efficient incorporation into substitutional position could be done by CL. Spectra acquired either in the boron-doped or phosphorous-doped layer of sample referenced PS2, made upon Design #2 are reported in Fig. 3 b and defect signature is discussed in supporting information.

Comparison of CL, and SIMS results demonstrate that none of the four samples met their initial design specifications, as depicted in Fig. 3 e. and f. Measured layer properties of the fabricated samples are summarized in Table 2. The boron-doped p-channels have decent channel doping levels with a deviation mean around 50% of their targeted value but are way thinner than expected. These results, are also in good agreement with further electrical characterizations that showed insulating properties for PS1 (Design #2), NS3 and NS4 (Design #1), p-channels. Failure analyses have also been conducted for these samples but unfortunately, neither oxide encapsulation or n-side polarization, permit to retrieve even a slight conductance or modulation of conductance. For PS1 sample, it could be due to the presence of a compensated semi-insulating layer on the surface of the channel, killing the conduction (see Fig. 3 e.). While on NS3 and NS4 samples, the thinner than expected p-channel could be fully depleted by the uncontrolled positive surface potential caused by the oxygen termination. Most importantly, an unexpected absence of phosphorous concentration has been observed whereas heavily doping was targeted for PS1 and PS2. Only small rise in this concentration tends to appear near the topside of the substrate, attesting of the attempts to incorporate phosphorous. However the concentration is still below boron's one and way below nitrogen's, but can still justify the defect signature observed in CL measurements in the low energy range. However, the unsuccessful attempt to produce a phosphorus-doped layer is in no way responsible for the problems of thickness on p-channels, as confirmed by the results for NS3 and NS4 samples.

It is important to acknowledge that, from CL and SIMS measurements performed on PS2 sample, phosphorus have been incorporated in the (001)-oriented diamond lattice, but no clear activation evidence could be reported, whereas for PS1 sample, even the incorporation could not be proven. This limitation may weaken the expected contribution of shallower dopants on gate conductivity hence, improvement in switching speed and, highlights the difficulty of achieving efficient phosphorus doping in (001)-oriented diamond. Phosphorus incorporation is sensitive to surface kinetics as step-flow growth on vicinal (off-cut) substrates promotes incorporation at step edges and can favour substitutional incorporation, whereas nominally on-axis (zero-misorientation) surfaces tend to nucleate by two-dimensional island or

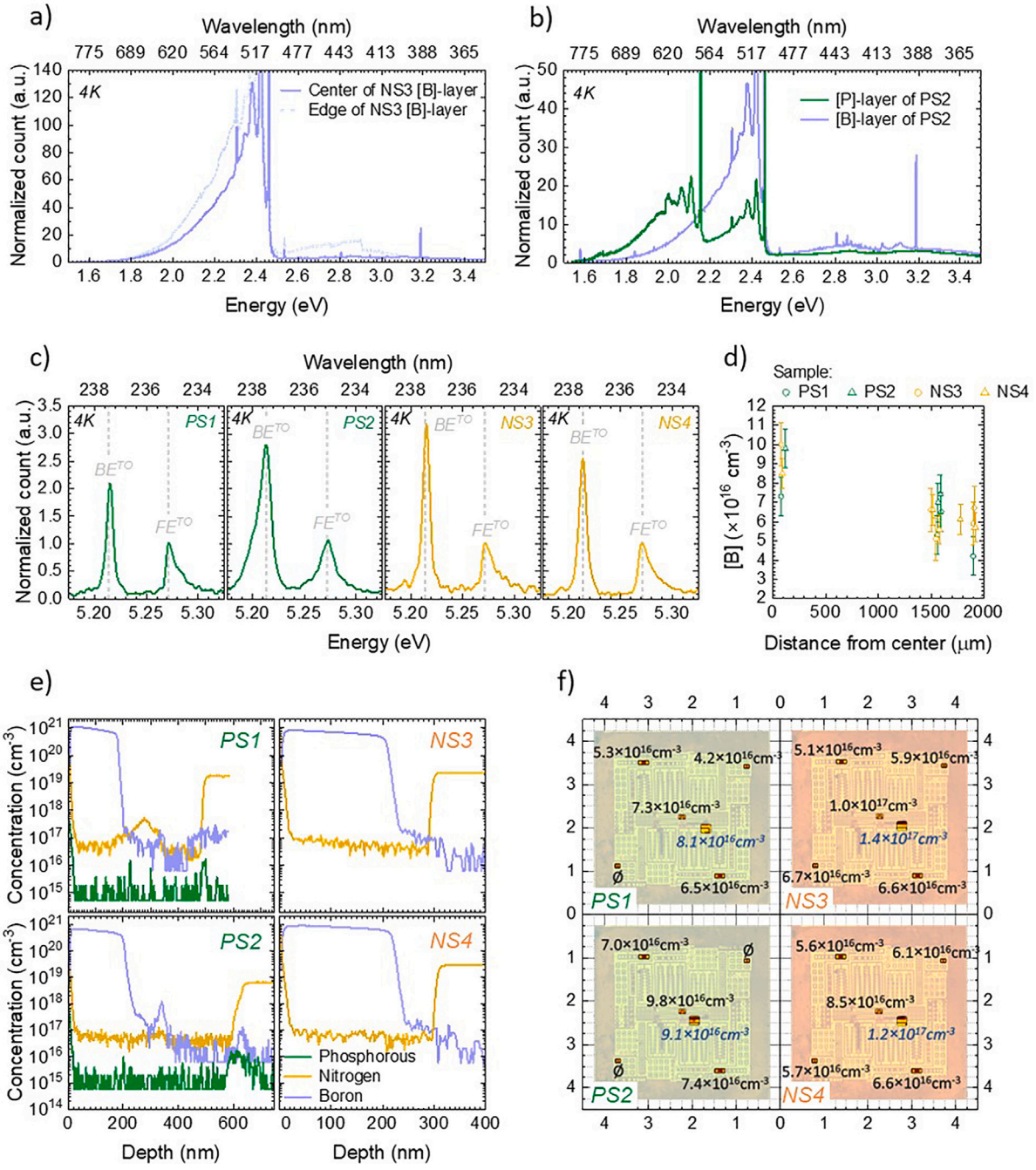


**Fig. 3.** (a) 4K CL spectrum recorded on the boron-doped layer of each sample. Spectra recorded compare defects band-emissions between the centre and the edge of sample NS3. (b) Similar comparison made between spectra obtained on the attempted phosphorous-doped layer and the boron doped layer of the same sample, PS2. (c) Excitonic-emission region recorded at the centre of each samples, used to extract doping levels, through peaks excitonic peak ratio [28]. Using this method, doping level extracted at different distances from the respective samples centre are enlightened in (d). SIMS spectra, (e), are displayed for each sample studied with analysis performed at the area marked in blue in (f). The later, (f) summarize the doping level extracted from CL (black) and SIMS (blue) as function of their recording position on the fabricated sample (background picture). ∅ symbol has been used to specify absence of measurement due to SEM-induced charging effect that caused loss of CL signals. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

multilayer growth, which can trap dopants in non-substitutional sites or at extended defects [29]. The discrepancies observed between the targeted and measured phosphorus doping levels, as well as the layer thicknesses for both the boron-doped p-channel and phosphorus-doped n-gate, may originate from the use of a nearly on-axis substrate. This hypothesis could be verified by characterizing the substrate misorientation angle using AFM or high-resolution X-ray diffraction. Further optimization of the growth process to favour substitutional phosphorus incorporation as a function of substrate misorientation is therefore a promising route to enhance functionalization yield. Additional strategies, such as ion implantation followed by thermal activation [30] or co-doping approaches involving shallow donors such as lithium [31], have been proposed to enhance the concentration of electrically active donors. Although in both cases, the resulting layer quality, being lower than in-situ doping during homo-epitaxial CVD growth, might limit these alternative solutions suitability for ultra-long term data retention.

**Table 2**
Measured layer properties for each fabricated sample.

| Sample Name | Design | p-contact Doping ($\times 10^{20}$ cm$^{-3}$) | $t_{p+}$ (nm) | p-channel Doping ($\times 10^{17}$ cm$^{-3}$) | $t_{ch}$ (nm) | n-substrate Doping ($\times 10^{19}$ cm$^{-3}$) |
|---|---|---|---|---|---|---|
| REF0 | | not measured | | $N_A - N_D = 2.3$ ($\pm 0.5$) [32] | 0.4 [32] | not measured |
| NS3 | #1 | $[B]_{SIMS} \approx 6.8$ ($\pm 1$) | 220 ($\pm 10$) | $[B]_{SIMS} \approx 1.4$ ($\pm 0.6$) | 70 ($\pm 10$) | $[N]_{SIMS} \approx 2.3$ |
| NS4 | | $[B]_{SIMS} \approx 7.8$ ($\pm 1$) | 230 ($\pm 10$) | $[B]_{SIMS} \approx 1.4$ ($\pm 0.5$) | 70 ($\pm 10$) | $[N]_{SIMS} \approx 2.9$ |
| PS1 | #2 | $[B]_{SIMS} \approx 8.9$ ($\pm 1.4$) | 190 ($\pm 10$) | $[B]_{SIMS} \approx 0.8$ ($\pm 0.5$) | 300 ($\pm 10$) | $[N]_{SIMS} \approx 1.8$ |
| PS2 | | $[B]_{SIMS} \approx 5.6$ ($\pm 0.9$) | 220 ($\pm 20$) | $[B]_{SIMS} \approx 1.2$ ($\pm 1$) | 400 ($\pm 20$) | $[N]_{SIMS} \approx 0.8$ |

Overall, the present prototype should be regarded as an initial step towards demonstrating faster-switching diamond-based memories. Even if phosphorus incorporation has not been unequivocally demonstrated, the inclusion of a metallic gate electrode on the top side of the sample, allowing for shorter channel to gate distances than the first case, crossing the thick Ib substrate (500 μm), reduces the overall gate internal resistance [22].

As shown by the statistics presented in this work, any standard deviation in fabrication processes or non-uniformity of active layer growth can hinder the fabrication of diamond-based NVPS and furthermore, diamond-based electronic or quantum devices. Attention is still mandatory on this part as high-quality layer are required for devices miniaturization, up to the deterministic scale, but also homogeneity is of importance, especially regarding the development of transistor to large-scale area. While the precise control of boron incorporation during diamond growth has considerably improved over the years [33], the mastery of n-type diamond growth still lags behind, despite its high relevance for a wide range of applications, spanning from quantum technologies to power electronics, including emerging domains highlighted in this work. For electrical transient and transistors characterization, analysis were performed on samples PS2 and REF0, the only one that proved transistors operation as shown in Fig. 2 through drain current vs. drain to source voltage characteristic. However, samples PS1, NS3 and NS4 are still functional for the electrical characterization of contacts made on n-gate layers, thanks to the p++ layer high quality (see Supporting information).

The limited functionalization yield and reproducibility observed in our prototypes (two successful devices out of five) are primarily attributed to process and material variability, including differences in surface state, substrate misorientation and crystal quality. Subsequent parameters that could drastically impact growth rate and dopants incorporation, as for equivalent growth recipes, variations have been measured between the different samples. Improving the functionalization yield will likely require transferring the fabrication process to the wafer scale, which would promote better process standardization and reproducibility. Additional gains can be achieved by performing growth in clean-room integrated environments equipped with in-situ diagnostic capabilities, allowing tighter control over growth parameters. Furthermore, correlating electrical performance with spatially resolved characterization techniques such as AFM, XRD, and XPS will help identify yield-limiting factors and guide process optimizations to enhance reproducibility and overall device performance.

### 4.2. Electro-optical characterization

Previous results on the same structure [22] already demonstrated that the gate electrode placement on the front surface of the n-layer, enabled the turn-OFF and turn-ON times to be reduced under constant illumination, as enlightened in Fig. 4 a. Unfortunately, first attempt to introduce a phosphorous-doped layer between the Ib substrate and the p-channel, was unsuccessful as confirmed by secondary ion mass spectroscopy (Fig. 3 e.). Subsequently, no switching frequency improvement from lower ionization energy dopants could have been experimentally demonstrated yet, even if the theory proposed [22], predicts that ionization dynamic is favoured for lower energy traps. Discrepancy between turn-ON and turn-OFF times is induced by variations of gate internal resistance during the transient imposed to the transistors. It subsists a trade-off, when the SCR capacitance is decreasing, the n-type layer resistance is increasing, assumption is made that this leads to shorter turning-ON time. In terms of ideal conception, it is demonstrated here that even if the gate contact is realized as in Design #2, including higher metallic (non-transparent) surface covering, the switching efficiency is improved compared to Design #1, stating that lowering of the gate internal resistance is more important over the light collection efficiency in the structure for fast switching application.

An important parameter over non-volatility for memories, is their longevity, or the time during which the device is able to maintain its logical state, considering every control power is removed or the memory is frozen in its read only state. In this case, as displayed in Fig. 4 b. to d., the time during which the JFET is able to maintain its read state under high temperature, when every control power (optical and electrical) is removed from the structure, except for the drain voltage which implies a drain current density $I_D$ in the conduction channel, witness of the transistor state. The stability testing protocol involves turning-OFF the transistors with light and gate voltage, then freezing their state by removing light, and shortly after remove the gate voltage. Stability proof is demonstrated by turning the light back on, hence setting the NVPS in their writing mode after two hours at high-temperature, and two days at room temperature, to prove non-loosed controllability of the transistor. At room temperature, the two designs have maintained a non-volatile OFF state for at least two days, limited up to now by the measurement setup. The non-volatility of NVPS devices, ideally driven by the photo-ionization of substitutional nitrogen in the Ib substrate (as sufficient phosphorous incorporation could not be proven), is adversely affected by temperature increases, with high temperatures (larger than 250 °C) leading to the loss of the non-volatile OFF state. At 100 °C, both designs maintained the OFF state with drain current densities reduced by three orders of magnitude compared to the ON state for at least 2.5 h. However, Design #1 exhibited higher leakage currents compared to Design #2. At 150 °C, device robustness significantly degraded, with the OFF state lost within approximately 7 min after removing the gate voltage and light. This degradation is attributed to increased deep levels ionization in the n-type layer, reducing stability. Furthermore, the observed longevity loss compared to the ideal theoretical value of a few days at 200 °C (see Fig. 1 c) could be indicative of the presence of electrically active defects shallower than the nitrogen dopants in the n-layer for both designs, although this remains to be experimentally verified. Confirming the nature and origin of such defects would require further analysis, involving transient spectroscopy technics.

### 4.3. Prospects for future diamond-based memory

As perspectives, although the NVPS building blocks introduced in this work have demonstrated enhanced efficiency for memory applications, the long-term development of innovative electro-optical control in diamond-based JFETs still faces several challenges. It is becoming increasingly evident that quality and reproducibility are critical factors in advancing competitive diamond-based devices. In the absence of a technological breakthrough enabling vertical transistors, the immediate priority remains the fabrication of homogeneous and reproducible devices. In this study, functionalization yield was achieved in only two

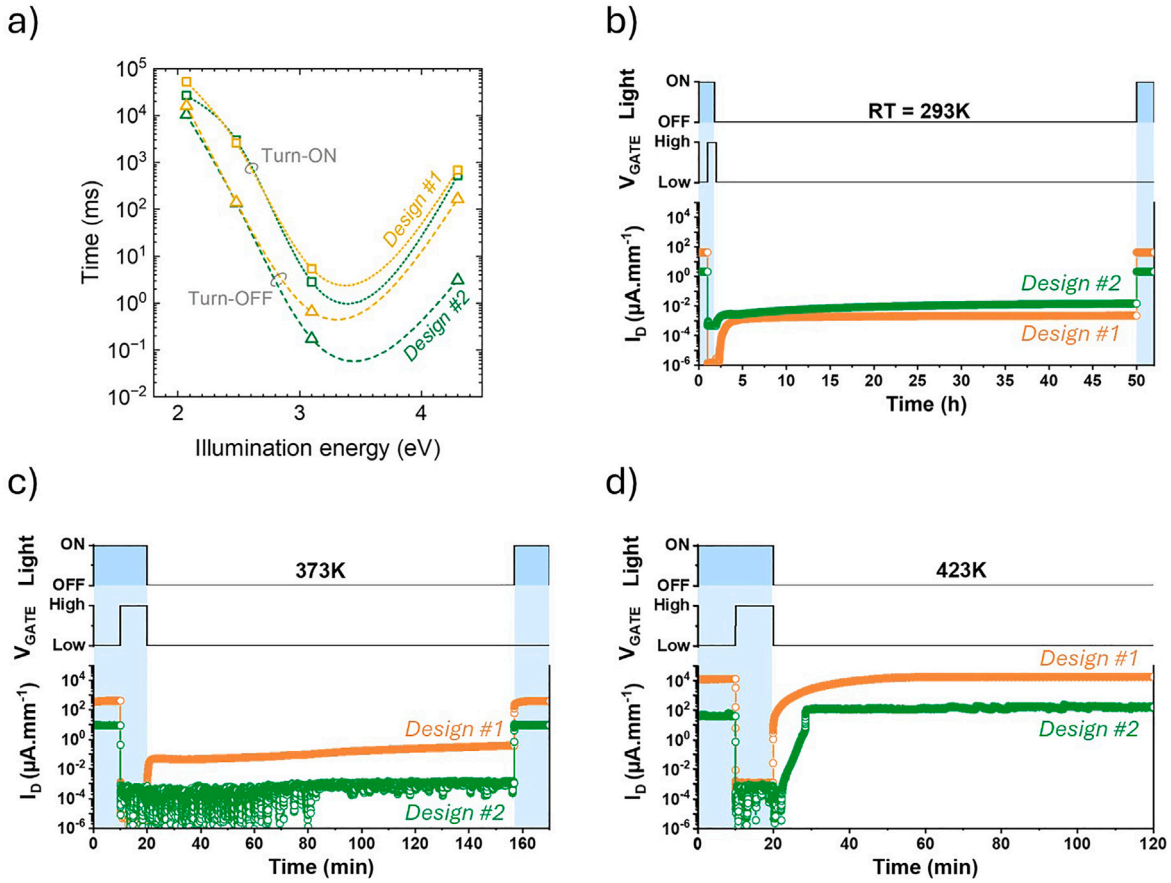


**Fig. 4.** (a) Time to turn-OFF (cubic dots) or -ON (triangle dots) the NVPS, namely write the memory state, as function of the constant illumination energy for the two designs compared within this study and the two functional samples, REF0 (orange) and PS2 (green). Illumination energy has been lowered, starting from the highest energy displayed, while light power density have been maintained constant through optical densities at 0.1 mW/mm$^2$. Dashed and dotted lines are guide for the eyes using cubic spline interpolation. (b) RT drain current density $I_D$ as function of time for REF0 sample and PS2, after a closing cycle (gate voltage high under illumination to close the transistor, then removing of illumination and shortly after, turning the gate voltage to low) of the transistor and removing of optical and electrostatic control. Time range is adapted to demonstrate the longevity of the freeze and non-volatile OFF state that have previously been set by applying a gate voltage under illumination (active state). Drain to source voltage ($V_{DS}$) is maintained constant at −30 V. (c) 373 K (100 °C) and (d), 423 K (150 °C) drain current density (at ($V_{DS}$ = −30 V)) as function of time for REF0 and PS2 sample, after the same closing routine of the transistor and removing of optical and electrostatic control. Gate voltage is switched between 0 V (Low) and +60 V (High) while light ON refers to a white light illumination of 11 mW/mm$^2$. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

out of five fabricated devices, with a notable standard deviation in doping levels compared to the target values, as well as variations in the active layer thickness for both p-type and n-type diamond films. While these deviations affect device-to-device reproducibility, they do not compromise the main conclusions of this work regarding the concept and relative performance of the two memory architectures. Reducing the highly resistive n-gate cross-section, and thereby lowering the internal gate resistance, is effective in increasing the memory writing speed. However, achieving a similar reduction through the use of lower activation energy dopants remains to be experimentally demonstrated, even though theoretical predictions suggest it would improve fast writing operation. Phosphorus doping could greatly reduce gate contact resistance, acknowledging that transparent contacts are feasible, though achieving it on (001) diamond remains highly challenging. Developing wire-bondable yet transparent contacts, either for drain and source, or gate electrodes, would be highly beneficial, providing low access resistivity while preserving efficient light absorption in the n-type layer.

To position our prototypes within the landscape of emerging NVM technologies, we report in Fig. 5 high operation speed amongst opto-electrical memories, while maintaining similar measured retention time. Electrical NVMs, particularly those relying on 2D materials, already demonstrate an excellent balance between speed and retention, combined with high endurance and low operating voltages. However, less mature opto-electrical approaches offer a unique opportunity: by leveraging optical control, they could not only bridge the gap with advanced photonic technologies but also establish a platform that connects the electronic and photonic domains for future memory applications. Among electro-optic memory concepts, the diamond-based NVMs proposed here show measured retention characteristics comparable with other reported devices and, according to JEDEC standard retention-time evaluation protocols [57,58], could meet the 10-year data-retention benchmark typically used for non-volatile memories. Future efforts towards competitive prototypes will concentrate on implementing tighter process control throughout fabrication steps, to increase conformity with targeted parameters and achieve robust device operation, while increasing devices operation speed.

The relatively high illumination power density and large gate bias amplitudes in the current prototypes indicate that the programming energy per bit remains substantial compared to electrical NVM market requirements [59], but is in good agreement with programming voltages (40–90 V) reported for other opto-electrical NVM [7,10,34–36]. Looking forward, several strategies could be employed to reduce the operating power while preserving the non-volatile characteristics. Miniaturizing the gate and channel areas would lower the total gate capacitance, directly reducing the voltage and energy required for

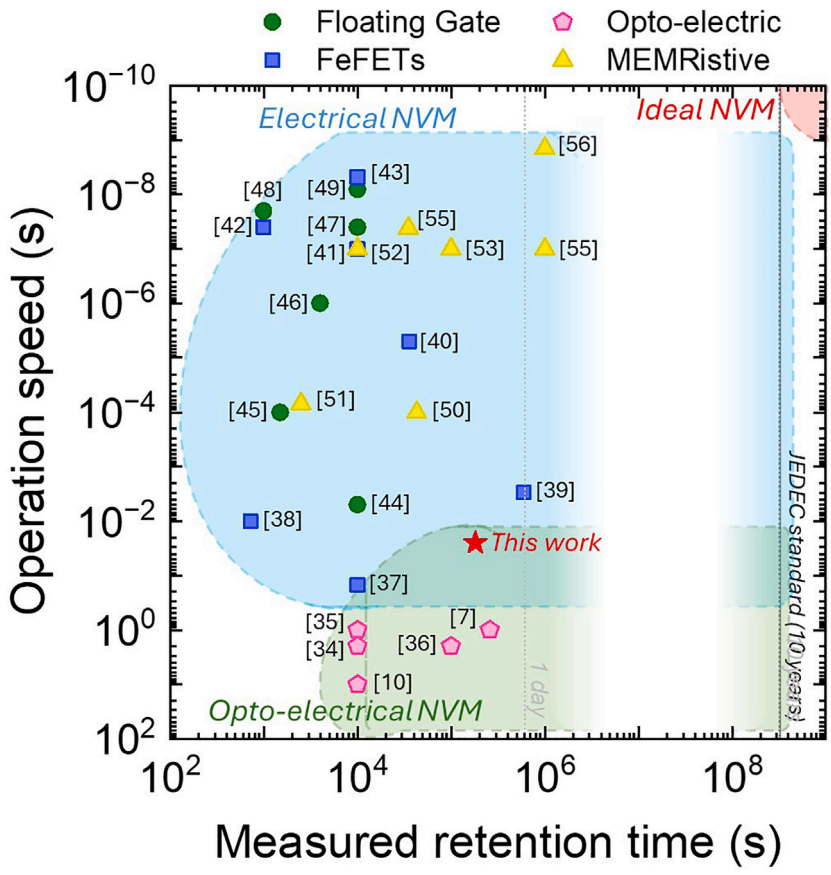


**Fig. 5.** Comparison of operation speed, namely a programming/reading cycle, and measured retention time for either, electrical only, or opto-electrical NVM reported in literature. [7,10,34–56]. While most devices reported comply with the JEDEC 10-year retention standard [57,58], the retention values shown here correspond to the measured durations obtained under comparable experimental conditions, as this approach avoids assumptions inherent to long-term extrapolation and enables a fairer comparison across differently driven prototypes.

switching. Integration of optical coupling elements, such as micro-lenses or waveguides, could concentrate light onto the active region, enhancing photon absorption efficiency and lowering the required illumination intensity. Electrical optimization, including improved contact design to reduce gate resistance and leakage, would allow lower bias voltages without compromising switching performance. However, such scaling introduces trade-offs that must be carefully considered. Reducing device dimensions may reduce retention time due to a smaller charge storage volume but at the benefits of increased switching speed through lowered RC time constants. It must be accounted that this solution automatically imply an increase in fabrication complexity, hence variability sources caused by variability in the current processes. Systematic exploration of these trade-off will be essential for progressing from current proof-of-concept devices to low-power, high-density memory arrays, and could guide the design of next-generation diamond-based non-volatile memories.

To achieve high light power density, a micrometer-scale light-emitting diode (LED) could be directly bonded to the n-diamond surface, maximizing light absorption in the n-layer. This approach would enhance the writing-state dynamics without compromising the non-volatile OFF state. While gallium nitride planar LEDs present an intriguing possibility, their integration remains unrealistic at this stage due to the significant technological advancements required before their practical implementation, even though diamond and GaN bonding have made remarkable progress recently [60–62]. However, transparent encapsulation oxide, as well as LED contacts bonding is expected to be challenging. From another perspective, the fabrication of memory arrays incorporating multiple independent NVPS units in a matrix-like configuration represents a promising advancement for bioelectronic applications. Due to its inherent biocompatibility, diamond-based NVPS arrays are well-suited for biomedical implants, making them one of the first implantable logic electronic devices based on diamond [63]. When integrated with a diamond sensor, these arrays could enable the development of a low-power diamond time-division multiplexer. In such a system, each row of a solution-gated field-effect diamond transistor array could be read sequentially, similar to the operation of a CCD sensor. This approach would significantly reduce the number of electrical connections, addressing the challenge of excessive wiring that increases the size and complexity of biomedical implants [64]. Additionally, the non-volatile memory are highly advantageous for minimizing power consumption, a critical factor for chronic implant applications.

## 5. Conclusion

In this work, we demonstrated that ultra-deep donors in diamond, specifically nitrogen dopants, can significantly enhance the retention characteristics of diamond-based non-volatile photo-switches, supporting their potential use as high-endurance memory elements. Experimental attempts in the fabrication of these photo-switches confirms the viability of this innovative concept, where optically controlled charge-imbalance can be imposed to diamond pn-junctions with remarkable longevity, owing to the unique energy range brought by ultra-wide bandgap diamond semiconductor.

A central finding of our study is that the non-volatility of the photo-switches is governed by the dynamic ionization time constant of the donors within the n-gate layer. Through theoretical modelling, we show that, in the limit of a defect-free diamond matrix, retention times

could exceed human timescales, opening the path towards ultra-long-term, solid-state memory devices operating at room temperature and beyond. To support these predictions, we fabricated and characterized prototype samples that exhibited robust OFF-state retention for over two days at room temperature. These experimental results represent a significant step forward, offering one of the first physical validations of charge storage in diamond via deep donor charge state manipulation. However, our experimental results also highlight current limitations in material quality. At elevated temperatures, retention performance was restricted to the scale of hours or minutes, supposedly due to the presence of electron-emitting impurities. While these behaviours suggest the involvement of such localized defects, it remains unclear whether point defects or extended structural defects, such as dislocations, are the dominant contributors to the degradation of memory retention in our samples. Further investigations, such as transient spectroscopy, would be necessary to clarify these mechanisms, though this technique is still under development and not yet fully adapted for diamond systems.

Moreover, reproducibility studies conducted within the scope of this work reveal that both intra-sample and inter-batch variability remain significant hurdles, currently limiting the performance consistency of the fabricated devices. These challenges indicate that, while the underlying concept is both sound and promising, achieving its full potential will require continued efforts in the optimization of diamond growth and doping processes. The prototypes fabricated in this work remain limited by material quality and fabrication constraints, and the “ultra-long-term” retention time is therefore presented as a future objective to be progressively approached.

## CRediT authorship contribution statement

**Martin Kah:** Writing – review & editing, Writing – original draft, Methodology, Investigation, Formal analysis, Data curation. **Cédric Masante:** Validation, Methodology, Investigation, Formal analysis, Conceptualization. **Nicolas Rouger:** Validation, Supervision, Resources, Project administration, Methodology, Investigation, Funding acquisition, Conceptualization. **Fabrice Donatini:** Supervision, Software, Resources, Methodology, Investigation, Formal analysis, Data curation. **Juliette Letellier:** Validation, Resources, Methodology, Investigation, Formal analysis. **Franz A. Koeck:** Validation, Resources. **Robert J. Nemanich:** Validation, Resources, Funding acquisition. **Julien Pernot:** Visualization, Validation, Supervision, Resources, Project administration, Methodology, Investigation, Funding acquisition, Conceptualization.

## Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests: Julien PERNOT, Nicolas ROUGER, Juliette LETELLIER reports financial support, administrative support, equipment, drugs, or supplies, and travel were provided by French National Research Agency. Franz KOECK, Robert NEMANICH reports financial support and equipment, drugs, or supplies were provided by Energy Frontier Research Centers. If there are other authors, they declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

## Acknowledgements

The authors are grateful to Nanofab for clean-room facilities, Khaled Driche (Diamfab), David Eon, Etienne Bustarret and Gwénolé Jacopin (Institut Néel) for fruitful discussions. This work was supported by French National Research Agency through LSDMOSFET (Large Scale Diamond MOSFET) under Project ANR-21-CE50-0036 AAPG-2021 PRCE. The work of Franz A. Koeck and Robert J. Nemanich was supported by the Ultra Materials for a Resilient, Smart Electricity Grid (ULTRA), the Energy Frontier Research Center (EFRC) funded by U.S. Department of Energy, Office of Science, Basic Energy Sciences under Award DESC0021230.

## Appendix A. Supplementary data

Supplementary material related to this article can be found online at https://doi.org/10.1016/j.carbon.2025.121089.

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