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Van der Waals contacts between three-dimensional metals and two-dimensional semiconductors

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As the dimensions of semiconducting channels in field effect transistors (FETs) decrease, the contact resistance of metal-semiconductor interface at the source and drain electrodes dominates the performance of devices[1–3]. Two dimensional (2D) transitional metal dichalcogenides (TMDs) such as molybdenum disulfide (MoS_2) have been demonstrated to be excellent semi-conductors for ultra-thin FETs[4,5]. However, unusually high contact resistance has been observed across the metal-2D TMD interface[3,5–9]. Recent studies have shown that van der Waals (vdW) contacts formed by transferred graphene[10,11] and metals[12] on few layered TMDs provide good properties. However, vdW contacts between a three-dimensional metal and single layer 2D TMDs have yet to be demonstrated. Here, we report the realization of ultra-clean vdW contacts between indium metal (thickness = 10 nm) capped with gold (thickness = 100 nm) electrodes and monolayer MoS_2. Using scanning transmission electron microscopy (STEM) imaging, we show that indium and Au layers form an In/Au solid solution after annealing at 200°C and that the In/Au-MoS_2 interface is atomically sharp with no detectable chemical interaction between the metal and 2D TMD, suggesting van-der-Waals-type bonding between the metal and single layer MoS_2. The contact resistance of indium/gold electrodes is ~ 3000 ± 300 Ω-μm for single layer and ~ 800 ± 200 Ω-μm for few layered MoS_2 – amongst the lowest observed for 3D metal electrodes evaporated on MoS_2 and is translated into high performance FETs with mobility of ~ 167 ± 20 cm^2-V^{-1}-s^{-1}. We also demonstrate low contact resistance of 220 ± 50 Ω-μm on ultrathin NbS_2 and near ideal band offsets, indicative of defect free interfaces, in WS_2 and WSe_2 contacted with indium. Our work provides a simple method for making ultra-clean vdW contacts using standard laboratory technology on single layer 2D semiconductors.

FETs using 2D semiconductors as the channel material offer excellent gate electrostatics, which allows mitigation of short channel effects – making them interesting for sub-10 nm node devices[13]. However, in short channel devices, the transport through the semiconductor is nearly ballistic and virtually all of the power is dissipated at the contacts[1]. Thus, optimizing the contacts between 2D semiconductors and metal electrodes is an important technological challenge. Several strategies such as phase engineering to create lateral metal-semiconductor-metal

54 heterojunctions[14], formation of clean interfaces via vdW contacts using graphene[10,11], mechanical
55 transfer of metal films[12] and using h-BN as tunnel barrier[15] have been reported for improving the
56 electrical properties of contacts on 2D materials. The main challenge in making contacts on
57 atomically thin materials exposed to atmosphere is the presence of adsorbed water or
58 hydrocarbons layers on their surface. The thickness of these layers is comparable to that of 2D
59 semiconductors so that when metal electrodes are deposited, the adsorbed contaminants are
60 incorporated at the interface between the metal and the 2D semiconductor. This leads to creation
61 of interface states that can pin the Fermi level and increase the contact resistance[16]. It is possible
62 to minimize the impact of adsorbed layers by depositing metal electrodes in ultra-high
63 vacuum[17,18], which reduces the contact resistance. In addition, transfer of thin metal films[12] or
64 few layered mechanically exfoliated h-BN[15] on top of 2D semiconductors can squeeze out
65 adsorbed layers. However, even when the adsorbed layer is removed, the direct deposition of
66 metal can lead to substantial damage *via* kinetic energy transfer or chemical reaction between the
67 metal atoms and 2D semiconductor. Studies have shown that creation of vdW contacts via metal
68 transfer[12], graphene[10,11] or h-BN[15] on 2D semiconductors can create clean interfaces without
69 damaging the underlying 2D semiconductor. However, all of these strategies for improving
70 contact properties have been reported for multi-layer 2D semiconductors and clean interfaces
71 with low contact resistance have yet to be reported on single layers.

72 We have characterized the ultra-clean vdW interface formed between single layer 2D MoS_2
73 and indium/gold (In/Au) electrodes deposited using a standard laboratory thermal evaporator at
74 normal vacuum (< 10^{-6} Torr) using annular dark field (ADF) scanning transmission electron
75 microscope (STEM) and X-ray photoelectron spectroscopy (XPS). The electrodes consist of 10
76 nm of In capped with 100 nm of Au to prevent reaction of In with the environment. The

77 schematic of the FET device tested in this work is shown in Fig. 1a (see Methods for details of
78 electrode deposition and device fabrication). To image and study the interface of In and MoS_2,
79 we conducted cross-sectional ADF STEM study. It is well known that single and few-layered
80 TMDs are damaged during metal deposition[12,16] and only dry transfer of electrodes provide clean
81 and intact interfaces[12]. In contrast, our analysis reveals that the In-MoS_2 interfaces for single
82 (Fig. 1b, broader view image is provided in Extended Data Fig. 1a) and few layered (Extended
83 Data Fig. 1b) MoS_2 are atomically sharp with no detectable evidence of reaction between the
84 indium metal and molybdenum disulfide layers. ADF and BF (bright field) STEM images in Fig.
85 1b clearly show the single layer MoS_2 and In/Au alloy contact on top with atomic resolution.
86 ADF intensity profile across the interface for In/Au on monolayer MoS_2 revealed that the
87 spacing between the sulfur atoms and In/Au atoms is 2.4 Å ± 0.3 Å (Extended Data Fig. 1c) –
88 indicating that the indium metal gently deposits on the 2D semiconductor. Our chemical analysis
89 reveals that only vacuum in the form of vdW gap is observed at the interface and no evidence for
90 oxidation or indium sulfide formation can be observed. X-ray photoelectron spectroscopy (XPS)
91 was performed to characterize the chemistry at the interface between the upper most sulfur layer
92 and In/Au alloy. The binding energy values for the Mo 3d and S 2p doublets were found to be
93 229.3 eV (Mo $3d_{5/2}$) and 162.1 eV (S $2p_{3/2}$) – typical of pristine MoS_2[19]. Nonstoichiometric
94 Mo_xS_y peaks were not observed, as indicated in Fig. 1c. Additional information about the
95 chemical state of the interface is provided in the form of In 3d spectra and In MNN Auger
96 measurements in Extended Data Fig. 1e and 1f. We corroborated this using electron energy loss
97 spectra (EELS) in Fig. 1d. The EELS was measured using a focused electron beam probe with
98 spatial resolution of ~ 0.8 Å so that the spectra from highly localized regions at the interface
99 could be obtained. It can be seen that the sulfur $L_{2,3}$-edge exhibits experimentally negligible

100 difference between the topmost MoS_2 layer in contact with the indium metal and the fifth layer
101 of MoS_2 – suggesting the deposition of indium does not introduce any chemical reactions,
102 distortions, or strain at the metal/semiconductor interface or within the 2D MoS_2.

103 To investigate whether the excellent structural features of vdW contacts with indium metal can
104 be translated into better device performance, we measured the contact resistance using transfer
105 length method (TLM) and also the FET properties. The TLM results shown in Fig. 2a for indium
106 electrodes on CVD grown single layer MoS_2 (see Extended Data Fig. 1g and 1h) reveal contact
107 resistance of ~ 3.3 ± 0.3 kΩ-µm (at $n = 5.0 \times 10^{12}$ cm^{-2}) and values of 800 ± 200 Ω-µm (at $n =$
108 3.1×10^{12} cm^{-2}, Extended Data Fig. 2a) were measured for few-layered mechanically exfoliated
109 MoS_2. The higher contact resistance in single layer MoS_2 compared to the few-layered material
110 can be attributed to substrate-carrier scattering[17]. Despite this, the contact resistances of In/Au
111 electrodes on single layer (Fig. 2b, 2c) and few-layered MoS_2 (Extended Data 2b, 2c) are among
112 the lowest reported in the literature (Extended Data Table 1) thus far at all carrier concentrations
113 that we measured and at low temperature. For comparison, Au electrodes deposited in ultra-high
114 vacuum have slightly higher contact resistance than In/Au devices (Fig. 2b,c) and the contact
115 resistance of graphene side contacts on h-BN encapsulated few-layered MoS_2 at 100 K has been
116 measured to be 1200 Ω-µm (at $n = 6.85 \times 10^{12}$ cm^{-2})[15].

117 Typical transfer and output curves for In/Au contacted single layer MoS_2 as the channel in
118 FETs are shown in Fig. 2d and 2e. The devices were fabricated on off-the-shelf thermal SiO_2
119 (300 nm) on Si and were not encapsulated. Despite this, the transfer characteristics such as the
120 one shown in Fig. 2d exhibited sharp turn on and high currents with mobility values reaching
121 167 ± 20 cm^2-V^{-1}-s^{-1}. Measurements of mobility with temperature reveals that the phonon-
122 limited mobility scales as $\mu \propto T^{-1}$ at low temperatures and as $\mu \propto T^{-1.6}$ at high temperatures

123 because of acoustic phonon scattering (Extended Data Fig. 2f)[23]. The FETs also exhibit linear
124 output characteristics both at room temperature and at low temperatures (Extended Data Fig. 2d
125 and 2e), suggesting the absence of a Schottky barrier. The highest current density we obtained
126 for multi-layered MoS_2 FETs was 196 μA/μm (see Extended Data Table 1 for comparison with
127 literature). Measurements as a function of temperature reveal Schottky barrier height to be
128 around 110 meV (Extended Data Fig. 2h), which is consistent with work function of the metal
129 and conduction band energy level of MoS_2.

130 In addition to MoS_2, we have also deposited In/Au on other TMDs such as NbS_2, WS_2 and
131 WSe_2. It can be seen from Fig. 3a that we obtain a contact resistance of 220 Ω-μm for NbS_2
132 grown by CVD, which is among the lowest values reported for any metal contact on a 2D TMD.
133 The TLM plot in Fig. 3b shows that the contact resistance for WS_2 is 2.4 ± 0.5 kΩ-μm, which is
134 also amongst the lowest reported in the literature as indicated by the summary of results shown
135 in Fig. 3c. The low contact resistance in WS_2 translates into better FET performance as indicated
136 by the transfer characteristics shown in Fig. 3d where substantially higher mobility (83 ± 10 cm^2-
137 V^{-1}-s^{-1}) can be observed for indium contacts in comparison with titanium electrodes (1.2 ± 1 cm^2-
138 V^{-1}-s^{-1}). Output curves of WS_2 devices are given in Extended Data Fig. 3.

139 We have also confirmed the formation of ultra-clean interface on WSe_2. Cross-sectional ADF
140 STEM image of indium electrodes on two layers of WSe_2 shown in Fig. 4a reveal clean vdW
141 interface with spacing of 2.94 Å between the metal and Se, as indicated in the schematic. In/Au
142 alloy electrodes on WSe_2 yield ambipolar FET characteristics with the electron current being
143 higher than the hole current, as shown in Fig. 4b. The output results for both p and n-type
144 devices are provides in Fig. 4c. The resistance for electron injection in 16 kΩ-μm and for holes it
145 is 225 kΩ-μm. These large values are consistent with the large energy offsets between the Fermi

146 level of indium (4.10 eV), the conduction (3.50 eV) and valence (4.83 eV) bands of WSe_2 (see
147 inset of Fig. 4b). Our measurements reveal that the energy barrier for hole injection is 0.73 eV
148 and the energy barrier for electrons is 0.60 eV. Thus, we expect the hole current to be less than
149 electron current with In/Au electrodes, consistent with our measurements. The energy barriers
150 for carrier injection into WSe_2 matches ideally with the band offsets and the FET properties. This
151 also suggests that the indium contacts form clean interfaces with WSe_2 without the creation of
152 defects or local reactions. Comparison of resistance values with literature shown in Fig. 4d and
153 4e reveal that the indium contacts yield the lowest resistance values and both the electron and
154 hole currents are higher.

155 Finally, the soft nature of indium allows it to readily form stable alloys with other metals
156 (Extended Data Fig. 4 and 5). This property can be used to adjust the work function of electrodes
157 to facilitate electron or hole injection while maintaining the ultra-clean interface. To demonstrate
158 this, we have deposited ~ 3 nm of In with high work function Pd metal on top. Kelvin force
159 microscopy results shown in Extended Data Fig. 6 shows that the work function of the alloy is
160 slightly increased, as indicated in the inset of Fig. 4b. Typical transfer curves of FET devices
161 with In/Pd alloy electrodes given in Fig. 4b exhibit higher hole current and lower electron current
162 due to the increased work function. The measurements indicate that the energy barrier for hole
163 injection is 0.63 eV and the energy barrier for electrons is 0.7 eV. The free adjusted barrier
164 height indicates clean interface between WSe_2 and In alloy without Fermi level pinning.

165 In sum, our results demonstrate ultra-clean vdW contacts on variety of truly two-dimensional
166 semiconductors. The resulting devices from such clean contacts exhibit excellent performance.
167 Our results should lead to realization of potential of ultra-thin electronics based on 2D
168 semiconductors.

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240

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247

248 **Author Contributions** MC conceived the idea, supervised the project, awrote the paper. YW
249 prepared and measured all devices. JCK, HYJ performed FIB and STEM on single layer MoS_2,
250 NbS_2, WSe_2. RJW and AM performed STEM on few layered MoS_2. JM assisted in making
251 contacts and measured work functions. XS synthesized 2D materials by CVD. JY performed
252 XPS and analyzed data. FZ assisted in device fabrication and In deposition. All authors read the
253 paper and agreed to its content.
254

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256 www.nature.com/reprints. The authors declare no competing financial interests.
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261

262 **Figure Captions:**

263

264 **Figure 1 | Atomic resolution imaging and chemical analyses of In-MoS_2 interface. a,** Device
265 structure of bottom gate FET used in this study. The electrodes consist of 10 nm of In capped
266 with 100 nm of Au. The ellipse under the contact indicates the interface region that was analyzed
267 using high resolution scanning transmission spectroscopy (STEM). **b,** Atomic resolution images
268 of In/Au on single layer MoS_2. (ii) Low-pass filtered annular dark field (ADF) STEM image
269 showing Mo, S and In atoms as indiacted by the enlarged image in (i). (iii) Corresponding bright
270 field (BF) STEM image of the monolayer. Scale bars = 5 Å. **c,** X-ray photoelectron spectrocopy
271 (XPS) of In/Au-MoS_2 interface showing pristine Mo and S peaks. The XPS also shows that the
272 deposition of In/Au does not modify the MoS_2. **d,** Electron energy loss spectroscopy (EELS) of S
273 $L_{2,3}$-edge showing that the sulfur atoms of the top layer are completely unaffected by the
274 deposition of metal on top. The sulfur peaks of the topmost and the fifth layer are the same
275 within the measurement precision.

276 **Figure 2 | Contact resistance and device properties of In/Au electrodes on single layer**
277 **MoS_2. a,** Contact resistance extracted using the transmission line method (TLM). **b,** Contact
278 resistance versus carrier concentration for In electrodes at room temperature (filled points) and at
279 80 K (open points). Au electrodes deposited in ultra-high vacuum (10^{-9} Torr) are provided for
280 comparison[18]. **c,** comparison of contact resistance from literature and our results for different
281 types of electrode materials[6,7,11,18,20–22]. **d,** Typical transfer characteristics of a field effect
282 transistor with monolayer MoS_2 as the channel and In/Au alloy as the source/drain electrodes,
283 length and width of the device are 2 and 6 μm. Mobility of ~ 170 cm^2-V^{-1}-s^{-1} can be achieved
284 with In/Au electrodes. **e,** Linear output characteristics indicating the absence of a contact barrier.

285 **Figure 3 | Contact properties of In/Au electrodes on 2D NbS_2 and WS_2. a,** TLM contact
286 resistance of In/Au electrodes on CVD grown NbS_2. **b,** TLM contact resistance of In/Au
287 electrodes on mechanical exfoliated WS_2. **c,** Contact resistance *versus* carrier concentration from
288 different studies reported in the literature[6,8,24–26]. It can be seen that the In/Au electrodes exhibit
289 the lowest values. **d,** Transfer characteristics of FETs with WS_2 as the channel material and
290 In/Au contacts, length and width of the device are 1 and 1.2 μm. Transfer curve of Ti contacted
291 WS_2 device is included for comparison, length and width of the devices are 0.5 μm and 2 μm,
292 respectively. In/Au devices show substantially better mobility (~ 85 cm^2-V^{-1}-s^{-1}) than devices
293 with Ti electrodes (~ 1 cm^2-V^{-1}-s^{-1}).

294 **Figure 4 | In alloy contacts on ultra-thin WSe_2. a,** Atomic resolution ADF image and
295 corresponding schematic of In-WSe_2 interface showing a clear vdW gap corresponding to
296 spacing between Se-Se. (ii) Intensity profile of (i) showing the distance between the bottom
297 metal and top selenium is 2.9 Å. **b,** Ambipolar transfer characteristics showing n-type dominant
298 behavior with In/Au contacts and hole dominant behavior with In/Pd contacts. Length and width
299 of the In/Au contacted device are 1 μm and 2 μm and In/Pd device are 0.5 μm and 1 μm. The
300 inset provides the energy band levels of WSe_2 and metal. **c,** Linear output characteristics of the
301 device. **d, e,** Comparison of contact resistance and drain current with those reported in the
302 literature[9,27–33].

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310 **METHODS**

311 **Sample preparation and device fabrication.** Single-layer MoS_2 were grown by chemical vapor
312 deposition (CVD) using MoO_3 and sulfur powder as precursors. 100 mg of MoO_3 and 400 mg of
313 sulfur were placed in two small tubes in the upstream of the tube furnace. A small drop of
314 perylene-3,4,9,10 tetracarboxylic acid tetrapotassium salt (PTAS) was dropped on SiO_2/Si
315 substrates as seed for growing. The substrates were placed face-up on top of Alumina boat in the
316 center of the furnace. Air was evacuated by flowing Ar (Ultrahigh purity, Air Gas) for 15 min at
317 200 sccm. The tube was heated at 200 ^{o}C for 15 min to remove moisture from the precursors.
318 Then the temperature was increased to 870 ^{o}C under a 90 sccm Ar flow and the MoO_3 and S
319 source were heat to 250 ^{o}C and 170 ^{o}C, respectively. After 20 min, the furnace was cooled down
320 to room temperature and the samples were removed from the furnace.
321 Few-layered TMDs were prepared by mechanically exfoliating flakes from bulk crystal (MoS_2,
322 WS_2, WSe_2 purchased from HQ graphene) via the scotch tape method. Thermally grown 300 nm
323 SiO_2 substrates on heavily doped Si were used as the gate insulator and electrode, respectively.
324 Monolayer or multilayer flakes were identified with optical microscopy and AFM. Then e-beam
325 lithography was used to pattern the electrodes. Before metal electrode deposition, the
326 evaporation system was pumped to a base pressure of $< 10^{-6}$ torr. Then, 10 nm of Indium metal
327 was deposited with a low rate of 0.2 Å/s and 100 nm of Au was deposited subsequently. The
328 device was rinsed with isopropanol after immersing in acetone for liftoff. Once the fabrication
329 process was completed, all devices were annealed at 200 ^{o}C in H_2/Ar gas for one hour before
330 measurements.

331

332 **Measurements.** Transport characteristics were measured by applying voltage with Keithley
333 4200. The low temperature measurements were performed in vacuum probe station with liquid
334 nitrogen and a temperature controller. X-ray photoelectron spectroscopy (XPS) was measured by
335 the Thermo Scientific K-Alpha system. AFM and SKPM are measured by Park NX-Hivac
336 system. PL data was collected using a 532-nm laser excitation focused through a $\times$ 100 objective
337 lens. The spectra was taken at an incident laser power of 50 μW, which was sufficiently low to
338 avoid any damage to the sample.

339

340 **Schottky barrier extraction.** Schottky barrier height of the contact was extracted by measuring
341 the activation energy in the thermionic emission region. In a Schottky Barrier FET, the reverse-
342 biased contact consumes most of the voltage drop and dominates the transistor behavior. The
343 current density of thermal emission through a metal-semiconductor contact is:

344 $$J = A^{*}T^{\alpha}\exp\left[-\frac{q\Phi_{B0}}{k_{B}T}\right]\left[1-\exp(-\frac{qV}{k_{B}T})\right] \quad (1)$$

345 Where A* is the Richardson constant, V is the applied voltage, T is the temperature, α is an
346 exponent equal to 2 for bulk semiconductors and 3/2 for 2D semiconductors, and k_B is the
347 Boltzmann's constant. Using this equation, the slope of the Richardson plot, $\ln(I/T^{3/2})$ ~1/T,
348 yields Φ_{B0} as a function of gate voltage. The gate voltage at which the Schottky barrier height
349 tends to curve away from the linear dependence is where the flat band condition occurs because
350 after the gate voltage reaches this condition carriers are transferred through tunneling as well. To
351 extract Schottky barrier height, we identify the voltage at which Φ_{B0} stops linearly depending on
352 V_g. As shown in Extended Data Figure 2f, the Schottky barrier of In/MoS_2 is 110 meV.
353
354 **STEM specimen preparation and acquisition parameters.** Cross sectional TEM lamellas of
355 the FET samples were prepared using a FEI Helios NanoLab G4 focused ion beam (FIB). The
356 cross-sectional STEM images of a single layer MoS_2 were taken at 200 keV using a FEI Titan^3
357 G2 60-300 with a double-side spherical aberration (Cs) corrector. The probe convergence semi-
358 angle was set to be ~ 25 mrad. ADF STEM images were acquired from 50-200 mrad range. All
359 EELS measurements were collected in dual-mode to enable simultaneous collection of a zero-
360 loss and a core-loss spectrum to compensate for energy drift during specimen acquisition. It is
361 worth noting that the energy drift was tested by continuous collection of zero-loss spectra for ~5
362 mins to ensure a reasonable energy drift (< 0.3 eV) before beginning any data acquisitions.
363

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397
398 **Data availability.** The data that support the findings of this study are available from the
399 corresponding author upon reasonable request.
400
401

402 **Extended Data Figure 1 | Atomic resolution imaging and chemical analyses of In-MoS_2**
403 **interface. a,** Broader view STEM images of 3D metal on 2D semiconductor. Cross-section
404 STEM image of interface between In/Au and monolayer MoS_2. Scale bar = 5 nm. **b,** Cross-
405 section STEM image of interface between In/Au and multi-layered MoS_2. Scale bar = 2 nm. **c,**
406 Bright field STEM of In/Au contact to monolayer MoS_2. The intensity profile shows that the
407 interface metal to first layer sulfur distance is ~ 2.4 Å. **c,** ADF- STEM and intensity profile of
408 In/Au contact to multilayer MoS_2. The intensity profile shows that the MoS_2 interlayer distance
409 is 6.2 Å, which is consistent with literature[34]. Sulfur to sulfur distance between two layers is 2.7
410 Å and the interface metal to first layer sulfur distance is also ~ 2.7 Å for multi-layered samples,
411 indicating van der Waals contact at the interface. **e,** X-ray photoelectron spectrocopy (XPS) of
412 In/Au-MoS_2 interface shows In metal $3d_{5/2}$ (443.8eV) and $3d_{3/2}$ (451.4eV) peaks along with In
413 metal loss features. **f,** X-ray induced Auger spectrum showing pristine Indium metal peak at
414 402.9 eV. In_2O_3 has a clear peak at 400.2 eV, which is absent in our samples. There is no sign of
415 In_2S_3 (407.3 eV) and indium NNM Auger spectra indicates no chemical reaction at the
416 interface[35]. **g,** Atomic force microscopy (AFM) image of CVD grown single layer MoS_2. **h,**
417 Photoluminescence (PL) of CVD MoS_2, A exciton peak at 1.84 eV and B exciton peak at 1.97
418 eV are clealry visible.
419

420 **Extended Data Figure 2 | Contact resistance and device properties of In/Au electrodes on**
421 **few-layered MoS_2. a,** TLM results of In/Au contacted few-layered MoS_2. **b,** Contact resistance
422 versus carrier concentration for In/Au electrodes. Sc, Ti and Au electrodes deposited in ultra-
423 high vacuum (10^{-9} Torr) are provided for comparison[5,17]. **c,** comparison of contact resistance
424 from literature and our results for different types of electrode materials[17,36–41] . **d,** Typical output

425 curve at room temperature shows that the highest current density is 196 μA/μm. **e,** Output
426 characteristics at low temperature, linear output characteristics indicating the absence of a
427 contact barrier. **f,** Mobility versus temperature reveals phonon-limited property at low
428 temperature and acoustic phonon scattering at high temperature. **g,** Transfer characteristics with
429 temperature showing metal-insulator transition. **h,** Schottky barrier extraction indicating ideal In
430 contacts with MoS_2, insert is energy band diagram of MoS_2 and In.
431
432 **Extended Data Figure 3 | Output characteristics of WS_2. a,** In contacts. **b,** Ti contacts.
433
434 **Extended Data Figure 4 | Energy-dispersive X-ray spectroscopy (EDS) mapping of the**
435 **contact. a,** Low resolution cross-sectional TEM image of the MoS_2 with In/Au contact. **b-e**,
436 Elemental mapping showing the distribution of In, Au, S, and O. In and Au overlap over the
437 entire metal layer, suggesting the formation of an alloy. S is observed underneath the In and Au.
438 O is obtained primarily from SiO_2 of the substrate. **f**, Diffraction Fourier transform pattern from
439 metal electrode showing alloying between In and Au. The diffraction pattern is of a FCC alloy.
440 Pure In has BCC crystal structure.
441
442 **Extended Data Figure 5 |** Typical transfer characteristics of the same device measured
443 immediately after fabrication and after 70 days.
444
445 **Extended Data Figure 6 | Topographical and Scanning Kelvin Probe Microscopy (SKPM)**
446 **images. a, d,** Topographical and surface potential results of Au sample, the work function (WF)
447 extracted is 5.09 eV, similar to the theoretical value. **b, e,** Topographical and surface potential
448 results of In/Au sample, the work function extracted is very close to In work function, 4.05eV. **c,**

449 **f,** Topographical and surface potential results of In/Pd sample, the work function extracted is

450 4.23eV, higher than that of In/Au.

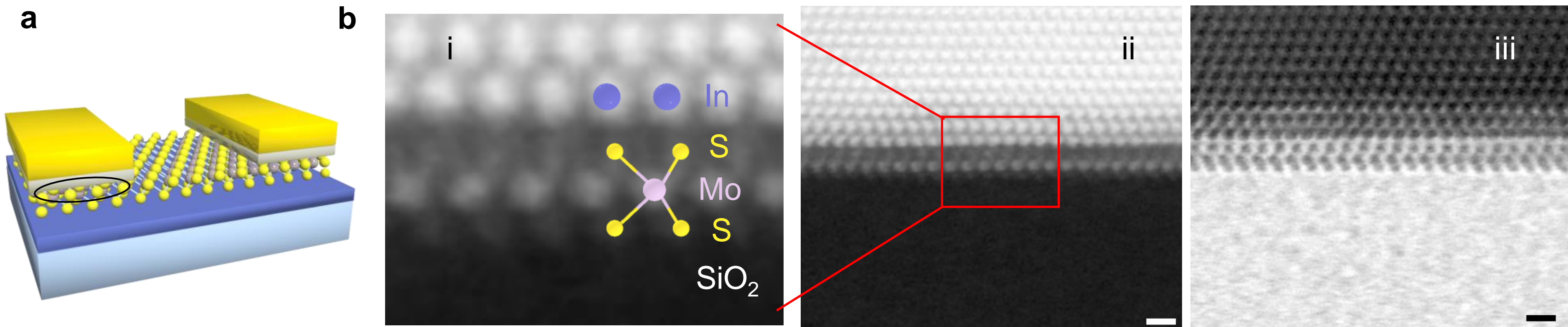
451

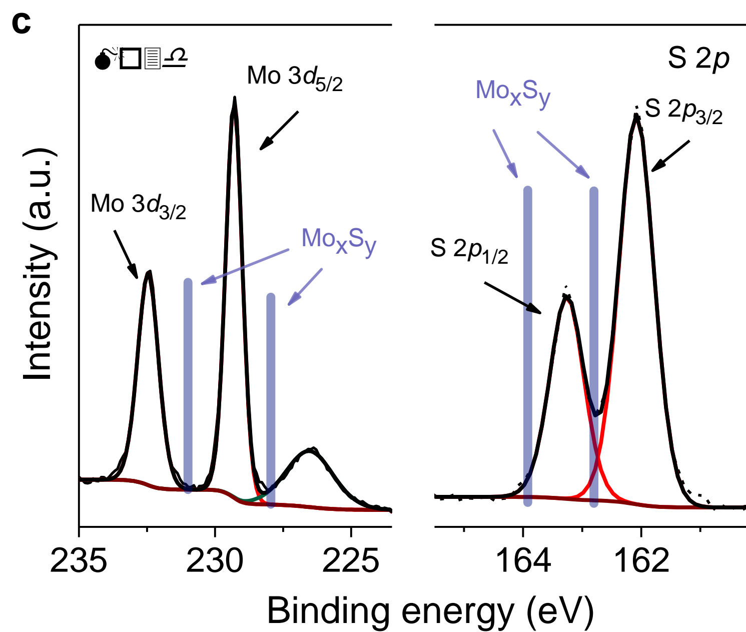
452

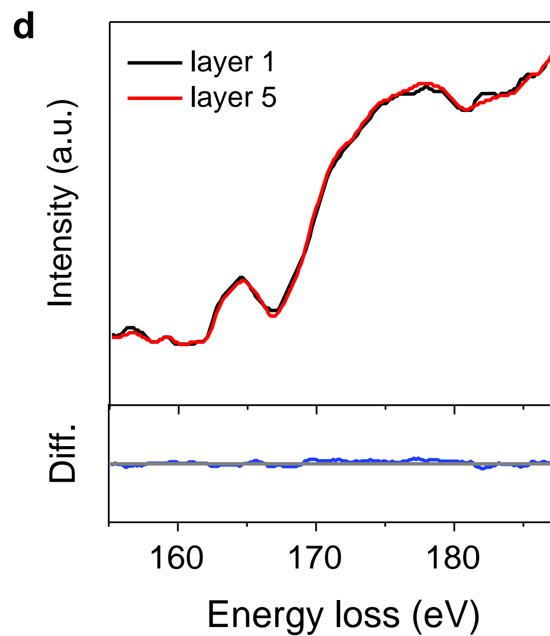
Method	Channel length (μm)	EOT	Gate voltage (V)	Drain voltage (V)	I on (μA/μm)	Contact resistance, (kΩ·μm)	reference
	Monolayer MoS_2						
In/Au clean contact	2	300 nm SiO_2	40	1	18	3	This work
Graphene contact	5	285 nm SiO_2	80	0.1	0.8	NA	10
Graphene edge contact	7	30 nm HfO_2	3	0.025	0.1	59	6
Graphene/Ag	4	300 nm SiO_2	80	1	5	115	11
Co/h-BN	0.2	BN+285 nm SiO_2	80	0.01	0.1	6	15
Au UHV	1.2	90 nm SiO_2	35	1	12	5	18
Cr contact	1	285 nm SiO_2	40	1	4	40	16
Re doping	10.5	300 nm SiO_2	80	0.1	0.05	26.25	20
Ag/Au	4	30 nm SiO_2	25	1	17	12	22
Double gate	0.1	B: 285 nm SiO_2 T: 16 nm Al2O_3	40	1	12	10	21
1T'/Au	10	285 nm SiO_2	50	1	1.8	NA	42
Al_2O_3 passivation	1.5	300 nm SiO_2	100	1	0.5	NA	43
	Multilayer MoS_2						
In/Au clean contact	0.5	300 nm SiO_2	40	3	196	0.8	This work
Sc	5	15 nm Al_2O_3	8	3	160	NA	5
Graphene contact	5	285 nm SiO_2	60	0.1	1	NA	10
Transferred Ag metal	0.16	BN+90 nm SiO_2	40	3	660	NA	12
Phase engineering	1.2	300 nm SiO_2	30	5	85	0.24	14
Au UHV	0.5	90 nm SiO_2	25	1	75	2	17
Graphene edge contact, h-BN cap	5	285 nm SiO_2	80	0.05	0.2	2.5	39

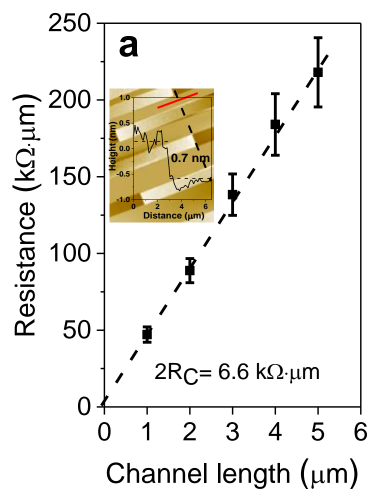
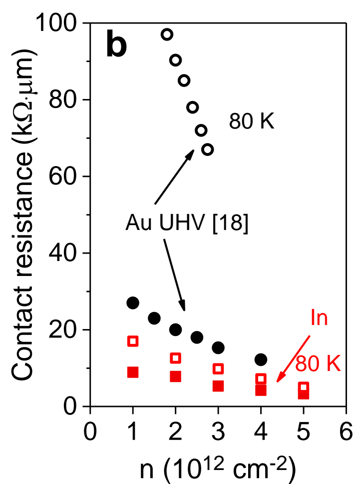
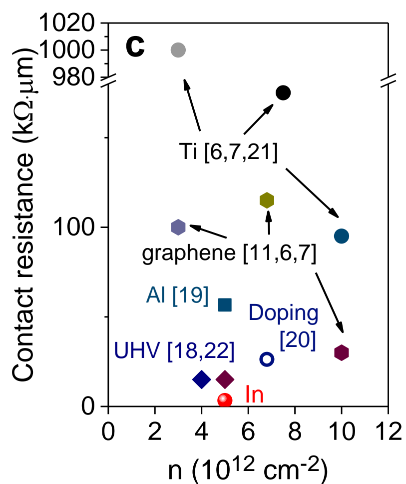
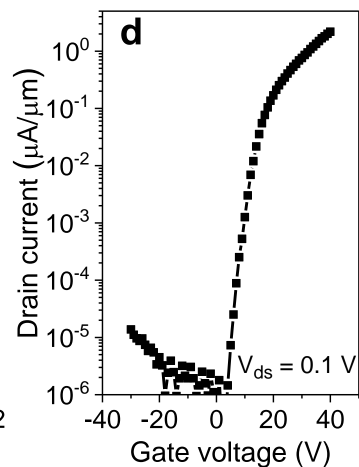
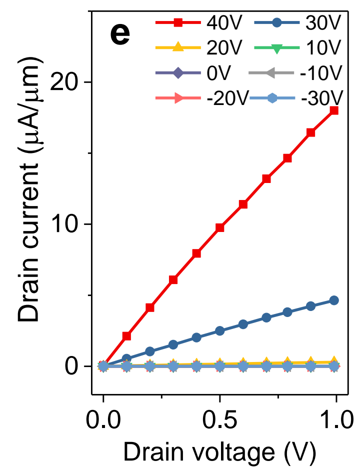
h-BN tunneling	0.3	255 nm SiO_2	40	1	30	4	[41]
Fermi level de-pining	1.5	90 nm SiO_2	20	3	24	5.4	[44]
Thiol-Molecules doping	2	300 nm SiO_2	40	3	50	25.2	[45]
Cl doping	0.5	90 nm SiO_2	50	1.2	200	0.5 (2×10^{13} cm^{-2})	[46]
K doping	0.5	B: 285 nm SiO_2 T: 17.5 nm ZrO_2	40 1.5	2.5	15	NA	[47]
Mo	2	72 nm Al_2O_3	30	3	140	2 (4×10^{13} cm^{-2})	[48]
Edge contact	2.2	300 nm SiO_2	30	0.48	0.8	205	[49]

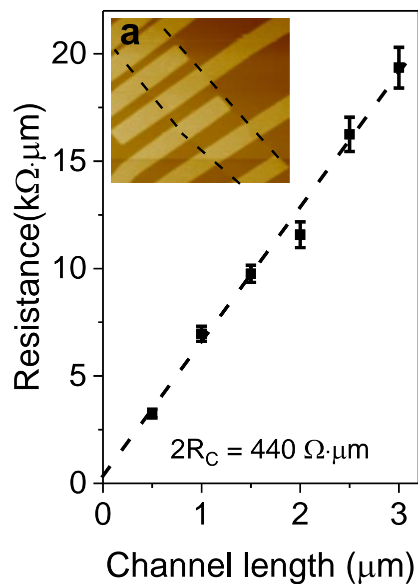
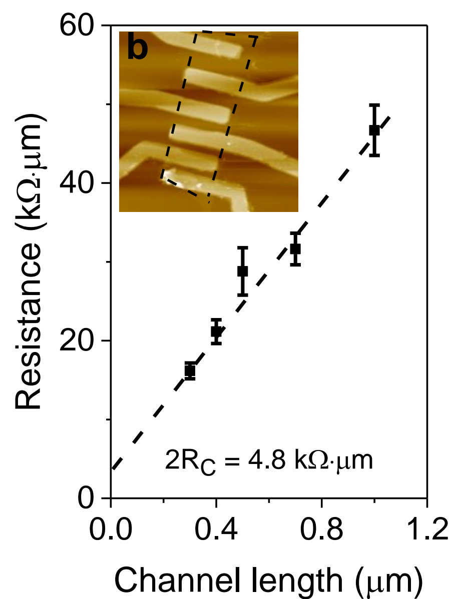
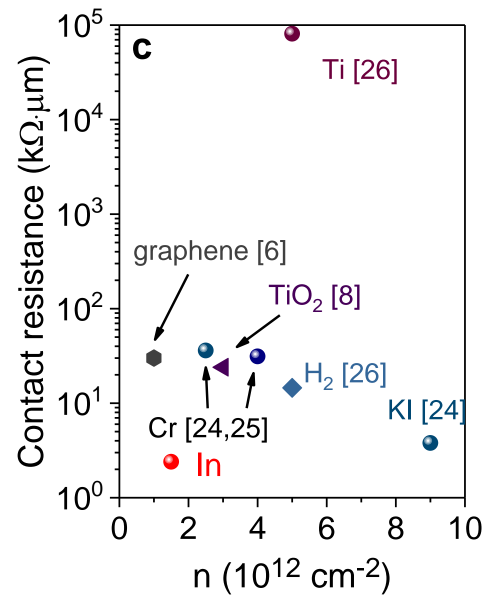
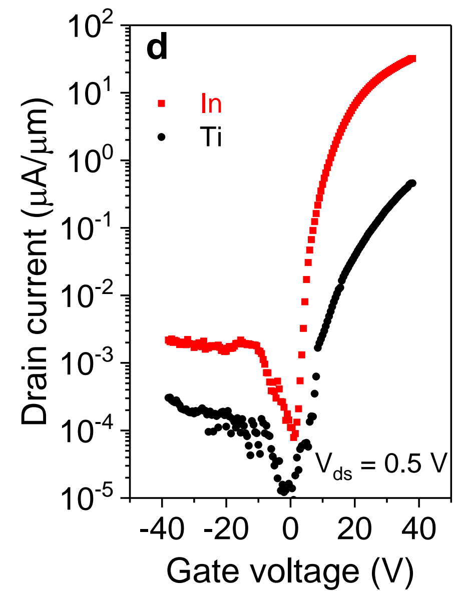
Extended Data Table 1 | Literature survey of device performance. Contact resistances are extracted at carrier concentration around 3×10^{12} cm^{-2} for multilayer MoS_2 and 5×10^{12} cm^{-2} for monolayer MoS_2 except where indicated otherwise.


a
b
i
In
S
Mo
S
SiO2
ii
iii

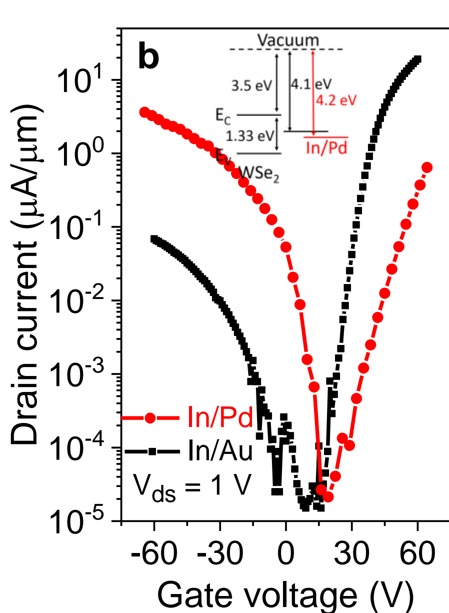

c
Mo 3d5/2
Mo 3d3/2
MoxSy
S 2p
MoxSy
S 2p3/2
S 2p1/2
Intensity (a.u.)
235
230
225
164
162
Binding energy (eV)

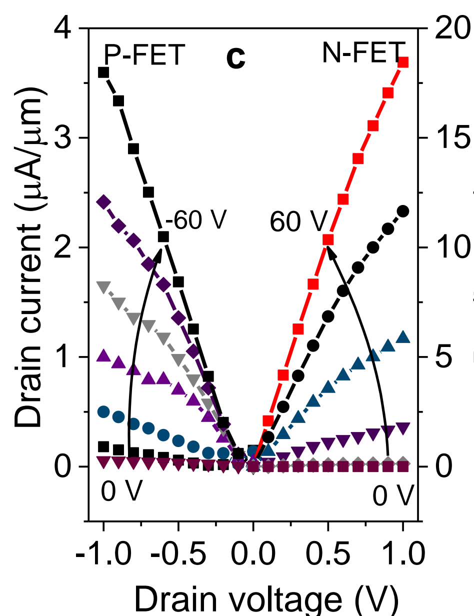

d
layer 1
layer 5
Intensity (a.u.)
Diff.
160
170
180
Energy loss (eV)

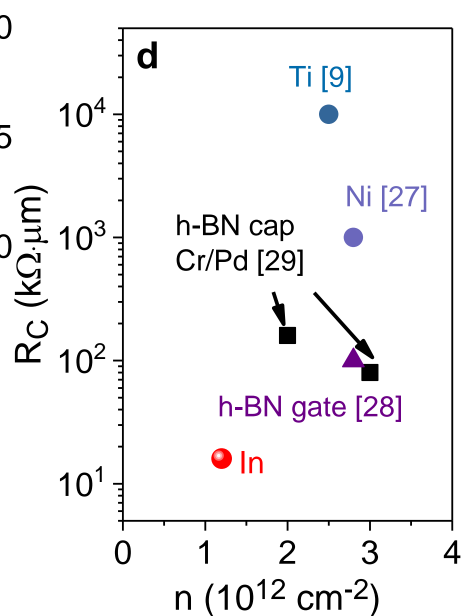

a
Resistance (kΩ·µm)
Channel length (µm)
2R_C= 6.6 kΩ·µm
0.7 nm
Distance (µm)
Height (nm)

b
Contact resistance (kΩ·µm)
n (10^12 cm^-2)
80 K
Au UHV [18]
In
80 K

c
Contact resistance (kΩ·µm)
n (10^12 cm^-2)
Ti [6,7,21]
graphene [11,6,7]
Al [19]
Doping
[20]
UHV [18,22]
In

d
Drain current (µA/µm)
Gate voltage (V)
V_ds = 0.1 V

e
Drain current (µA/µm)
Drain voltage (V)
40V
30V
20V
10V
0V
-10V
-20V
-30V

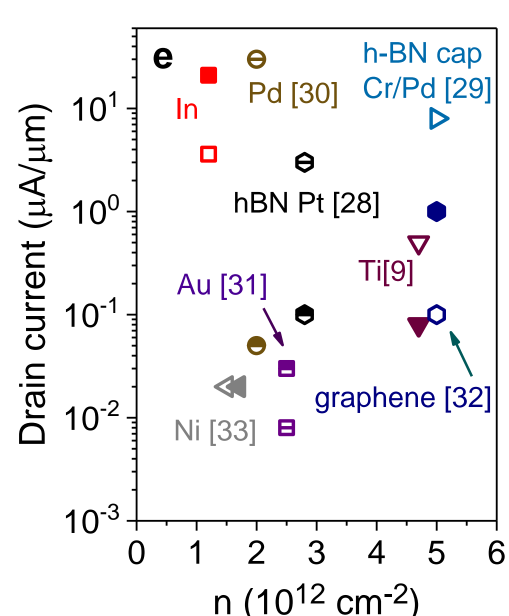

a
Resistance(kΩ·μm)
Channel length (μm)
2R_C = 440 Ω·μm
0
5
10
15
20
0
1
2
3

b
Resistance (kΩ·μm)
Channel length (μm)
2R_C = 4.8 kΩ·μm
0
20
40
60
0.0
0.4
0.8
1.2

c
Contact resistance (kΩ·μm)
n (10^12 cm^-2)
Ti [26]
graphene [6]
TiO2 [8]
H2 [26]
KI [24]
Cr [24,25]
In

d
Drain current (μA/μm)
Gate voltage (V)
In
Ti
V_ds = 0.5 V
-40
-20
0
20
40

a
i
2.9 Å
3.1 Å
ii
metal
W
Se
Se
Intensity (a.u.)
0.0
0.5
1.0
1.5
Distance (nm)


b
Vacuum
3.5 eV
4.1 eV
4.2 eV
Ec
1.33 eV
Ev
In/Pd
WSe2
Drain current (μA/μm)
In/Pd
In/Au
Vds = 1 V
-60
-30
0
30
60
Gate voltage (V)


c
P-FET
N-FET
-60 V
60 V
0 V
0 V
Drain current (μA/μm)
Drain voltage (V)
-1.0
-0.5
0.0
0.5
1.0


d
Ti [9]
Ni [27]
h-BN cap
Cr/Pd [29]
h-BN gate [28]
In
RC (kΩ·μm)
n (10^12 cm^-2)


e
In
Pd [30]
h-BN cap
Cr/Pd [29]
hBN Pt [28]
Ti[9]
Au [31]
graphene [32]
Ni [33]
Drain current (μA/μm)
n (10^12 cm^-2)